MC9300/MC8300 Series

The MTTL complex functions are designed for digital applications in the medium to high-speed range.

These MTTL devices provide significant reduction in package count and increased logic per function over devices in the basic MTTL and MDTL families.

INDEX

Function	Operating Temperature Range		Packages		
			Dual-in-line		
	−55°C TO +125°C	0°C TO +75°C	Plastic	Ceramic	Flat
Universal 4-Bit Shift Register	MC9300	MC8300	P	L	F
BCD to Decimal Decoder	MC9301	MC8301	P	L	F
Dual Full Adder	MC9304	MC8304	P	L	F
Presettable Decade Up/Down Counter	MC9306	MC8306	P	L	F
7-Segment Decoder	MC9307	MC8307	P	L	F
Dual 4-Bit Latch	MC9308	MC8308	P	L	F
Dual 4-Channel Data Selector	MC9309	MC8309	P	L	F
Presetable Decade Counter	MC9310	MC8310	P	L	F
One of Sixteen Decoder	MC9311	MC8311	P	L	F
8 Channel Data Selector	MC9312	MC8312	P	L	F
4 Bit Latch	MC9314	MC8314	P	L	F
4 Bit Binary Counter	MC9316	MC8316	P	L	F
7 Segment Decider/Driver	MC9317	MC8317	P	L	F
8 Input Priority Encoder	MC9318	MC8318	P	L	F
Quad 2 Input Multiplexer	MC9322	MC8322	P	L	F
5 Bit Comparator	MC9324	MC8324	P	L	F
Dual 8 Bit Shift Register	MC9328	MC8328	P	L	F
One Shot Multivibrator	MC9601	MC8601	P	L	F
Dual One Shot Multivibrator	MC9602	MC8602	P	L	F

UNIVERSAL
4-BIT SHIFT REGISTER

MC9300
MC8300

Compatible with all MTTL and MDTL families.

Input Loading Factor
J, $\overline{K}$, $\overline{MR}$, D_{P0}, D_{P1}, D_{P2}, D_{P3} = 1
$\overline{PE}$ = 2.3
Clock = 4

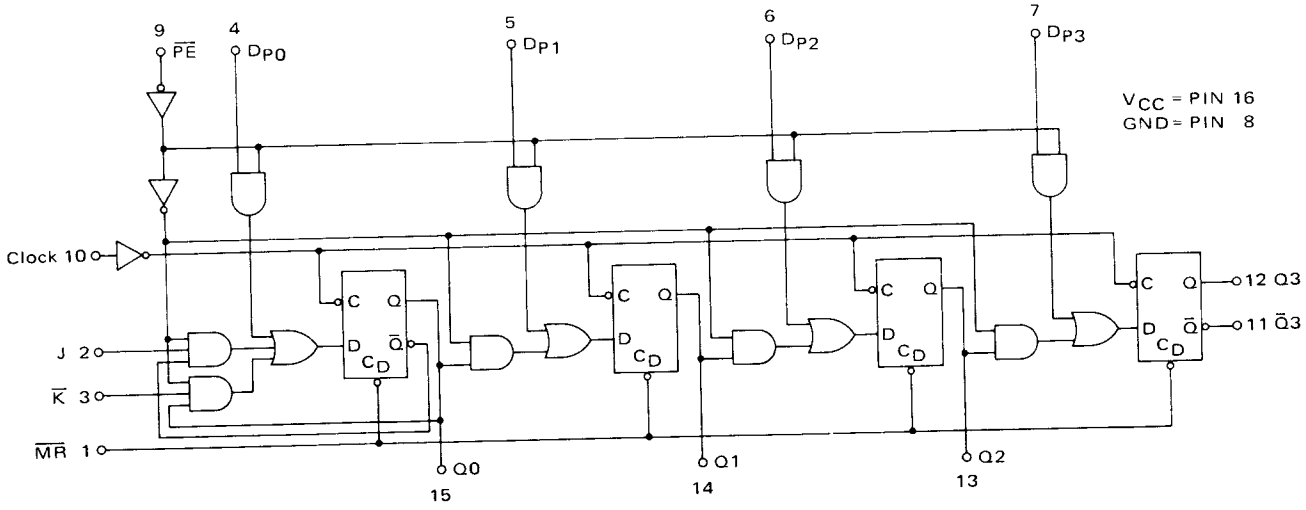
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg

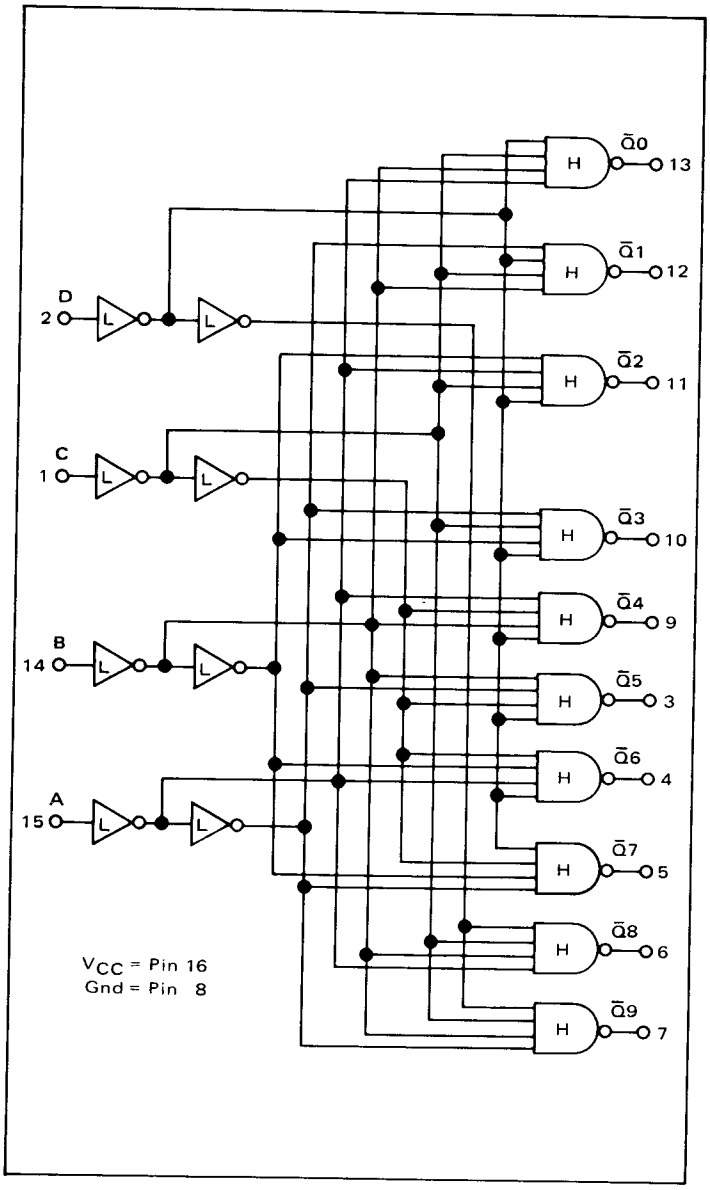
Propagation Delay Time = 25 ns typ

This serial/parallel shift register consists of four flip-flops operated in the synchronous mode. Functions available are shift left, shift right, serial-to-serial, parallel-to-parallel, serial to-parallel, and parallel-to-serial conversion.

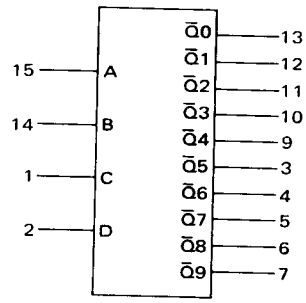
This device operates on the positive-going edge of the clock pulse in both the serial and parallel mode. The device includes an internal clock buffer, input clamp diodes to reduce ringing, Q outputs for all four stages, $\overline{Q}$ output for the last stage, synchronous parallel entry, and an asychronous master reset. The J and $\overline{K}$ inputs are available, and may be tied together to produce a D input.



MC9301
MC8301



This decoder converts four-bit BCD inputs to select one-of-ten outputs. The selected output is in the logic "0" state while all other outputs are in the logic "1" state. When a binary code greater than nine is applied to the inputs, all outputs will be in the logic "1" state. This device is useful in memory selection, industrial control, and data routing applications.



Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 125 mW typ/pkg
Propagation Delay Time = 22 ns typ

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

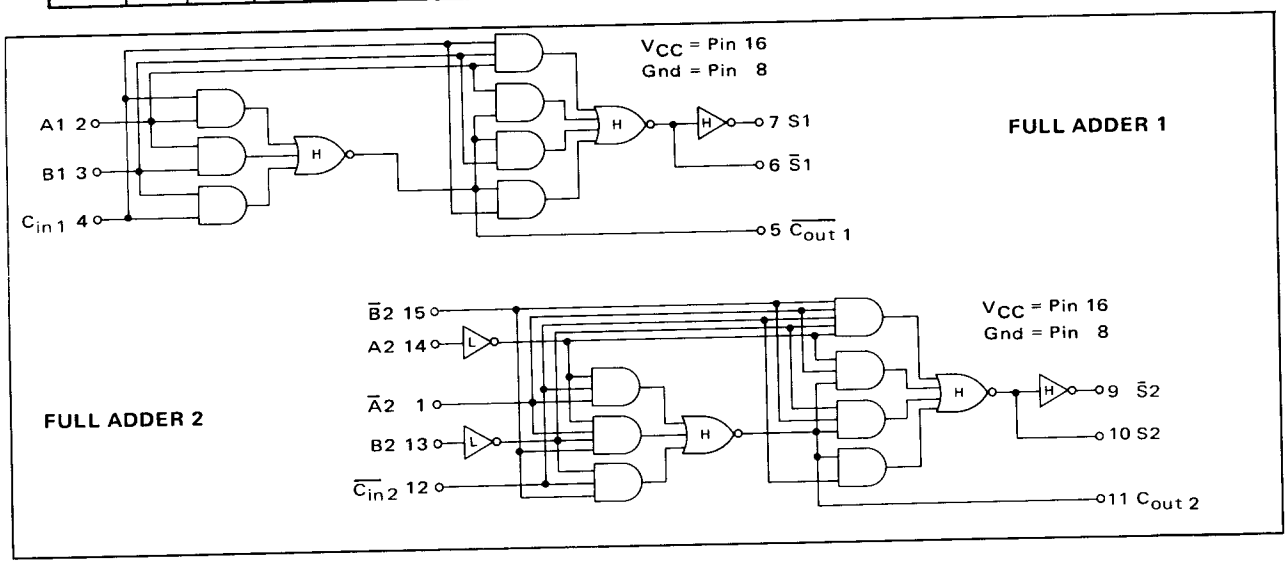
DUAL FULL ADDER

MC9304
MC8304

This device consists of two independent, high-speed, binary full adders, with complementary Sum outputs. Adder two has provisions for both active high and active low inputs. Carry In and Carry Out of adder two are complementary to those of adder one. These choices provide greater design flexibility and minimum package count.

ADDER 1

INPUT			OUTPUT		
C_{in1}	B1	A1	$\overline{C_{out1}}$	$\overline{S1}$	S1
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1



Input Loading Factors:
Adder 1: A1, B1, C_{in1} = 4
Adder 2: $\overline{A2}$, $\overline{B2}$, $\overline{C_{in2}}$ = 4
A2, B2 = 1

Output Loading Factors:
Adder 1: $\overline{C_{out1}}$ = 7
S1 = 10
$\overline{S1}$ = 9
Adder 2: C_{out2} = 7
S2 = 9
$\overline{S2}$ = 10

Total Power Dissipation = 110 mW typ/pkg

TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	t_{pd-}		t_{pd+}	
	$\overline{C_{out}}$	$\overline{S}$	$\overline{C_{out}}$	$\overline{S}$
C_{in}	8.0	–	8.0	–
A1	–	25	–	28

ADDER 2

INPUT					OUTPUT		
$\overline{C_{in\,2}}$	B2	A2	$\overline{B2}$	$\overline{A2}$	$C_{out\,2}$	S2	$\overline{S2}$
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	1

MC9306
MC8306

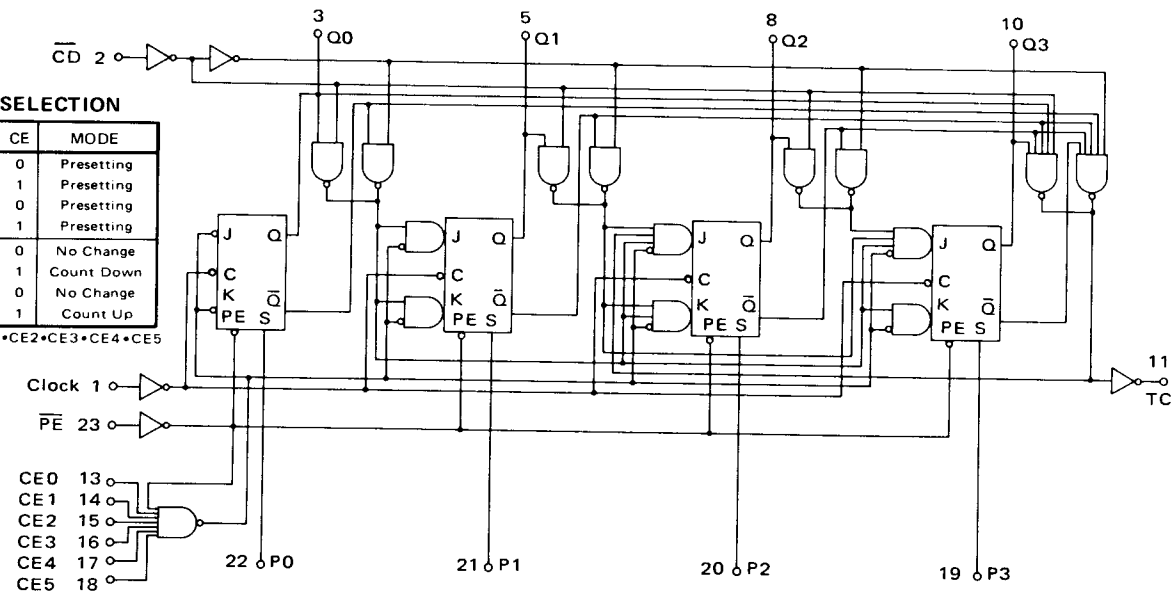
Add Suffix L for 24-pin dual in-line ceramic package (Case 623).
Suffix P for 24-pin dual in-line plastic package (Case 649) MC8306 only.

The MC9306/8306 decade counter is constructed of four master-slave J-K flip-flops driven synchronously. Parallel inputs (P0 thru P3) provide synchronous loading capability. Outputs from each stage (Q0 thru Q3) are available. An active low enable ($\overline{PE}$) allows entry of data into the preset inputs (P0 thru P3). The Count Enable inputs (CE0 thru CE5) and the terminal count (TC) output provide for cascading of up to seven stages without external gating. A single count mode input ($\overline{CD}$) determines the direction of count.

MODE SELECTION

$\overline{PE}$	CD	CE	MODE
0	0	0	Presetting
0	0	1	Presetting
0	1	0	Presetting
0	1	1	Presetting
1	0	0	No Change
1	0	1	Count Down
1	1	0	No Change
1	1	1	Count Up

CE = CE0•CE1•CE2•CE3•CE4•CE5



V_{CC} = Pin 24
Gnd = Pin 12

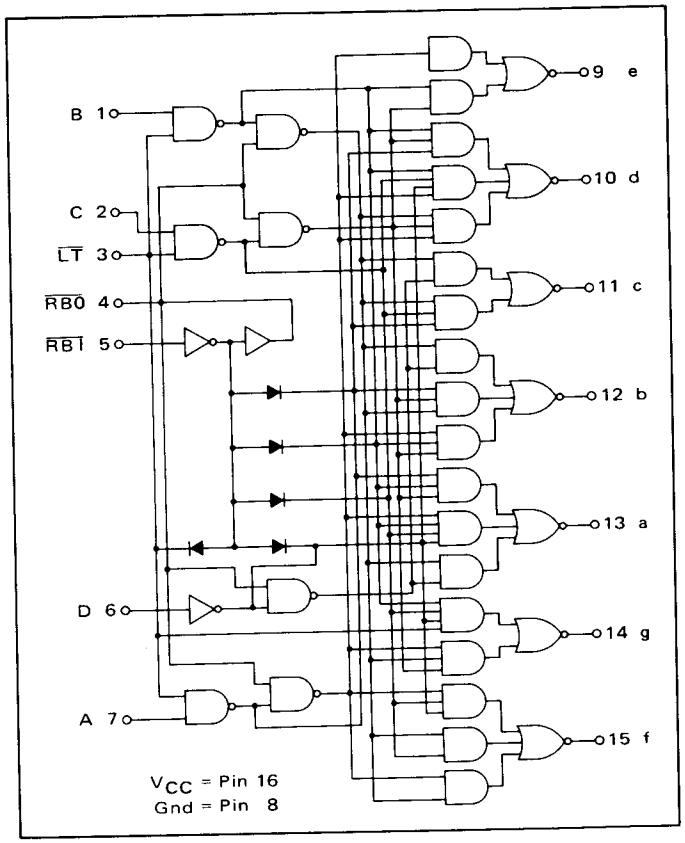
Total Power Dissipation = 350 mW typ/pkg.
Propagation Delay Time (Clock to Q) = 20 ns typ
Toggle Frequency = 18 MHz typ

Input Loading Factor:
$\overline{CD}$, CE = 1
Clock, $\overline{PE}$ = 2
P0, P1, P2, P3 = 2/3
Output Loading Factor = 6

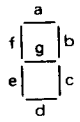
$T_C = \overline{CD} \bullet Q0 \bullet \bar{Q}1 \bullet \bar{Q}2 \bullet Q3 + \overline{CD} \bullet \bar{Q}0 \bullet \bar{Q}1 \bullet \bar{Q}2 \bullet \bar{Q}3$

BCD-TO-SEVEN SEGMENT DECODER

MC9307
MC8307

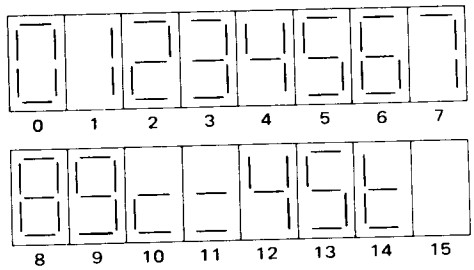


This device decodes a 4-bit BCD code input and produces outputs suitable for use with seven-segment display indicators. Active high outputs permit a buffer transistor to be used directly to provide the high currents required for incandescent displays. The device has provision for automatic blanking of non-significant zeros in a multi-digit decimal number, resulting in an easily readable display. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The decoder has an active low Lamp Test input which over-rides all other inputs to test for display segment malfunctions.



SEGMENT IDENTIFICATION

NUMERICAL DESIGNATION – SEGMENTS ILLUMINATED



	MC9307	MC8307
Input Loading Factors		
A, B, C, D	1	1
$\overline{RBI}$	1	0.5
LT	5	4.3
Output Loading Factors		
a thru g	8	7
$\overline{RBO}$	2	1.5

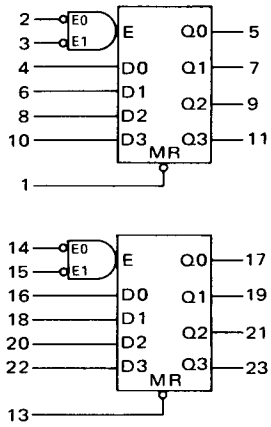
Total Power Dissipation = 165 mW typ/pkg
Propagation Delay Time (Input to Segment Outputs) = 250 ns typ

TRUTH TABLE

DIGIT OR FUNCTION	INPUT						OUTPUT							
	$\overline{LT}$ Pin 3	$\overline{RBI}$ Pin 5	D Pin 6	C Pin 2	B Pin 1	A Pin 7	a Pin 13	b Pin 12	c Pin 11	d Pin 10	e Pin 9	f Pin 15	g Pin 14	$\overline{RBO}$ Pin 4
8	0	X	X	X	X	X	1	1	1	1	1	1	1	1
	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	0	1	1	1	1	1
3	1	X	0	0	1	1	1	1	1	1	0	0	1	1
4	1	X	0	1	0	0	0	1	1	0	0	1	1	1
5	1	X	0	1	0	1	1	0	1	1	0	1	1	1
6	1	X	0	1	1	0	1	0	1	1	0	1	1	1
7	1	X	0	1	1	1	1	1	1	0	0	0	0	1
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1
9	1	X	1	0	0	1	1	1	1	1	0	1	1	1
10	1	X	1	0	1	0	0	0	0	1	1	0	1	1
11	1	X	1	0	1	1	0	0	0	1	0	0	1	1
12	1	X	1	1	0	0	0	1	1	0	0	1	1	1
13	1	X	1	1	0	1	1	0	1	1	0	1	1	1
14	1	X	1	1	1	0	1	0	0	1	0	1	1	1
15	1	X	1	1	1	1	0	0	0	0	0	0	0	1

X = Don't care

MC9308
MC8308



V_{CC} = Pin 24
GND = Pin 12

Input Loading Factors:
D0, D1, D2, D3 = 1.5
$\overline{MR}$, $\overline{E}0$, $\overline{E}1$ = 1.0
Output Loading Factor = 9

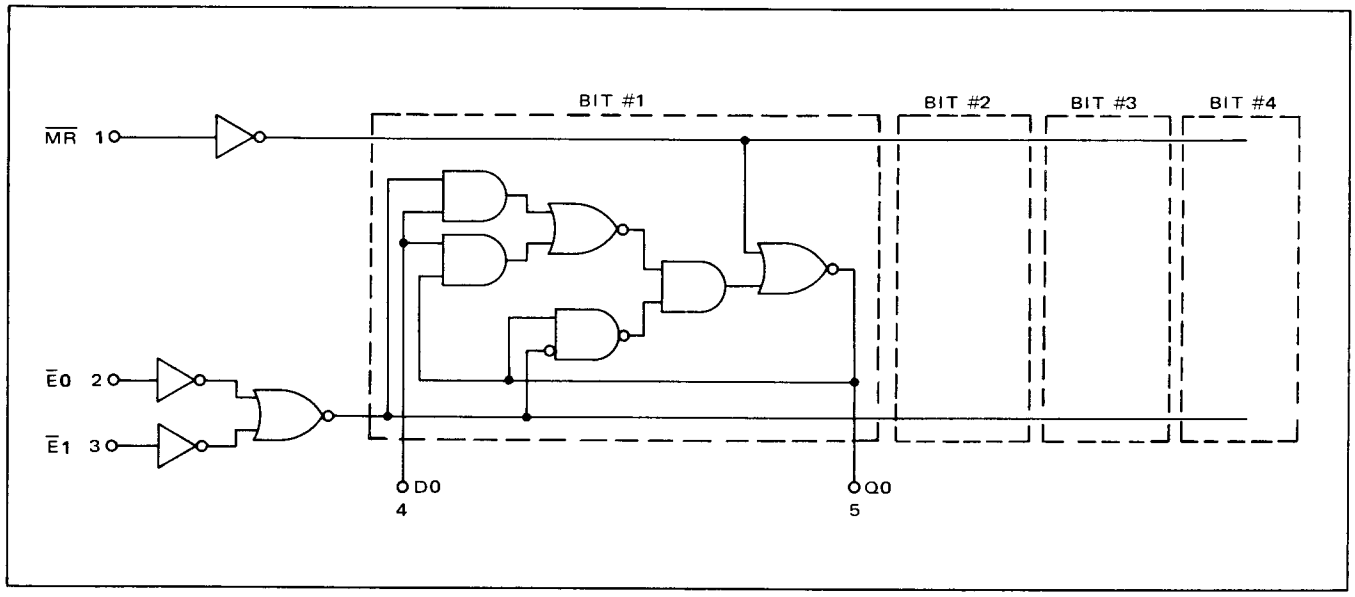
Total Power Dissipation = 325 mW typ/pkg
Propagation Delay Time (Enable to Output) = 25 ns typ

This device is constructed of AND, NAND, and NOR gates. Each half of the device contains four latches with common enable ($\overline{E}0$) and $\overline{E}1$) and common Master Reset ($\overline{MR}$). Data entered at the D input of each latch will appear at the corresponding Q output if the enable inputs are in the logic "0" state. When the enable inputs are in the logic "1" state, each latch will maintain the information present when the enable inputs were last in the logic "0" state. The master reset input overrides all other input states. When a logic "0" is applied to the $\overline{MR}$ input, all outputs of the quad latch will be forced to a logic "0".

INPUTS							OUTPUTS			
$\overline{MR}$	$\overline{E}0$	$\overline{E}1$	D3	D2	D1	D0	Q3	Q2	Q1	Q0
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0	0	0	1
1	0	0	0	0	1	0	0	0	1	0
1	0	0	0	0	1	1	0	1	0	0
1	0	0	1	0	0	0	1	0	0	0
1	0	0	0	0	1	1	0	0	1	1
1	0	0	0	1	0	0	0	1	0	1
1	0	0	1	0	0	1	1	0	0	1
1	0	0	0	1	1	0	0	1	1	0
1	0	0	1	0	1	1	1	0	1	1
1	0	0	0	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	0	0
1	0	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	0	1
1	0	0	1	1	1	0	1	1	1	0
1	0	0	1	1	1	1	1	1	1	1
1	0	1	X	X	X	X	LATCHED			
1	1	0	X	X	X	X	LATCHED			
1	1	1	X	X	X	X	LATCHED			
0	X	X	X	X	X	X	0	0	0	0

X = Don't Care

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN

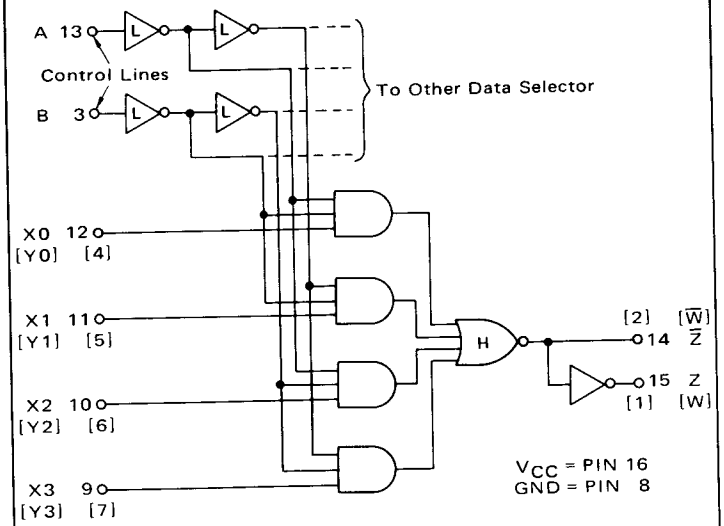


DUAL 4-CHANNEL
DATA SELECTOR

MC9309
MC8309L

1/2 OF DEVICE SHOWN

(Numbers and symbols in parenthesis are for other half of device)



$$Z = \bar{A}\bar{B}X0 + A\bar{B}X1 + \bar{A}BX2 + ABX3$$
$$\bar{Z} = \bar{A}\bar{B}\bar{X0} + A\bar{B}\bar{X1} + \bar{A}B\bar{X2} + AB\bar{X3}$$
$$W = \bar{A}\bar{B}Y0 + A\bar{B}Y1 + \bar{A}BY2 + ABY3$$
$$\bar{W} = \bar{A}\bar{B}\bar{Y0} + A\bar{B}\bar{Y1} + AB\bar{Y2} + AB\bar{Y3}$$

Input Loading Factor = 1

Output Loading Factor: $Z, W = 10$
$\bar{Z}, \bar{W} = 9$

Total Power Dissipation = 150 mW typ/pkg

This device consists of two four-channel data selectors with common control lines, constructed from high-level AND-OR-INVERT gates with active pullup outputs, and low-level inverters on the control inputs. By selecting one of four logic combinations, information on one of the four data inputs will be routed to the complementary outputs.

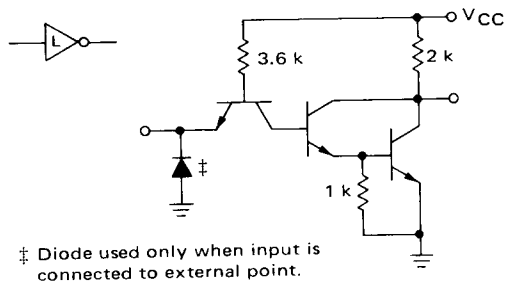
Data selectors are useful in applications where digital data is to be routed from one of several registers or locations to another register or location for processing.

The MC9309/8309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss.

TYPICAL PROPAGATION DELAY TIMES (ns)
$T_A = 25^oC$

INPUT	Z	$\bar{Z}$	CONDITIONS
A	24	16	X0 = X2 = X3 = logic "0", X1 = logic "1". A and B are defined by the logic equations.
X1	17	9	

LOW-LEVEL INVERTER



‡ Diode used only when input is connected to external point.

PRESETTABLE
DECADE COUNTER

MC9310
MC8310L

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

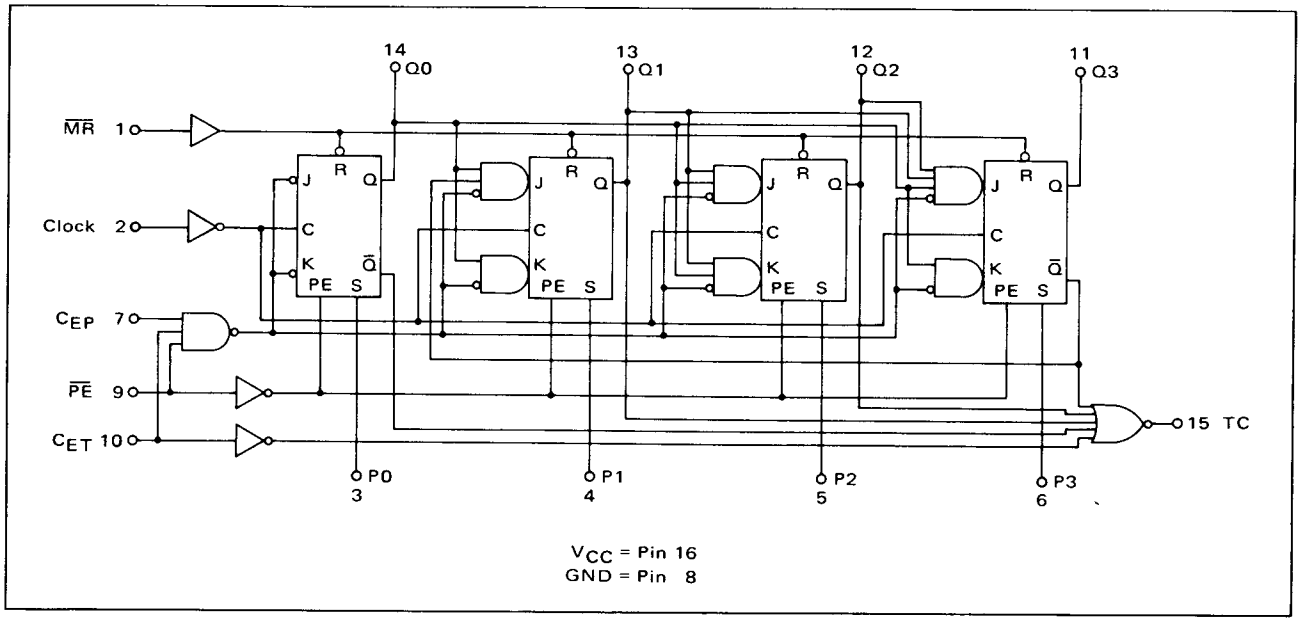
The MC9310/8310 decade counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

Input Loading Factors:
$\overline{MR}$, C_{EP} = 1
Clock, $\overline{PE}$, C_{ET} = 2
P0, P1, P2, P3 = 2/3
Output Loading Factor = 6

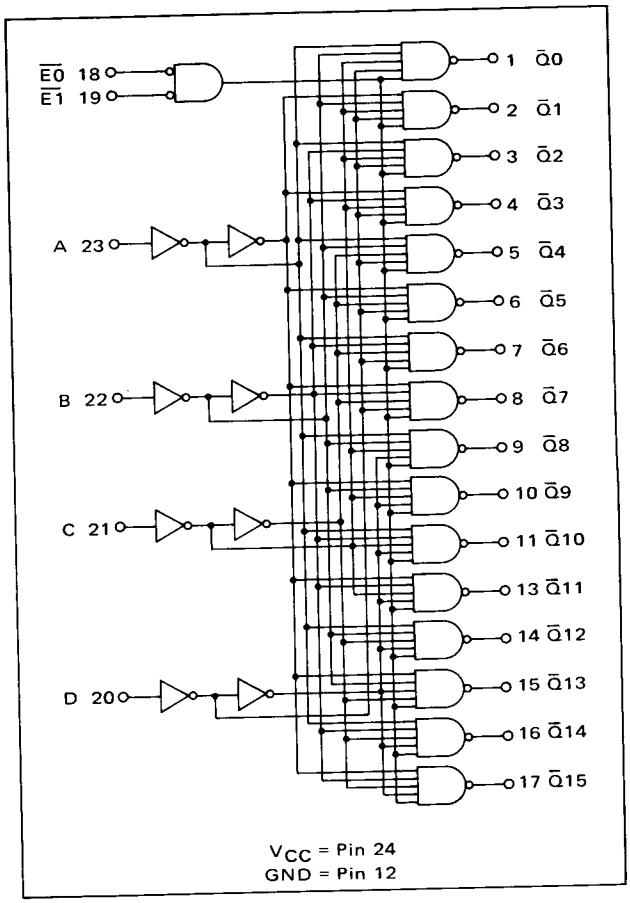
Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 14 to 35 ns typ
Toggle Frequency = 28 MHz typ



V_{CC} = Pin 16
GND = Pin 8

ONE-OF-SIXTEEN DECODER

MC9311
MC8311



This device converts four BCD inputs to select one of sixteen outputs. The selected output is in the logic "0" state while all other outputs are in the logic "1" state. Two $\overline{\text{Enable}}$ inputs are provided for increased logic capability. This device is useful in memory selection control and data routing applications.

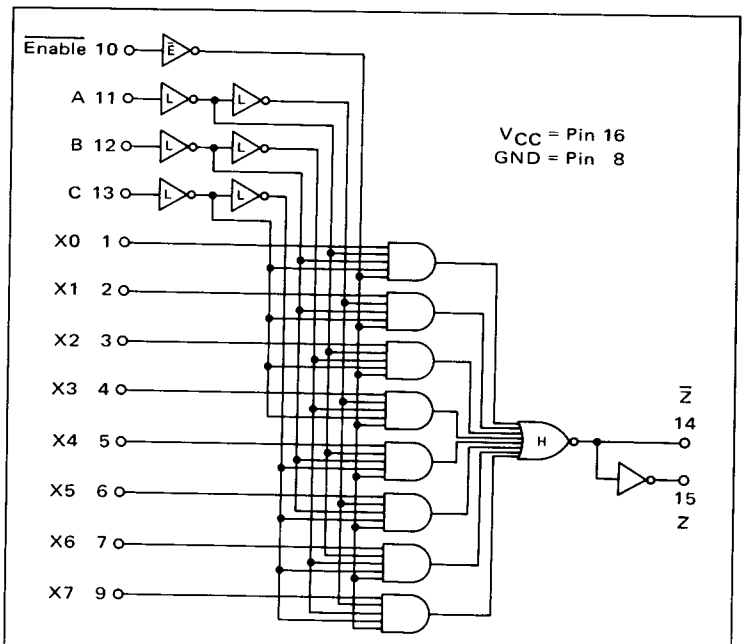
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 175 mW typ/pkg
Propagation Delay Time $\overline{\text{Enable}}$ to Output = 26 ns max

INPUT						OUTPUT															
$\overline{E0}$	$\overline{E1}$	D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

X = Don't care

MC9312
MC8312



$Z = E \cdot (\bar{A}\bar{B}\bar{C}X0 + A\bar{B}\bar{C}X1 + \bar{A}B\bar{C}X2 + AB\bar{C}X3 + \bar{A}\bar{B}CX4 + A\bar{B}CX5 + \bar{A}BCX6 + ABCX7)$

$\bar{Z} = E \cdot (\bar{A}\bar{B}\bar{C}\bar{X0} + A\bar{B}\bar{C}\bar{X1} + \bar{A}B\bar{C}\bar{X2} + AB\bar{C}\bar{X3} + \bar{A}\bar{B}C\bar{X4} + A\bar{B}C\bar{X5} + \bar{A}BC\bar{X6} + ABC\bar{X7})$

Input Loading Factor = 1

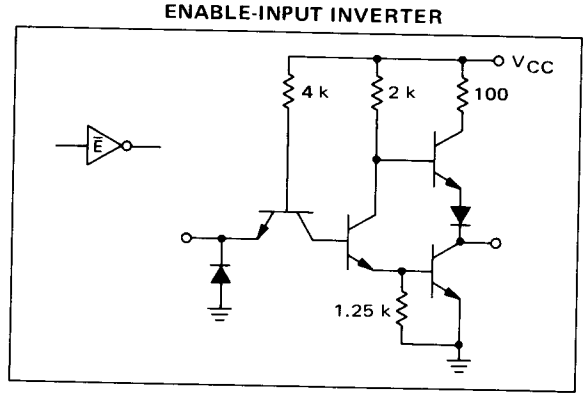
Output Loading Factor:
High: Z = 20, $\bar{Z}$ = 18
Low: Z = 10, $\bar{Z}$ = 9

Propagation Delay Time = 24 ns typ

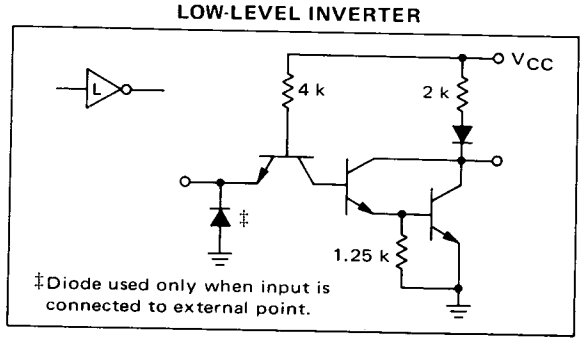
Power Dissipation = 135 mW typ/pkg

This 8-channel data selector is constructed from high-level and low-level gates interconnected as shown in the logic diagram. It is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of the select inputs, A, B, and C. Complementary outputs are provided. The $\overline{\text{Enable}}$ input is active in the low state. When the $\overline{\text{Enable}}$ input is high, the $\bar{Z}$ output is high and the Z output low, regardless of the state of the other inputs.

ENABLE-INPUT INVERTER



LOW-LEVEL INVERTER



‡Diode used only when input is connected to external point.

QUAD LATCH

MC9314
MC8314

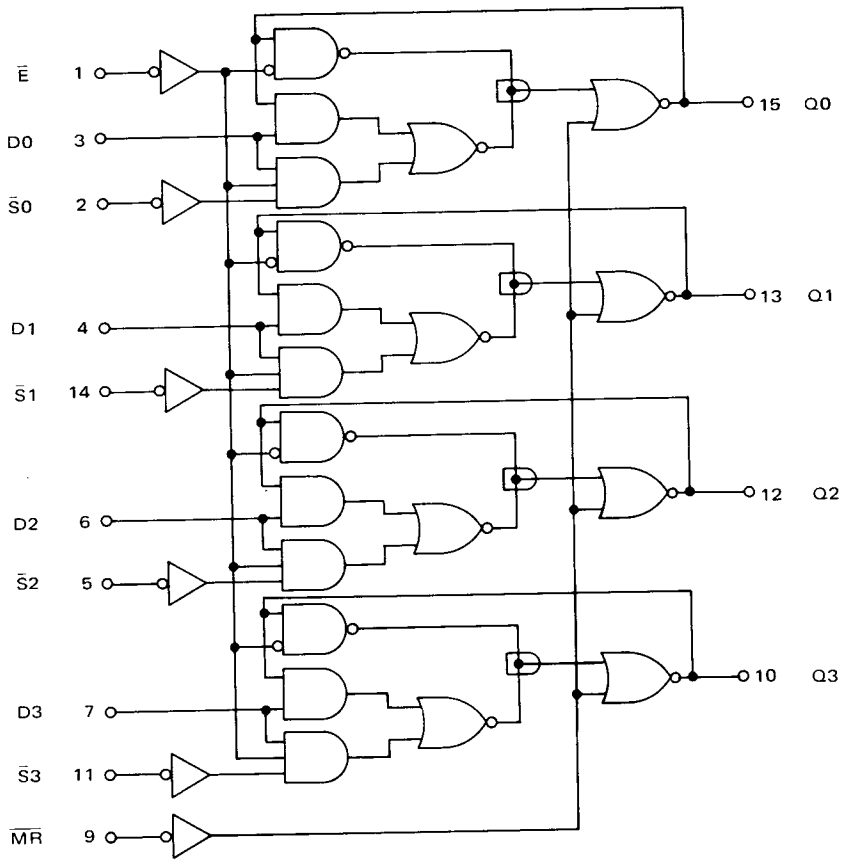
The MC9314/8314 four-bit latch can be used mainly for storage of information. In this versatile device, storage can be achieved in different ways by combining the states of the D and $\overline{S}$ inputs as shown by the truth table. The enable ($\overline{E}$) and master reset ($\overline{MR}$) inputs provide the added flexibility of cascading several of these latches for multi-bit storage in high-speed systems applications.

In the D-type latch operation, when the $\overline{E}$ and $\overline{S}$ inputs are in the "0" state and the $\overline{MR}$ input is in the "1" state, the data is processed thru and no information is stored. In this case the state of the outputs follows the D input. When $\overline{E}$ is switched to the "1" state while $\overline{MR}$ remains in the "1" state, the information present at the outputs is stored and is not affected by the state of the other inputs.

When operated in the set/reset mode, with $\overline{E}$ in the "0" state and $\overline{MR}$ in the "1" state, the output is reset if D is "0", or set if S is "0". In each latch the D and S signals are wire-ANDed together, thus if both D and $\overline{S}$ are "0", the D signal will prevail, and the output will reset. If both D and $\overline{S}$ are "1", or if the enable changes to the "1" state, the outputs will remain at the level stored prior to the change.

When $\overline{MR}$ is switched to the "0" state, all outputs will be forced into the "0" state for as long as $\overline{MR}$ stays low.

This device has input protection diodes, and active pull-up configurations at all outputs.



OPERATION	INPUT $\overline{MR}$	$\overline{E}$	$\overline{S}$	D	OUTPUT Q_n
D Mode	1	0	0	0	0
	1	0	0	1	1
	1	1	X	X	Q_{n-1}
R/S Mode	1	0	0	0	0
	1	0	0	1	1
	1	0	1	0	0
	1	0	1	1	Q_{n-1}
	1	1	X	X	Q_{n-1}
Device Reset	0	X	X	X	0

X = Don't care.

Input Loading Factor:
D Inputs = 1.5
All Other Inputs = 1

Output Loading Factor = 10

Total Power Dissipation = 200 mW typ/pkg

V_{CC} = Pin 16
Gnd = Pin 8

MC9316
MC8316

The MC9316/8316 hexadecimal counter consists of four J-K master-slave flip-flops plus additional gating to accomplish the counter function. Parallel inputs are provided for presetting data and parallel outputs for full counting flexibility.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of other input states. Parallel information may be preset only while the parallel enable ($\overline{PE}$) is in the logic "0" state.

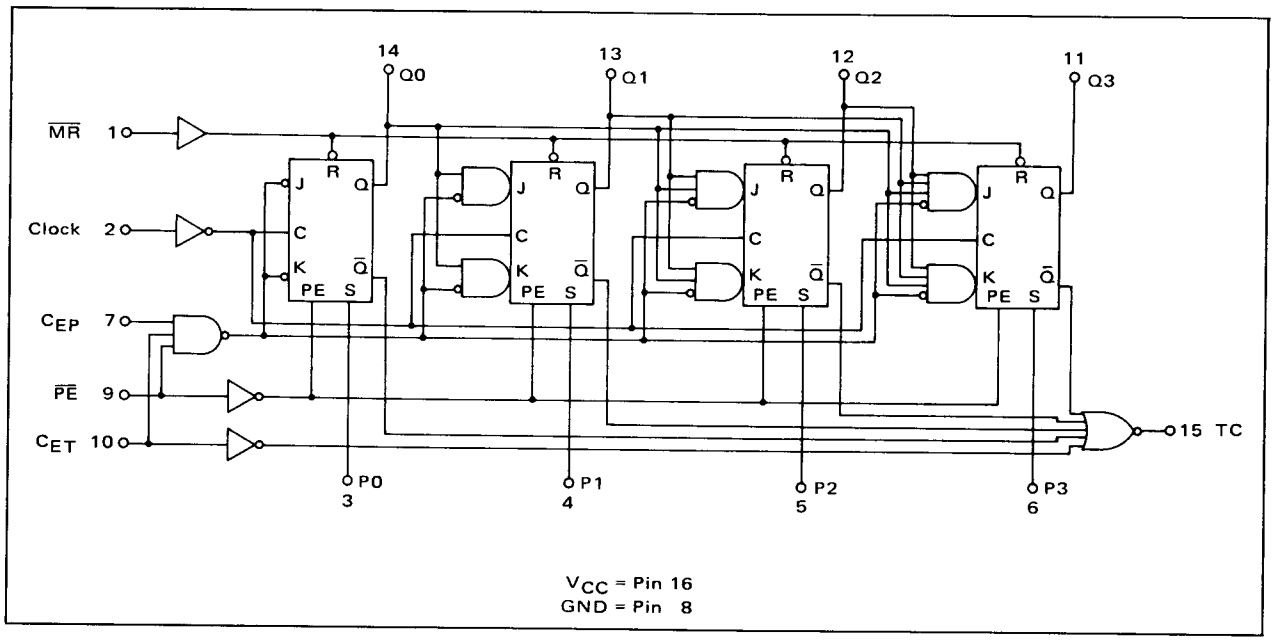
Inputs C_{EP} and C_{ET} and output TC are useful in cascading counters. TC provides an output pulse each time the counter reaches its maximum count.

COUNT SEQUENCE TRUTH TABLE

COUNT	OUTPUT Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Input Loading Factors:
$\overline{MR}$, C_{EP} = 1
Clock, $\overline{PE}$, C_{ET} = 2
P0, P1, P2, P3 = 2/3
Output Loading Factor = 6

Total Power Dissipation = 300 mW typ/pkg
Propagation Delay Time = 14 to 35 ns typ
Toggle Frequency = 28 MHz typ



V_{CC} = Pin 16
GND = Pin 8

SEVEN SEGMENT DECODER

MC9317
MC8317

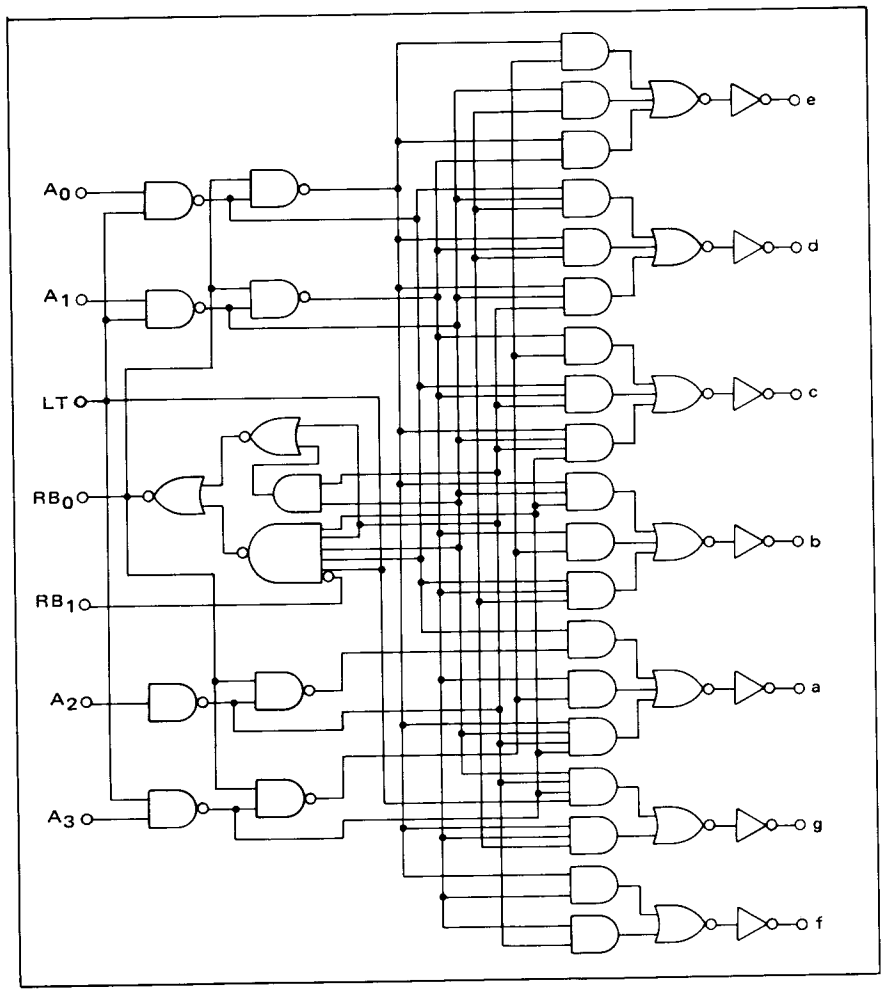


Figure 1
Segment Designation

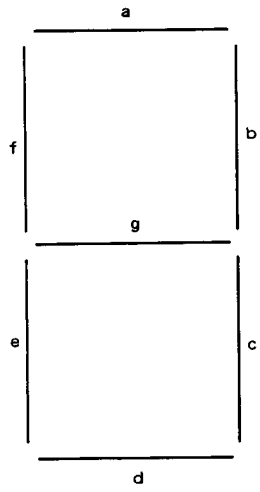
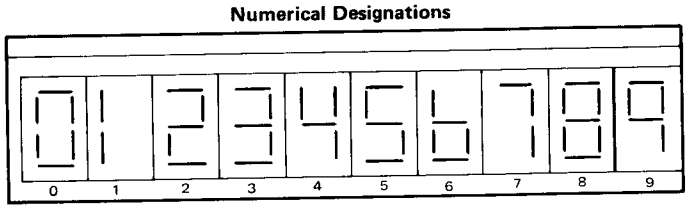


Figure 2
Truth Table

$\overline{LT}$	$\overline{RB1}$	A_0	A_1	A_2	A_3	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	$\overline{RB0}$	Decimal or Function
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	H	L	0
H	H	L	L	L	L	L	L	L	L	L	L	L	H	0
	X	H	L	L	L	H	H	H	H	L	L	H	H	1
		L	H	L	L	L	L	H	L	L	H	L	H	2
		H	H	L	L	L	L	L	L	H	H	L	H	3
		L	L	H	L	H	L	L	H	H	L	L	H	4
		H	L	H	L	L	H	L	L	H	L	L	H	5
		L	H	H	L	H	H	L	L	L	L	L	H	6
		H	H	H	L	L	L	L	H	H	H	H	H	7
		L	L	L	H	L	L	L	L	L	L	L	H	8
		H	L	L	H	L	L	L	H	H	L	L	H	9
		L	H	L	H	H	H	H	H	H	H	H	L	10
		H	H	L	H	H	H	H	H	H	H	H	L	11
		L	L	H	H	H	H	H	H	H	H	H	L	12
		H	L	H	H	H	H	H	H	H	H	H	L	13
		L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

Figure 3
Numerical Designations

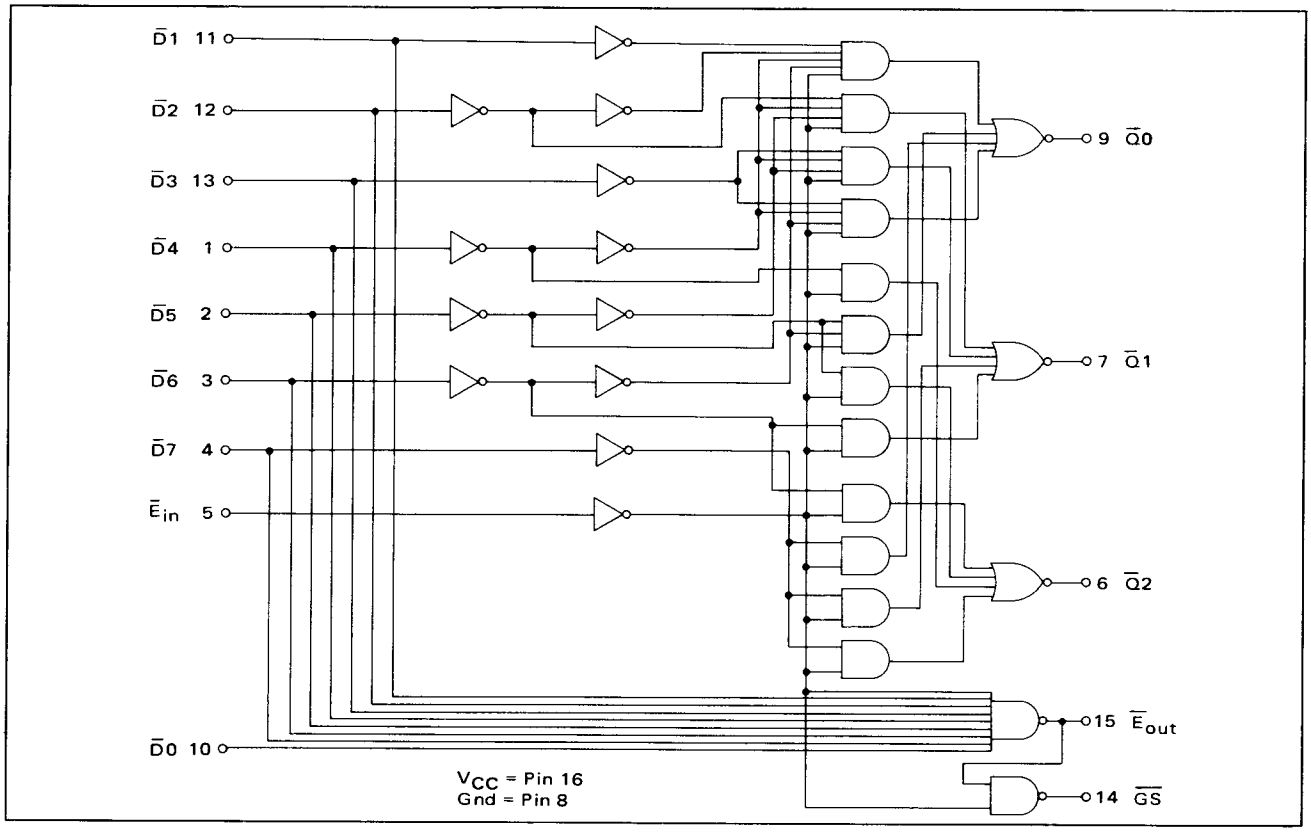


8-INPUT
PRIORITY ENCODER

MC9318
MC8318

Input Loading Factor:
$\overline{D}0 = 1$
All Other Inputs = 2
Output Loading Factor:
$\overline{E}_{out} = 5$
$\overline{GS} = 6$
$\overline{Q}0, \overline{Q}1, \overline{Q}2 = 10$
Total Power Dissipation = 225 mW typ/pkg

The MC9318/8318 is an eight-bit priority encoder which converts a one-of-eight code to a three-bit binary code in order of priority, with $\overline{D}7$ assigned the highest priority. All inputs and outputs are active in the low state. The $\overline{E}_{in}$ (input enable) forces all outputs high and overrides all the data inputs, allowing new data to settle on the inputs without affecting the outputs until the $\overline{E}_{in}$ is switched low. The $\overline{GS}$ (group signal) is low when any input is low. The $\overline{E}_{out}$ is low only when all inputs are high. The $\overline{E}_{out}$, when used in conjunction with the $\overline{E}_{in}$ is cascaded encoders, provides priority encoding of N input signals.

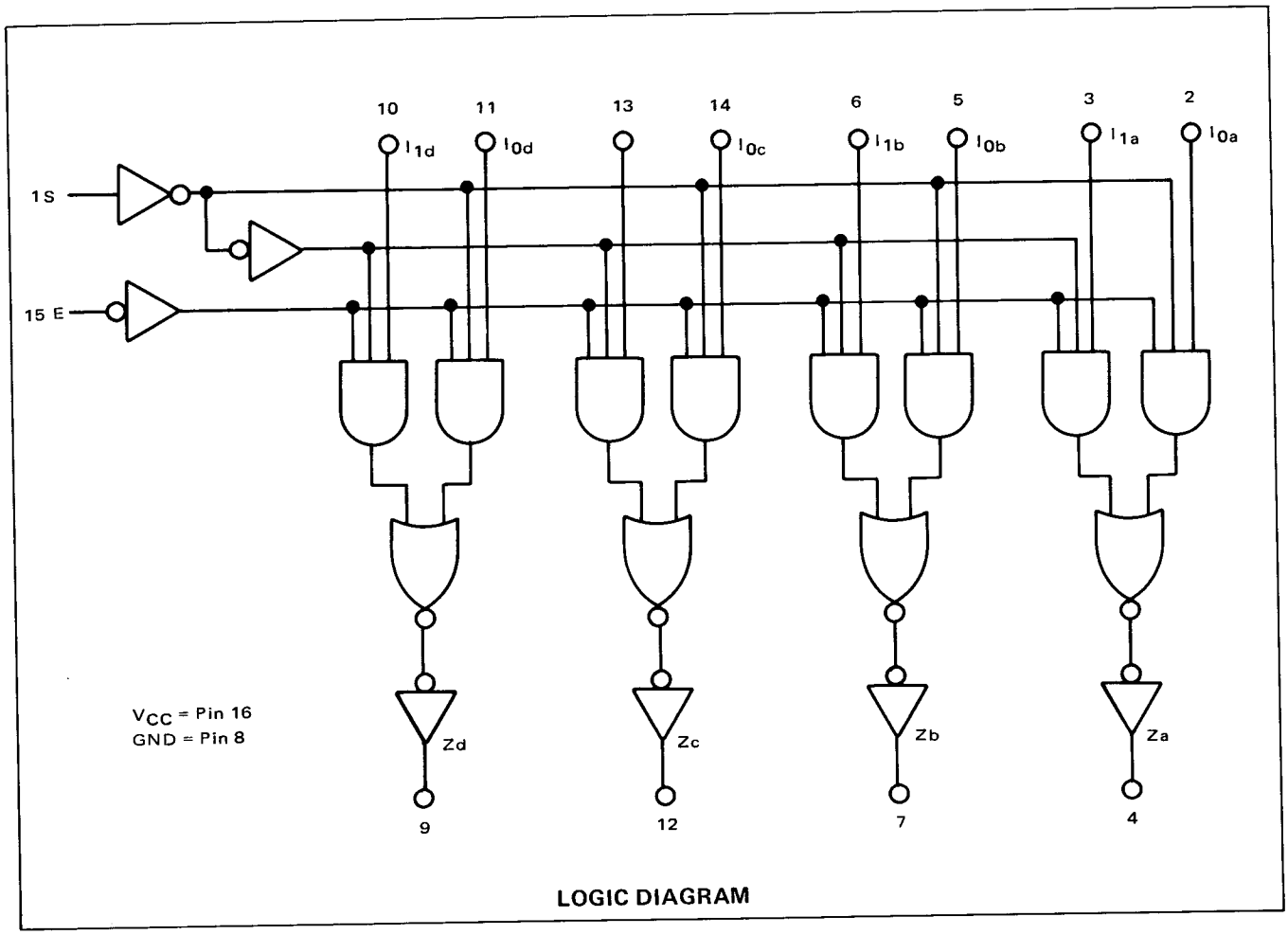


INPUT									OUTPUT				
$\overline{E}_{in}$	$\overline{D}7$	$\overline{D}6$	$\overline{D}5$	$\overline{D}4$	$\overline{D}3$	$\overline{D}2$	$\overline{D}1$	$\overline{D}0$	$\overline{GS}$	$\overline{Q}2$	$\overline{Q}1$	$\overline{Q}0$	$\overline{E}_{out}$
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	X	X	X	X	X	X	X	0	0	0	0	1
0	1	0	X	X	X	X	X	X	0	0	0	1	1
0	1	1	0	X	X	X	X	X	0	0	1	0	1
0	1	1	1	0	X	X	X	X	0	0	1	1	1
0	1	1	1	1	0	X	X	X	0	1	0	0	1
0	1	1	1	1	1	0	X	X	0	1	0	1	1
0	1	1	1	1	1	1	0	X	0	1	1	0	1
0	1	1	1	1	1	1	1	0	0	1	1	1	1

X = Don't Care

MC9322
MC8322

DESCRIPTION — The MC9322/8322 is a Monolithic, High Speed, Quad Two-Input Digital Multiplexer Circuit. It consists of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output. The circuit uses TTL for high speed, high fan out operation and is compatible with all other members of the Motorola TTL family.



LOGIC DIAGRAM

TRUTH TABLE

Enable	Select Input	Inputs		Output
E	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Logic Level

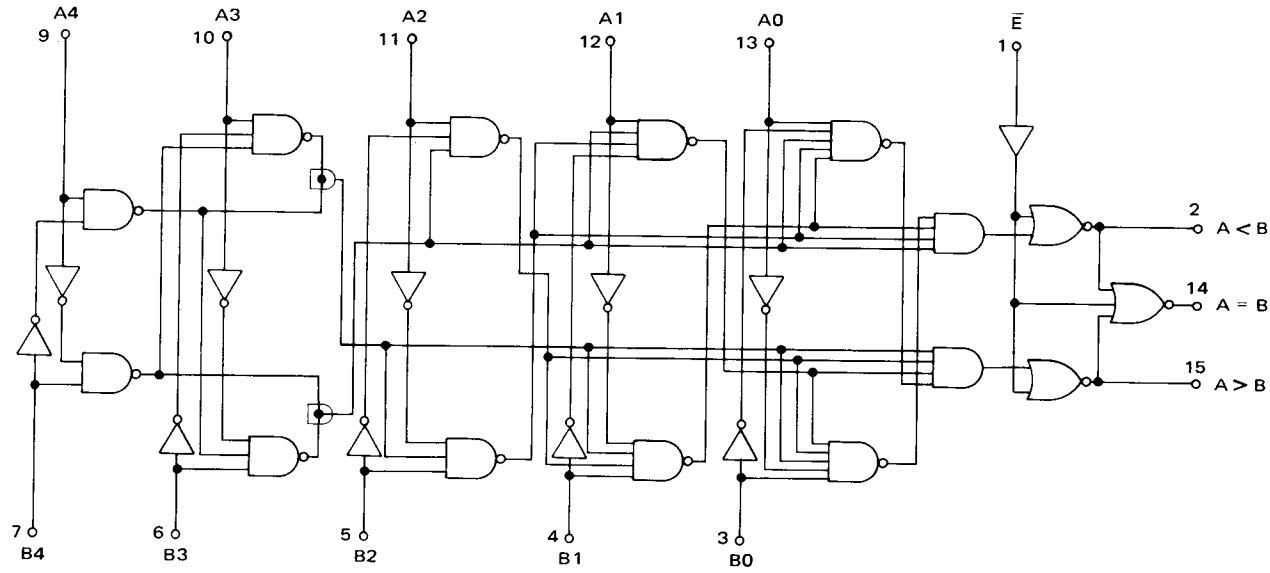
MC9324
MC8324

The MC9324/8324 compares two 5-bit binary words, A and B. The outputs indicate the three possible relations between A and B: A < B, A = B, and A > B.

Outputs for the conditions A < B and A > B are generated in only three gate delays. For detecting A = B, one NOR gate is used at those two outputs to sense "A not greater and not less than B". All three outputs may be activated by the active-low Enable input, $\overline{E}$.

This 5-bit comparator may be expanded for use with larger words. To do that, the A > B and A < B outputs of one device are tied to an A and a B input (respectively) on another comparator.

It should be noted that the A4 and B4 inputs are the most significant inputs, and A0 and B0 the least significant. Thus if A4 is high and B4 is low, the A > B output will be high regardless of the state of any other inputs (except $\overline{E}$).



V_{CC} = Pin 16
Gnd = Pin 8

INPUT			OUTPUT		
$\overline{E}$	A_n	B_n	A < B	A > B	A = B
1	X	X	0	0	0
0	Word A = Word B		0	0	1
0	Word A > Word B		0	1	0
0	Word A < Word B		1	0	0

X = Don't Care

Input Loading Factor = 2
Output Loading Factor = 10
Total Power Dissipation = 220 mW typ/pkg

DUAL 8-BIT SHIFT REGISTER

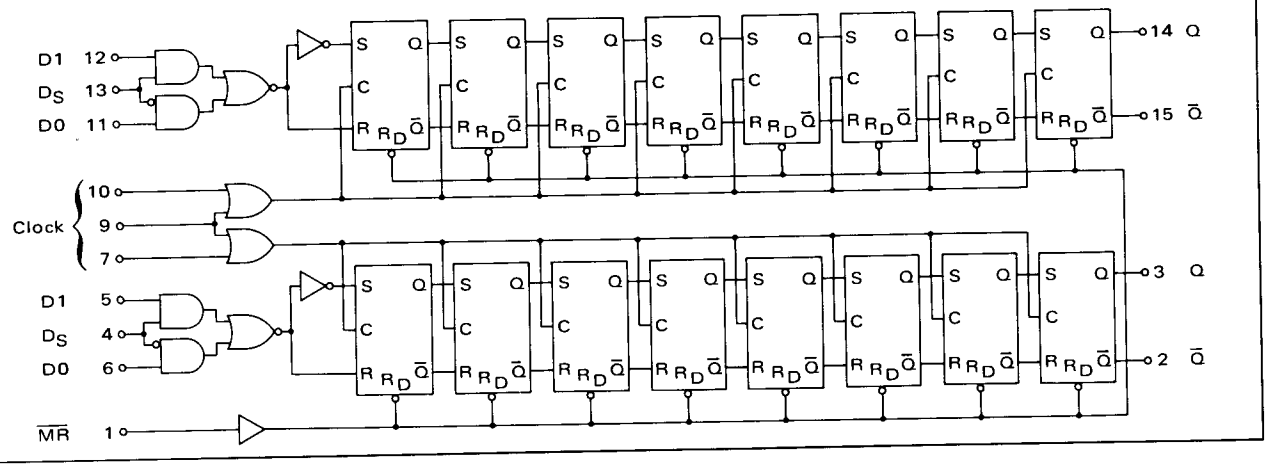
MC9328
MC8328

Input Loading Factors:
$\overline{MR}$, D0, D1 = 1
D_S = 2
Clock — Pins 7, 10 = 1.5
Pin 9 = 3
Output Loading Factor = 6

Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time = :
Clock to Output, t_{pd-} = 22 ns typ
t_{pd+} = 13 ns typ
$\overline{MR}$ to Output, t_{pd-} or t_{pd+} = 35 ns typ

V_{CC} = Pin 16
GND = Pin 8

The MC9328/8328 is a monolithic dual 8-bit serial shift register. Each 8-bit register is provided with a 2-input multiplexer circuit and complementary serial outputs. The two registers can be clocked together with a common line, or clocked separately with separate lines. A common $\overline{\text{Master Reset}}$ input is active in the low level and overrides all other inputs.

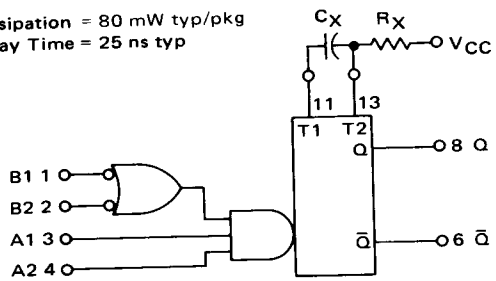


RETRIGGERABLE
MONOSTABLE
MULTIVIBRATOR

MC9601F
MC8601F

Input Loading Factor = 1
Output Loading Factor:
MC9601 = 6
MC8601 = 8
Total Power Dissipation = 80 mW typ/pkg
Propagation Delay Time = 25 ns typ

V_{CC} = Pin 14
GND = Pin 7



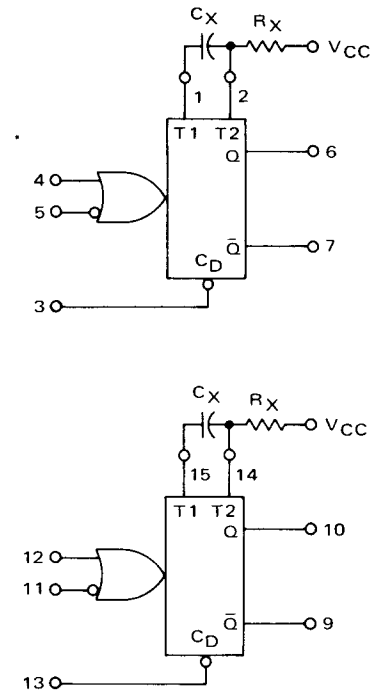
The MC9601/8601 monostable multivibrator may be triggered from either edge of an input pulse and will produce accurate output pulse over a wide range of widths. The duration and accuracy of the complementary output pulses are determined by the external timing components, R_X and C_X. Each time the input conditions for triggering are met the external timing capacitor, C_X, is discharged, starting a new output pulse. The output goes to the high state while C_X is being discharged and remains there until the capacitor recharges through R_X, to a threshold determined by an internal comparator. Input pulses applied during the active state again discharge the capacitor, thus adding another full timing cycle to the output pulse width. This retriggering feature can be inhibited if not required.

DUAL RETRIGGERABLE
RESETTABLE
MONOSTABLE
MULTIVIBRATOR

MC9602
MC8602

Add Suffix F for TO-86 ceramic flat package (Case 607).
Suffix L for TO-116 ceramic dual in-line package (Case 632).
Suffix P for TO-116 plastic dual in-line package (Case 646) MC8602 only.

The MC9602/8602 monostable multivibrator may be triggered from either edge of an input pulse and will produce accurate output pulse over a wide range of widths. The duration and accuracy of the complementary output pulses are determined by the external timing components, R_X and C_X. Each time the input conditions for triggering are met the external timing capacitor, C_X, is discharged, starting a new output pulse. The output goes to the high state while C_X is being discharged and remains there until the capacitor recharges through R_X, to a threshold determined by an internal comparator. Input pulses applied during the active state again discharge the capacitor, thus adding another full timing cycle to the output pulse width. This retriggering feature can be inhibited if not required.



V_{CC} = Pin 16
Gnd = Pin 8

Input Loading Factor = 1
Output Loading Factor:
MC9602 = 6
MC8602 = 8
Total Power Dissipation = 160 mW typ/pkg
Propagation Delay Time = 25 ns typ

For $C_X > 1000$ pF

$$PW = 0.35\, R_X\, C_X \left(1 + \frac{0.85}{R_X}\right)$$

For $C_X < 1000$ pF see Figure 1