

# HD404710 Series

## Description

The HD404710 Series 4-bit single-chip microcomputers incorporate five timers, two serial interfaces, an A/D converter, an input capture timer, and an output compare timer. They also include a 32.768-kHz oscillator and low-power dissipation modes. The HD404710 and HD4074710 are modifications of the HD404719 and HD4074719, respectively, by the addition of pattern ROM.

The HD404710 is a mask ROM version. The HD4074710 is a PROM version (ZTAT™ microcomputer with 27256 compatibility).

## Features

- 16,384-word × 10-bit program ROM (HD404719, HD404710)
- 16,384-word × 10-bit program PROM (HD4074719, HD4074710)
- 8,192-word × 10-bit pattern ROM (HD404710)
- 8,192-word × 10-bit pattern PROM (HD4074710)
- 960-digit × 4-bit RAM
- 70 I/O pins including 36 high-voltage, high-current pins (15 mA, max.)
- Five timer/counters
- Two 8-bit clock-synchronous serial interfaces
- 8-channel × 8-bit A/D converter
- Voltage comparator (with one input channel)
- 2-channel × 8-bit input capture timer
- 16-bit output compare timer
- Eight-level buzzer output line
- 14 interrupt sources
  - Six by external sources, including three edge-programmable type sources
  - Eight by internal sources
- Subroutine stack up to 16 levels, including interrupts
- Four low-power dissipation modes
  - Subactive mode
  - Standby mode
  - Watch mode
  - Stop mode
- Built-in oscillator
  - Crystal or ceramic oscillator (an external clock also possible) as main clock
  - 32.768-kHz crystal subclock
- Instruction cycle time: 0.89 μs to 1.78 μs

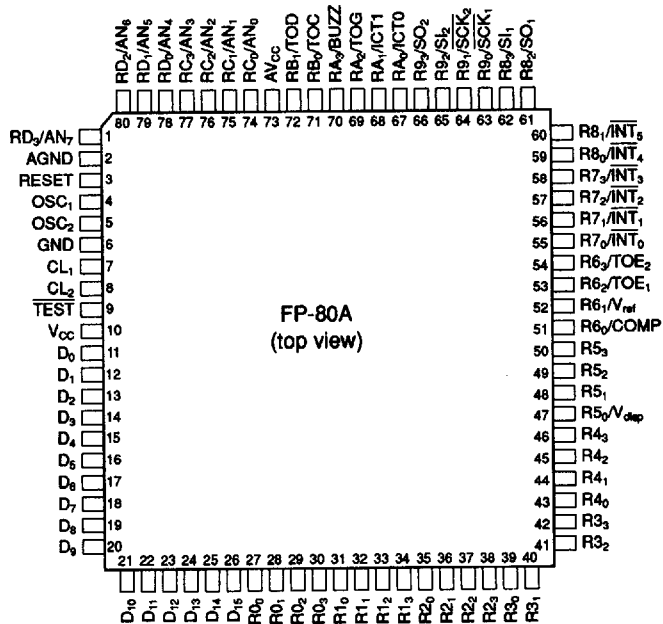
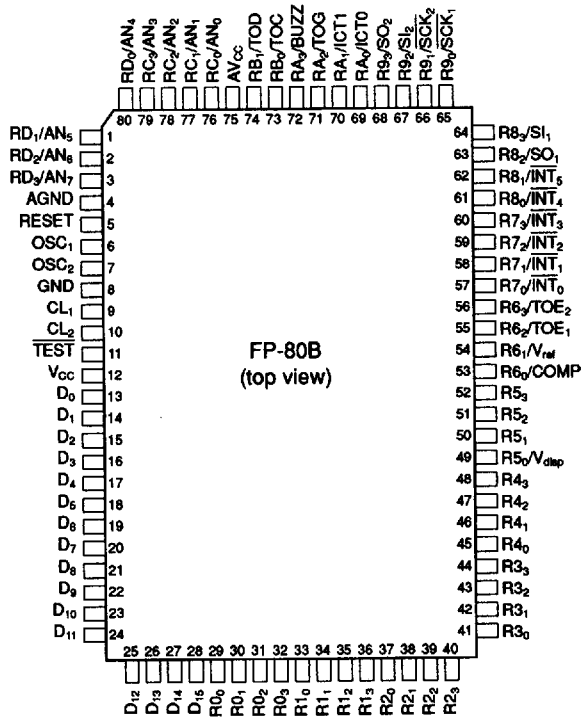
## Ordering Information

Type	Product Name	Model Name	Program ROM (Words)	Pattern ROM (Words)	Package
Mask ROM	HD404719	HD404719FS	16,384	—	FP-80B
		HD404719H		—	FP-80A
	HD404710	HD404710FS	8,192	FP-80B	
ZTAT™	HD4074719	HD4074719FS	16,384	—	FP-80B
		HD4074719H		—	FP-80A
	HD4074710	HD4074710FS	8,192	FP-80B	

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# HD404710 Series

## Pin Arrangement



Pin Description

Pin Number		Pin Name	Input/ Output	Pin Number		Pin Name	Input/ Output
FP-80B	FP-80A			FP-80B	FP-80A		
1	79	RD <sub>1</sub> /AN <sub>5</sub>	I	34	32	R1 <sub>1</sub>	I/O
2	80	RD <sub>2</sub> /AN <sub>6</sub>	I	35	33	R1 <sub>2</sub>	I/O
3	1	RD <sub>3</sub> /AN <sub>7</sub>	I	36	34	R1 <sub>3</sub>	I/O
4	2	AGND		37	35	R2 <sub>0</sub>	I/O
5	3	RESET	I	38	36	R2 <sub>1</sub>	I/O
6	4	OSC <sub>1</sub>	I	39	37	R2 <sub>2</sub>	I/O
7	5	OSC <sub>2</sub>	O	40	38	R2 <sub>3</sub>	I/O
8	6	GND		41	39	R3 <sub>0</sub>	I/O
9	7	CL <sub>1</sub>	I	42	40	R3 <sub>1</sub>	I/O
10	8	CL <sub>2</sub>	O	43	41	R3 <sub>2</sub>	I/O
11	9	TEST	I	44	42	R3 <sub>3</sub>	I/O
12	10	V <sub>CC</sub>		45	43	R4 <sub>0</sub>	I/O
13	11	D <sub>0</sub>	I/O	46	44	R4 <sub>1</sub>	I/O
14	12	D <sub>1</sub>	I/O	47	45	R4 <sub>2</sub>	I/O
15	13	D <sub>2</sub>	I/O	48	46	R4 <sub>3</sub>	I/O
16	14	D <sub>3</sub>	I/O	49	47	R5 <sub>0</sub> /V <sub>disp</sub>	I
17	15	D <sub>4</sub>	I/O	50	48	R5 <sub>1</sub>	I
18	16	D <sub>5</sub>	I/O	51	49	R5 <sub>2</sub>	I
19	17	D <sub>6</sub>	I/O	52	50	R5 <sub>3</sub>	I
20	18	D <sub>7</sub>	I/O	53	51	R6 <sub>0</sub> /COMP	I/O
21	19	D <sub>8</sub>	I/O	54	52	R6 <sub>1</sub> /V <sub>ref</sub>	I/O
22	20	D <sub>9</sub>	I/O	55	53	R6 <sub>2</sub> /TOE <sub>1</sub>	I/O
23	21	D <sub>10</sub>	I/O	56	54	R6 <sub>3</sub> /TOE <sub>2</sub>	I/O
24	22	D <sub>11</sub>	I/O	57	55	R7 <sub>0</sub> /INT <sub>0</sub>	I/O
25	23	D <sub>12</sub>	I/O	58	56	R7 <sub>1</sub> /INT <sub>1</sub>	I/O
26	24	D <sub>13</sub>	I/O	59	57	R7 <sub>2</sub> /INT <sub>2</sub>	I/O
27	25	D <sub>14</sub>	I/O	60	58	R7 <sub>3</sub> /INT <sub>3</sub>	I/O
28	26	D <sub>15</sub>	I/O	61	59	R8 <sub>0</sub> /INT <sub>4</sub>	I/O
29	27	R0 <sub>0</sub>	I/O	62	60	R8 <sub>1</sub> /INT <sub>5</sub>	I/O
30	28	R0 <sub>1</sub>	I/O	63	61	R8 <sub>2</sub> /SO <sub>1</sub>	I/O
31	29	R0 <sub>2</sub>	I/O	64	62	R8 <sub>3</sub> /SI <sub>1</sub>	I/O
32	30	R0 <sub>3</sub>	I/O	65	63	R9 <sub>0</sub> /SCK <sub>1</sub>	I/O
33	31	R1 <sub>0</sub>	I/O	66	64	R9 <sub>1</sub> /SCK <sub>2</sub>	I/O

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### Pin Description (cont)

Pin Number		Pin Name	Input/ Output	Pin Number		Pin Name	Input/ Output
FP-80B	FP-80A			FP-80B	FP-80A		
67	65	R9 <sub>2</sub> /SI <sub>2</sub>	I/O	74	72	RB <sub>1</sub> /TOD	I/O
68	66	R9 <sub>3</sub> /SO <sub>2</sub>	I/O	75	73	AV <sub>CC</sub>	
69	67	RA <sub>0</sub> /ICT <sub>0</sub>	I/O	76	74	RC <sub>0</sub> /AN <sub>0</sub>	I
70	68	RA <sub>1</sub> /ICT <sub>1</sub>	I/O	77	75	RC <sub>1</sub> /AN <sub>1</sub>	I
71	69	RA <sub>2</sub> /TOG	I/O	78	76	RC <sub>2</sub> /AN <sub>2</sub>	I
72	70	RA <sub>3</sub> /BUZZ	I/O	79	77	RC <sub>3</sub> /AN <sub>3</sub>	I
73	71	RB <sub>0</sub> /TOC	I/O	80	78	RD <sub>0</sub> /AN <sub>4</sub>	I

## Pin Functions

### Power Supply

**V<sub>CC</sub>**: Apply power voltage to this pin.

**GND**: Connect to ground.

**TEST**: Used for test purposes only. Connect it to V<sub>CC</sub>.

**RESET**: Resets the MCU.

### Oscillators

**OSC<sub>1</sub>, OSC<sub>2</sub>**: Used as pins for the internal oscillator circuit. They can be connected to a crystal resonator or a ceramic resonator, or OSC<sub>1</sub> can be connected to an external oscillator circuit.

**CL<sub>1</sub>, CL<sub>2</sub>**: Used for a 32.768-kHz crystal oscillator that acts as a clock.

### Ports

**D<sub>0</sub>-D<sub>15</sub> (D Port)**: Input/output port addressable by individual bits. Each port output consists of an open-drain PMOS which enables high-voltage, high-current drive ability for its pin.

**R0-RD (R Ports)**: Input/output ports addressable in 4-bit units. R5, RC, and RD are input-only ports. The R5 to RD port pins are standard pins, but the R0 to R4 pins are high-voltage pins. Each of the R0 to R4 output pins consists of an open-drain PMOS which enables high-voltage drive ability for its pin. Port pins R7<sub>0</sub> to R7<sub>3</sub> and R6<sub>0</sub> to R6<sub>3</sub> are multiplexed with peripheral pins.

### Interrupts

**INT<sub>0</sub>-INT<sub>5</sub>**: Input external interrupts to the MCU. INT<sub>0</sub> to INT<sub>5</sub> are multiplexed with R7<sub>0</sub> to R7<sub>3</sub> and R8<sub>0</sub> to R8<sub>1</sub>, respectively.

### Serial Interface

**SCK<sub>1</sub>, SCK<sub>2</sub>**: Input/output serial interface clock pins that are multiplexed with pins R9<sub>0</sub> and R9<sub>1</sub>, respectively.

**SI<sub>1</sub>, SI<sub>2</sub>**: Serial interface receiving data input pins that are multiplexed with pins R8<sub>3</sub> and R9<sub>2</sub>, respectively.

**SO<sub>1</sub>, SO<sub>2</sub>**: Serial interface transmission data output pins that are multiplexed with pins R8<sub>2</sub> and R9<sub>3</sub>, respectively.

### Timers

**TOC, TOD**: Output variable-duty square waves. They are multiplexed with pins RB<sub>0</sub> and RB<sub>1</sub>, respectively.

**TOE<sub>1</sub>, TOE<sub>2</sub>**: Output square waves from the PWM. They are multiplexed with pins R6<sub>2</sub> and R6<sub>3</sub>, respectively.

**TOG**: Outputs a square wave specified by the output compare function. It is multiplexed with pin RA<sub>2</sub>.

### Buzzer

**Buzz**: Outputs a variable-duty square wave. It is multiplexed with RA<sub>3</sub>.

### A/D Converter

**AV<sub>CC</sub>**: V<sub>CC</sub> power supply for the A/D converter.

**AGND**: GND ground for the A/D converter.

**AN<sub>0</sub>-AN<sub>7</sub>**: Analog data input pins for A/D conversion that are multiplexed with pins RC<sub>0</sub> to RC<sub>3</sub> and RD<sub>0</sub> to RD<sub>3</sub>, respectively.

### Comparator

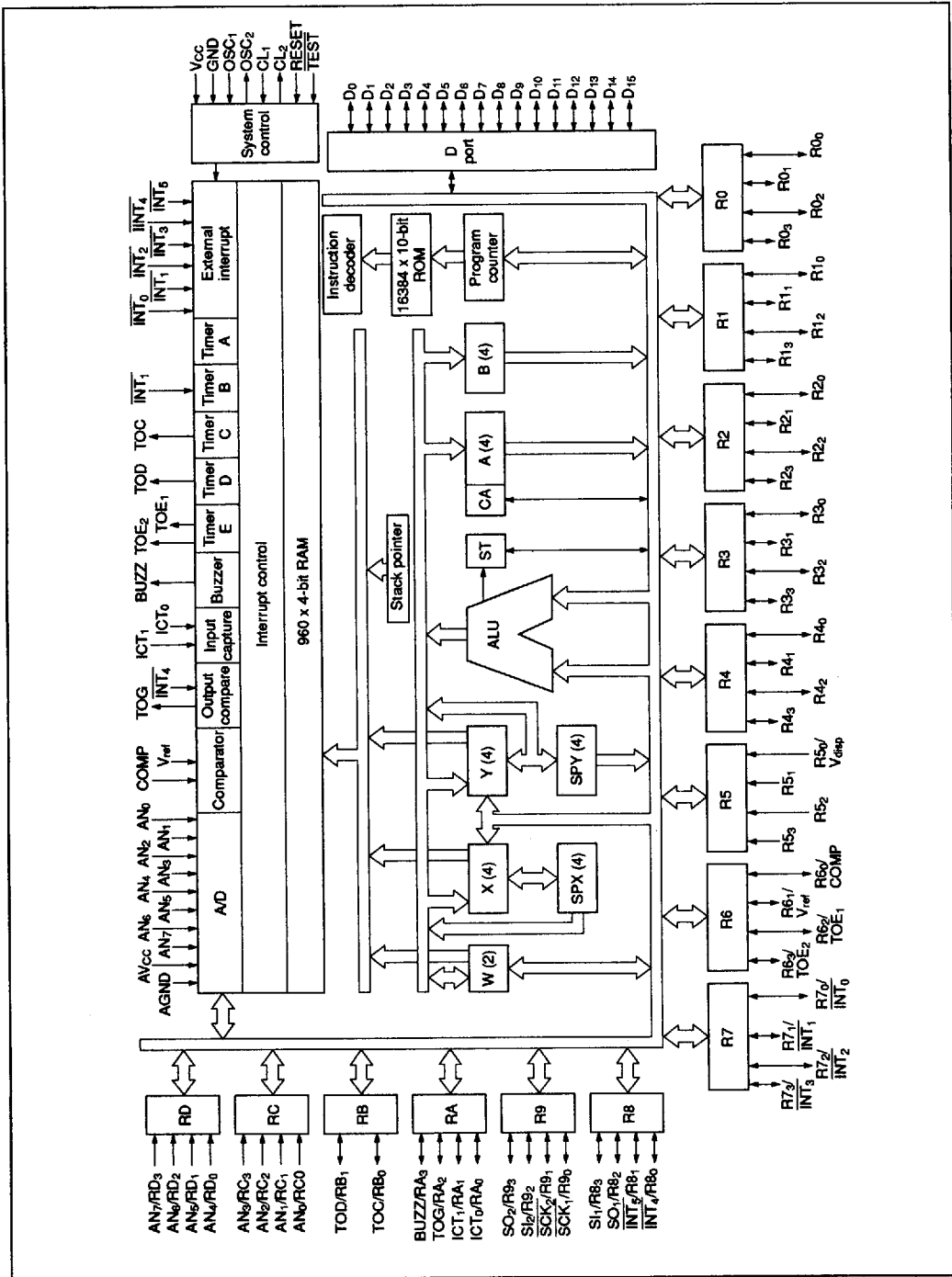
**COMP**: Input pin for the comparator. It is multiplexed with pin R6<sub>0</sub>.

**V<sub>ref</sub>**: Inputs reference voltage for the analog comparator. It is multiplexed with pin R6<sub>1</sub>.

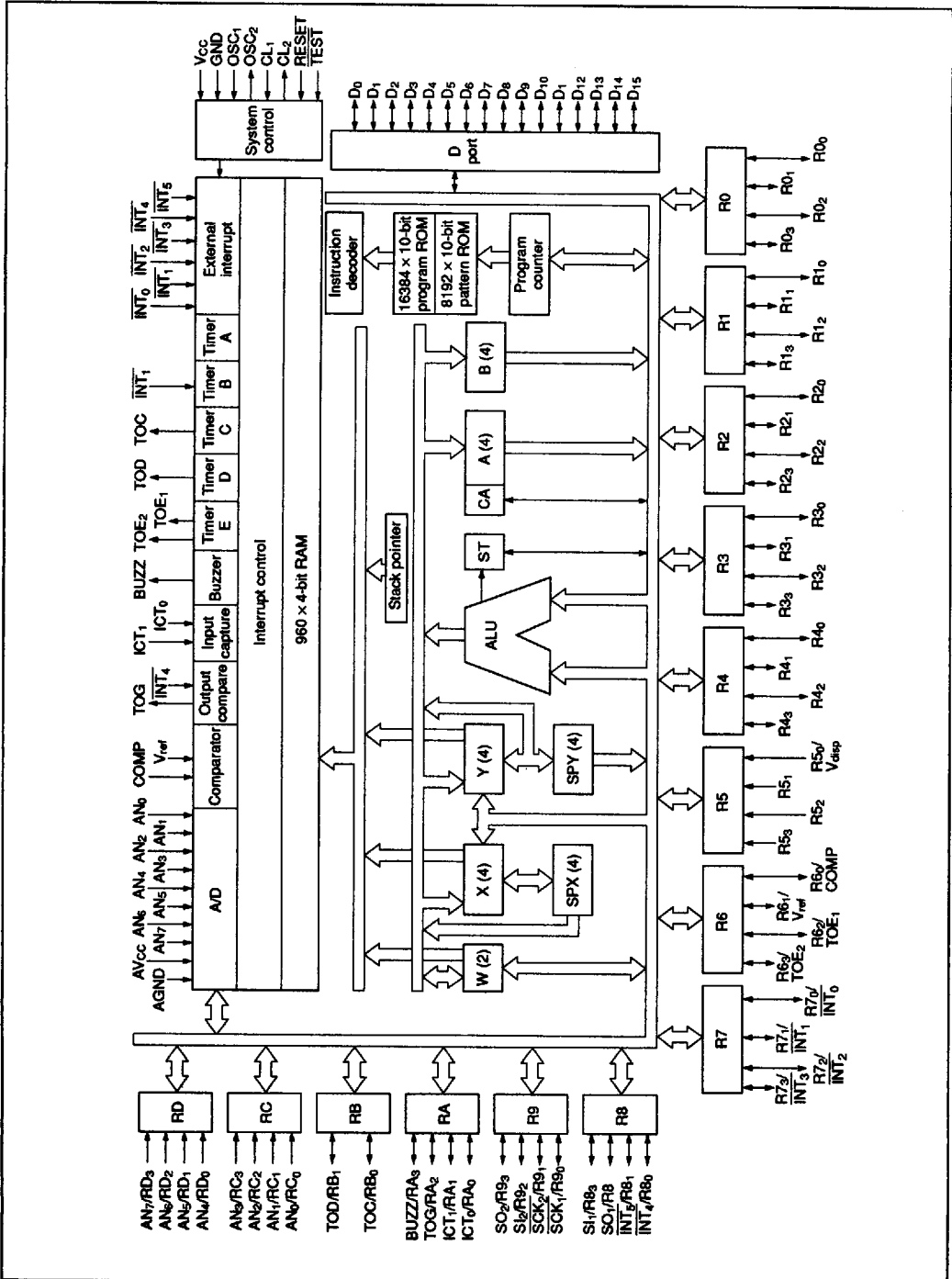
# HD404710 Series

## Block Diagram

### 1. HD404719, HD404719



2. HD404710, HD4074710



# HD404710 Series

## Memory Map

### Program ROM Memory Map

The program ROM memory map is shown in figure 1, and the ROM is described in detail below.

**Vector Address Area (\$0000–\$001F):** Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt execution, the program starts from the vector address.

**Zero-Page Subroutine Area (\$0000–\$003F):** Reserved for subroutines. The program branches to the subroutine in this area in response to the CAL instruction.

### Pattern Area (\$0000–\$0FFF):

- HD404719, HD404719: Reserved for ROM data that is referenced as a pattern by the P instruction.
- HD404710, HD404710: Reserved for ROM data that can be referenced as a pattern by the P instruction. The data in this area is available when bit 1 of the pattern bank register (PBNK) is 0.

**Program Area (\$0000–\$3FFF):** Used for program code.

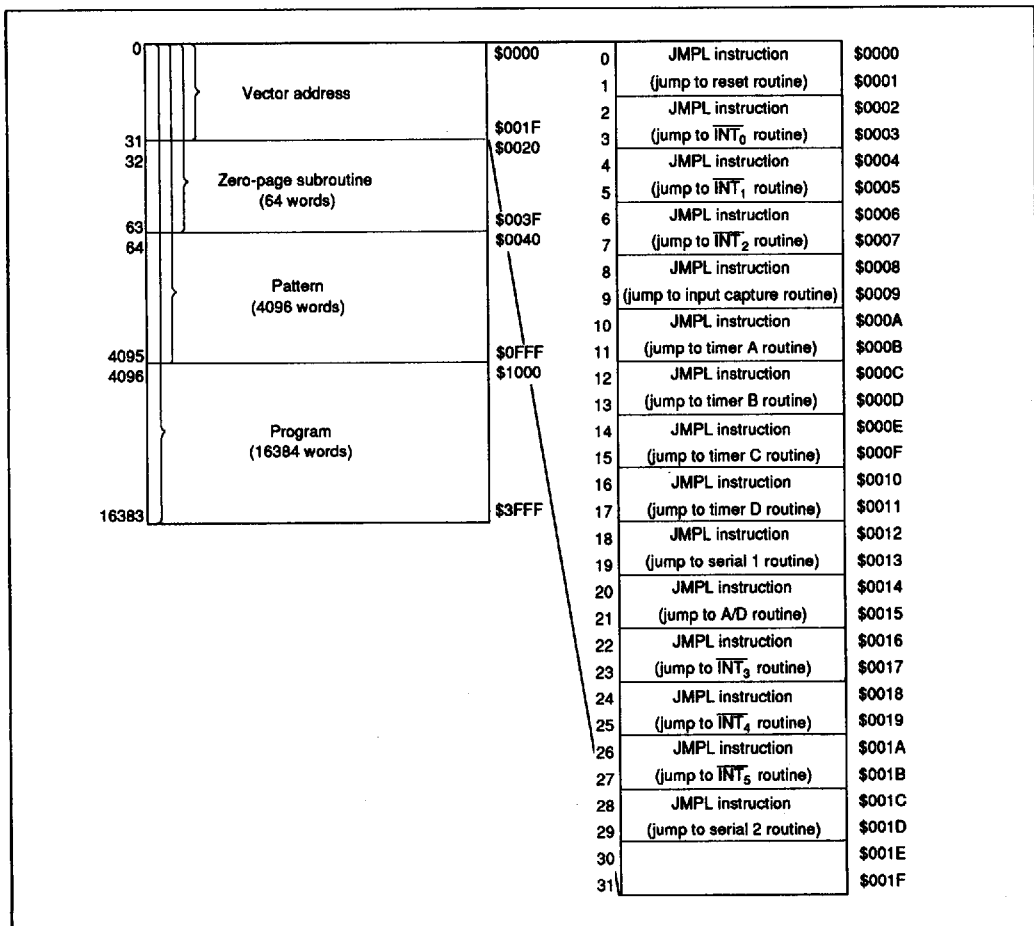


Figure 1 Program ROM Memory Map



**Pattern ROM Memory Map  
(HD404710, HD4074710)**

The pattern ROM memory map is shown in figure 2. The access conditions are shown in figures 3 to 5 and described below.

**8-kword Pattern Area (\$0000-\$1FFF):** Data in this area is accessed as the pattern data of the P instruction

instruction when bit 1 of the pattern ROM bank register (PBNK) is 1. When bit 0 of PBNK (PBNK0) is 0, area \$0000-\$0FFF is accessed, and when PBNK0 = 1, area \$1000-\$1FFF is accessed.

When PBNK1 = 0, data in the area limited to \$0000-\$0FFF in the 16-kword program area is accessed as the pattern data of the P instruction.

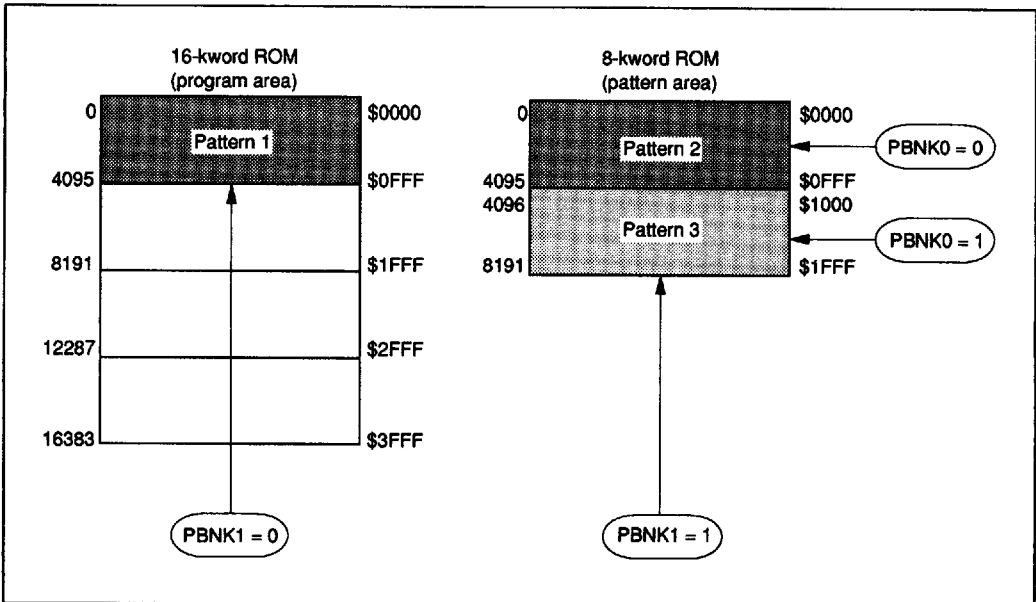


Figure 2 Pattern Reference Area of the P Instruction

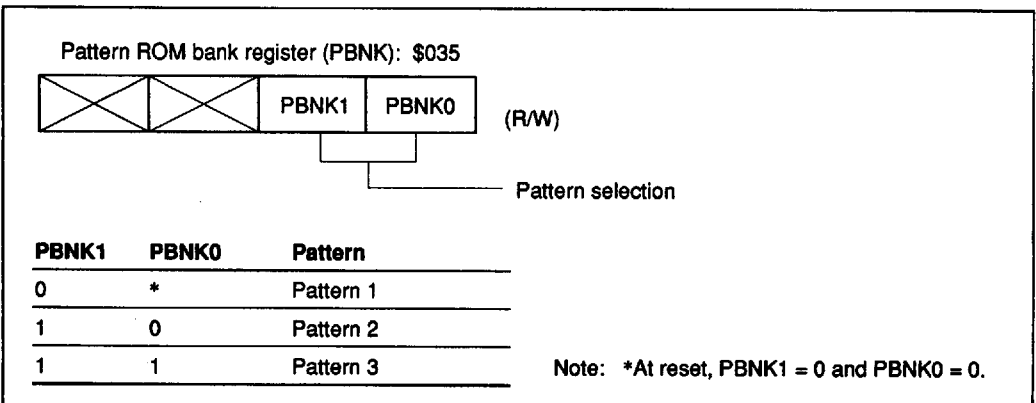


Figure 3 Pattern ROM Bank Register

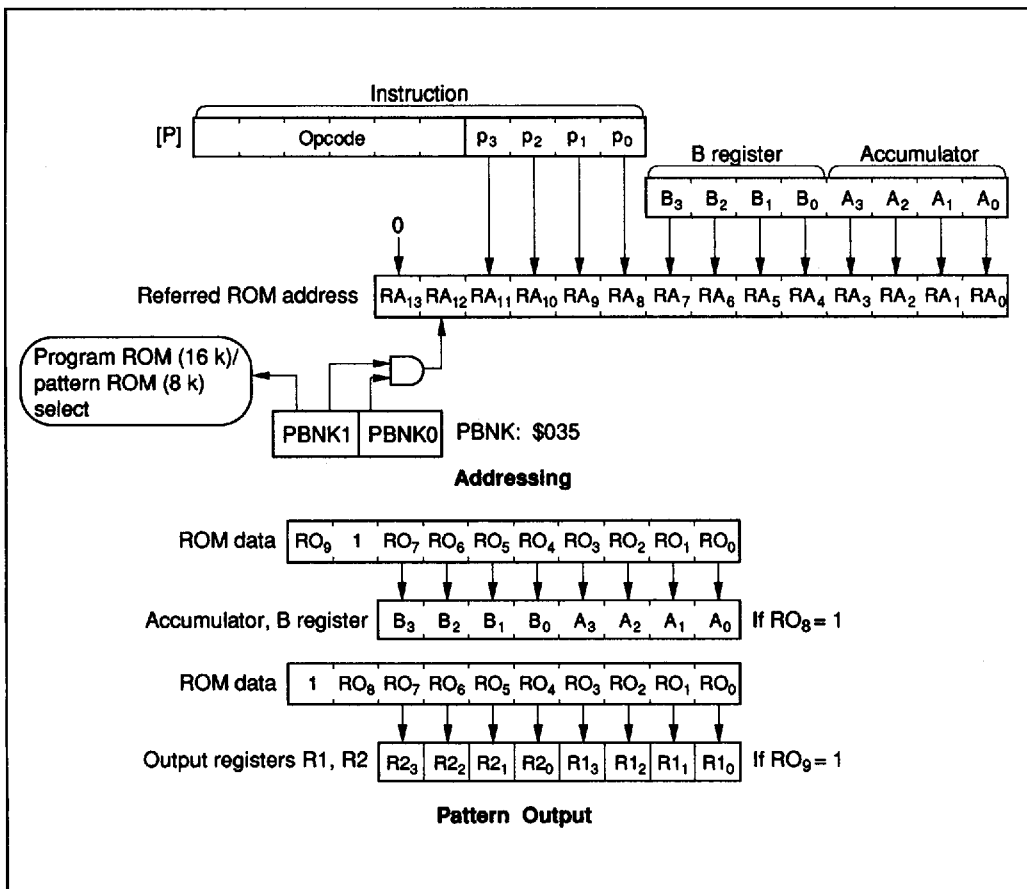
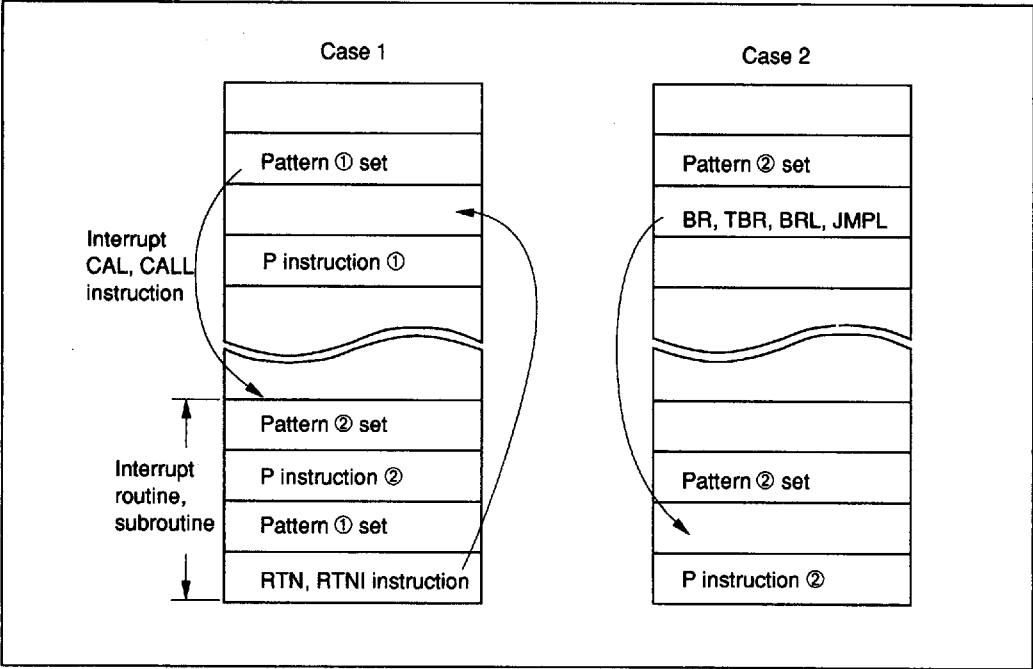


Figure 4 P (Pattern) Instruction

**Notes for Pattern ROM Bank Control:**

**Case 1:** When changing PBNK data during an interrupt routine or subroutine, the previous PBNK data must be stored in RAM and retrieved just before the RTN or RTNI instruction (figure 5).

**Case 2:** In some cases, the PBNK set operation must be programmed just before the BR, TBR, BRL, or JMPL instruction (figure 5).



**Figure 5 Pattern ROM Bank Control**

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## HD404710 Series

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### RAM Memory Map

The MCU contains a 960-digit × 4-bit RAM area for data and stack areas. In addition, interrupt control bits and special function registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figures 6-1 and 6-2, and the RAM area is described in detail below.

**Interrupt Control Bits Area (\$000–\$003, \$020–\$024):** Used for interrupt control (figure 7). It can be accessed only by RAM bit manipulation instructions. However, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer, the DTON, LSON, and WDON flags are accessed only by RAM bit manipulation instructions, and the WDON flag can only be set to 1 by the SEM and SEMD instructions.

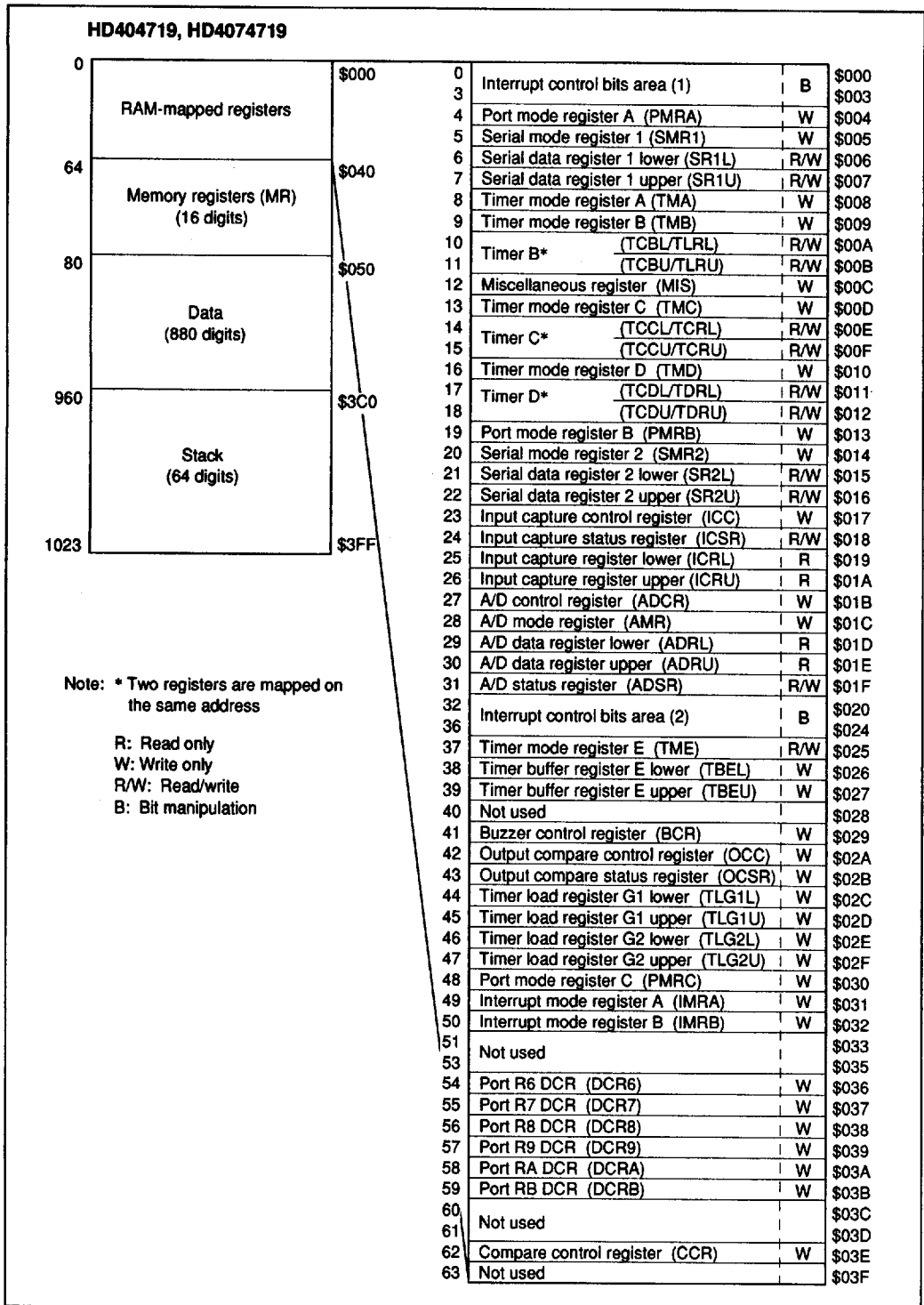
**Special Function Registers Area (\$004–\$01F, \$025–\$03F):** Used as mode registers for external interrupts, the serial interface, the timer/counters, and as data control registers and data registers for

I/O ports. As shown in figure 6, there are three types of registers: read-only, write-only, and read/write. These registers cannot be accessed by RAM bit manipulation instructions.

**Data Area (\$040–\$04F, \$050–\$3BF):** The memory registers (MRs), which are in 16 digits (\$040–\$04F), can also be accessed by the LAMR and XMRA instructions (figure 8).

**Stack Area (\$3C0–\$3FF):** Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and interrupt processing. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The stack area and data to be saved in it are shown in figure 8.

The program counter is popped from the stack by the RTN and RTNI instructions, but the status and carry flags can only be popped from the stack by the RTNI instruction. Any unused area is available for data storage.



**Figure 6-1 RAM Memory Map (HD404719, HD4074719)**

# HD404710 Series

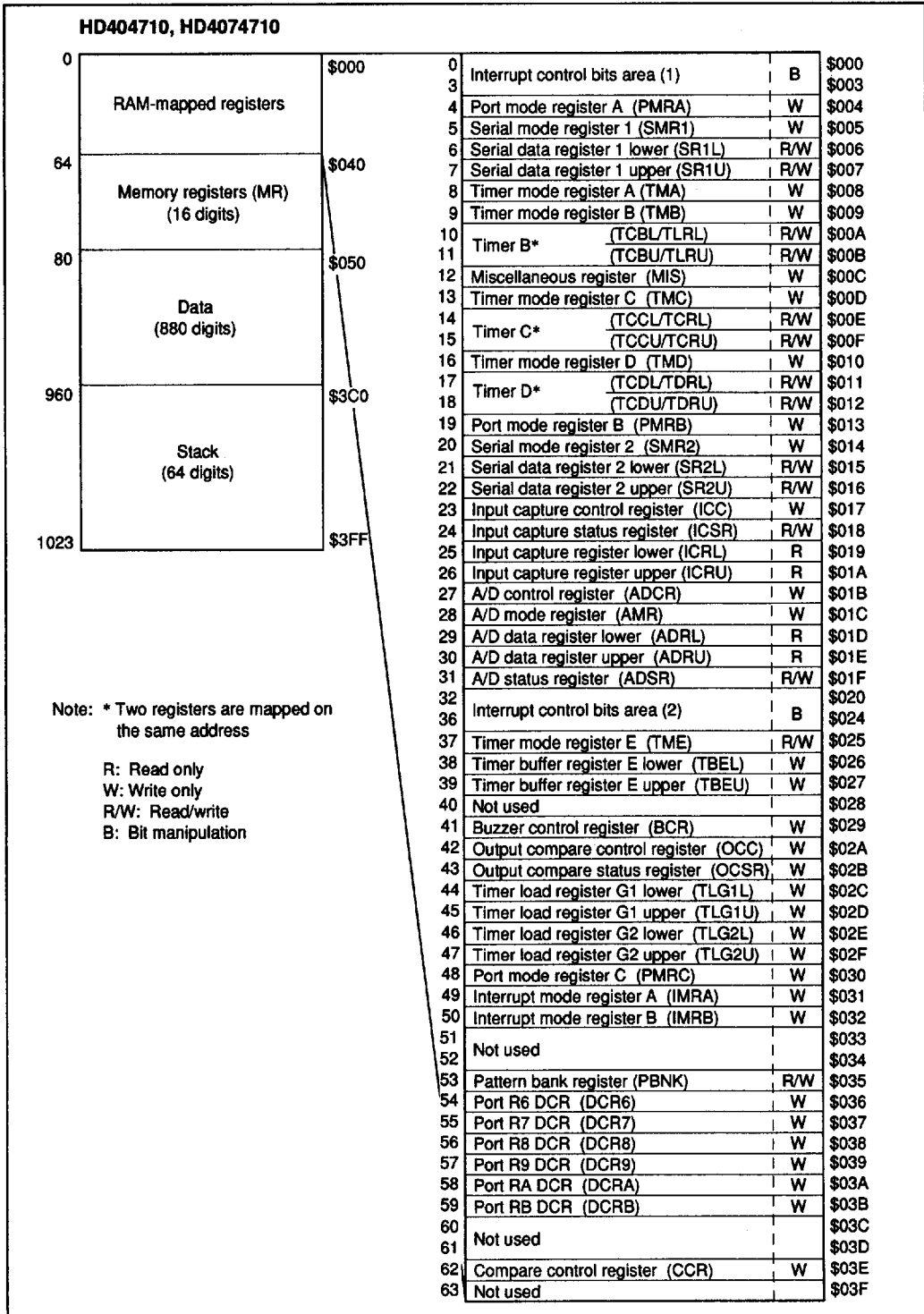


Figure 6-2 RAM Memory Map (HD404710, HD4074710)

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of INT <sub>0</sub> )	IF0 (IF of INT <sub>0</sub> )	RSP (Reset SP bit)	IE (Interrupt enable flag)	\$000
1	IM2 (IM of INT <sub>2</sub> )	IF2 (IF of INT <sub>2</sub> )	IM1 (IM of INT <sub>1</sub> )	IF1 (IF of INT <sub>1</sub> )	\$001
2	IMTA (IM of timer A)	IFTA (IF of timer A)	IMIC (IM of input capture)	IFIC (IF of input capture)	\$002
3	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	\$003
32	DTON (Direct transfer on flag)	Not used	WDON (Watchdog on flag)	LSON (Low speed on flag)	\$020
33	IMS1 (IM of serial 1)	IFS1 (IF of serial 1)	IMTD (IM of timer D)	IFTD (IF of timer D)	\$021
34	IM3 (IM of INT <sub>3</sub> )	IF3 (IF of INT <sub>3</sub> )	IMAD (IM of A/D)	IFAD (IF of A/D)	\$022
35	IM5 (IM of INT <sub>5</sub> )	IF5 (IF of INT <sub>5</sub> )	IM4 (IM of INT <sub>4</sub> )	IF4 (IF of INT <sub>4</sub> )	\$023
36	Not used	Not used	IMS2 (IM of serial 2)	IFS2 (IF of serial 2)	\$024

IF: Interrupt request flag  
 IM: Interrupt mask  
 IE: Interrupt enable flag  
 SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.  
 However, note that the IF cannot be set by the SEM or SEMD instruction. If the RSP bit or an unusable bit is tested by the TM or TMD instruction, its status is undefined.  
 The WDON flag can only be used by the SEM or SEMD instruction (it is reset only by MCU reset).

**Figure 7 Configuration of Interrupt Control Bits and Register Flag Areas**

Memory registers			Stack area			
64	MR (0)	\$040	960	Level 16	\$3C0	
65	MR (1)	\$041		Level 15		
66	MR (2)	\$042		Level 14		
67	MR (3)	\$043		Level 13		
68	MR (4)	\$044		Level 12		
69	MR (5)	\$045		Level 11		
70	MR (6)	\$046		Level 10		
71	MR (7)	\$047		Level 9		
72	MR (8)	\$048		Level 8		
73	MR (9)	\$049		Level 7		
74	MR (10)	\$04A		Level 6		
75	MR (11)	\$04B		Level 5		
76	MR (12)	\$04C		Level 4		
77	MR (13)	\$04D		Level 3		
78	MR (14)	\$04E		Level 2		
79	MR (15)	\$04F	1023	Level 1	\$3FF	

	Bit 3	Bit 2	Bit 1	Bit 0	
1020	ST	$\overline{PC}_{13}$	$\overline{PC}_{12}$	$\overline{PC}_{11}$	\$3FC
1021	$\overline{PC}_{10}$	$\overline{PC}_9$	$\overline{PC}_8$	$\overline{PC}_7$	\$3FD
1022	CA	$\overline{PC}_6$	$\overline{PC}_5$	$\overline{PC}_4$	\$3FE
1023	$\overline{PC}_3$	$\overline{PC}_2$	$\overline{PC}_1$	$\overline{PC}_0$	\$3FF

PC<sub>13</sub>–PC<sub>0</sub>: Program counter  
 ST: Status flag  
 CA: Carry flag

**Figure 8 Configuration of Memory Register and Stack Areas, and Stack Position**

# HD404710 Series

## Functional Description

### Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 9 and described below.

**Accumulator (A), B Register (B):** Four-bit registers used to hold results from the arithmetic logic unit (ALU) and to transfer data between memory, I/O, and other registers.

**W Register (W), X Register (X), Y Register (Y):** Two-bit (W) and four-bit (X and Y) registers used

for indirect RAM addressing. The Y register is also used for D-port addressing.

**SPX Register (SPX), SPY Register (SPY):** Four-bit registers used to supplement the X and Y registers.

**Carry Flag (CA):** One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

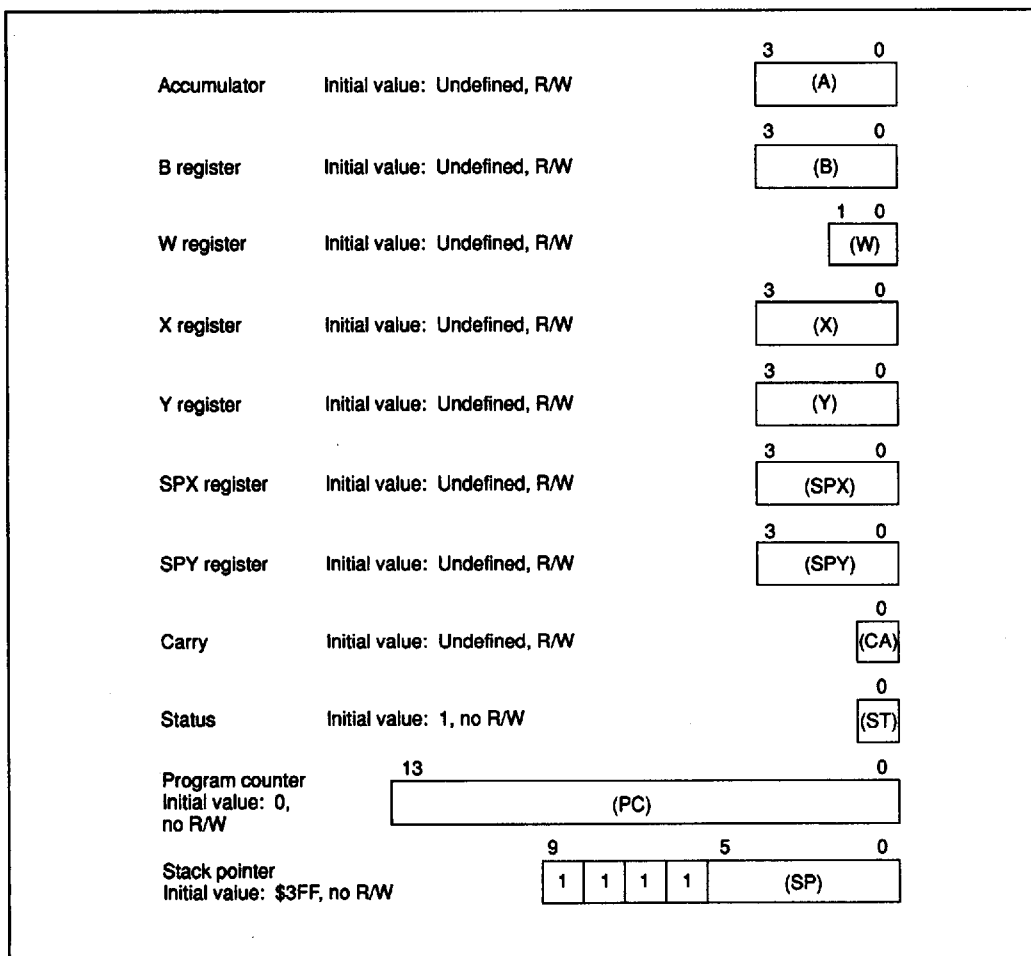


Figure 9 Registers and Flags



**Status Flag (ST):** One-bit flag that indicates an ALU overflow or ALU non-zero generated during an arithmetic or compare instruction, or the result of a bit test instruction. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is fetched, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

**Program Counter (PC):** A 14-bit counter that points to the ROM address of the instruction being executed.

**Stack Pointer (SP):** Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to \$3FF by MCU reset. It is decre-

mented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top 4 bits of the SP are fixed to 1111, a stack of up to 16 levels can be used.

The SP is initialized to \$3FF in two ways: by MCU reset or by resetting the RSP bit with the REM or REMD instruction.

**Reset**

The MCU is reset by setting the RESET pin high. At power-on or when stop mode is cancelled, RESET must be high for at least one  $t_{RC}$  to enable the oscillator to stabilize. In other cases, a RESET input for two instruction cycles resets the MCU.

Initial values of the registers and counters after MCU reset are listed in table 1.

**Table 1 Initial Values after MCU Reset**

Item	Abbr.	Initial Value	Contents	
Program counter	(PC)	\$0000	Indicates program execution point from start address of ROM area	
Status flag	(ST)	1	Enables conditional branching	
Stack pointer	(SP)	\$3FF	Stack level 0	
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Open-drain PMOS port data register	(PDR)	All bits 0	Enables output at level 0
	Standard port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Port mode register C	(PMRC)	0000	Refer to description of port mode register C
	Interrupt mode registers A, B	(IMRA, IMRB)	0000	Refer to description of interrupt mode registers A and B

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**Table 1 Initial Values after MCU Reset (cont)**

Item	Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000 Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000 Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000 Refer to description of timer mode register C
	Timer mode register D	(TMD)	0000 Refer to description of timer mode register D
	Timer mode register E	(TME)	0000 Refer to description of timer mode register E
	Serial mode register 1	(SMR1)	0000 Refer to description of serial mode register 1
	Serial mode register 2	(SMR2)	0000 Refer to description of serial mode register 2
	Prescaler S		\$000 —
	Prescaler W		\$00 —
	Timer counter A	(TCA)	\$00 —
	Timer counter B	(TCB)	\$00 —
	Timer counter C	(TCC)	\$00 —
	Timer counter D	(TCD)	\$00 —
	Timer buffer register E	(TBE)	\$00 Refer to description of timer buffer register E
	Timer load register B	(TLR)	\$00 Refer to description of timer load register B
	Timer load register C	(TCR)	\$00 Refer to description of timer load register C
	Timer load register D	(TDR)	\$00 Refer to description of timer load register D
	Octal counter (× 2)		000 —
	Timer load register G	(TLG)	\$0000 Refer to description of timer load register G
	A/D control register	(ADCR)	0000 Refer to description of A/D control register
Input capture control register	(ICC)	0000 Refer to description of input capture control register	
Input capture data register	(ICSR)	0000 Refer to description of input capture data register	
Buzzer control register	(BCR)	0000 Refer to description of buzzer control register	

**Table 1 Initial Values after MCU Reset (cont)**

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface (cont)	Output compare control register	(OCC)	0000	Refer to description of output compare control register
	Output compare status register	(OCSR)	0000	Refer to description of output compare status register
	A/D status register	(ADSR)	0000	Refer to description of A/D status register
	A/D data register	(ADR)	\$80	Refer to description of A/D data register
	16-bit counter (timer counter G)	(TCG)	\$0000	—
	8-bit counter (timer counter F)	(TCF)	\$00	—
	Compare control register	(CCR)	0000	Refer to description of output compare control register
Bit register	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
Miscellaneous register		(MIS)	0000	Refer to description of miscellaneous register
Pattern ROM bank register		(PBNK)*	00	Refer to description of 8-kword pattern ROM

Notes: The status of other registers and flags after MCU reset are shown below.

\* Applies to HD404710 and HD4074710.

Item	Abbr.	Status after Cancellation of Stop Mode by MCU Reset	In Other Cases at MCU Reset
Carry flag	(CA)	Pre-MCU-reset values are not retained: values must be initialized by software	Pre-MCU-reset values are not retained: values must be initialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial 1 data register	(SR1)		
Serial 2 data register	(SR2)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

## HD404710 Series

### Interrupts

The MCU has 14 interrupt sources: six external signals ( $\overline{INT}_0$ – $\overline{INT}_5$ ), four timer/counters (timers A, B, C, and D), two serial interfaces (serial 1 and serial 2), an A/D converter, and an input capture. An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

**Interrupt Control Bits and Interrupt Processing:** Locations \$000 through \$003 and \$020 through \$024 in RAM are reserved for the interrupt control bits which can only be accessed by RAM bit manipulation instructions. The interrupt request flags (IFs) can only be set by signals from interrupt sources. MCU reset initializes the interrupt enable flag (IE) and interrupt request flags (IFs) to 0 and the interrupt masks (IMs) to 1.

A block diagram of the interrupt control circuit is shown in figure 10, interrupt priorities and vector addresses are listed in table 2, and the interrupt

processing conditions for the 14 interrupt sources are listed in table 3. An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, interrupt processing begins. A priority programmable logic array generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 11, and an interrupt processing flowchart is shown in figure 12. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMWL instruction at each vector address to branch the program to the start address of the interrupt routine, and reset the IF by a software instruction within the interrupt routine.

Note: The interrupt mask bit will not be set by interrupt processing.

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET	—	\$0000
$\overline{INT}_0$	1	\$0002
$\overline{INT}_1$	2	\$0004
$\overline{INT}_2$	3	\$0006
Input capture	4	\$0008
Timer A	5	\$000A
Timer B	6	\$000C
Timer C	7	\$000E
Timer D	8	\$0010
Serial 1	9	\$0012
A/D	10	\$0014
$\overline{INT}_3$	11	\$0016
$\overline{INT}_4$	12	\$0018
$\overline{INT}_5$	13	\$001A
Serial 2	14	\$001C

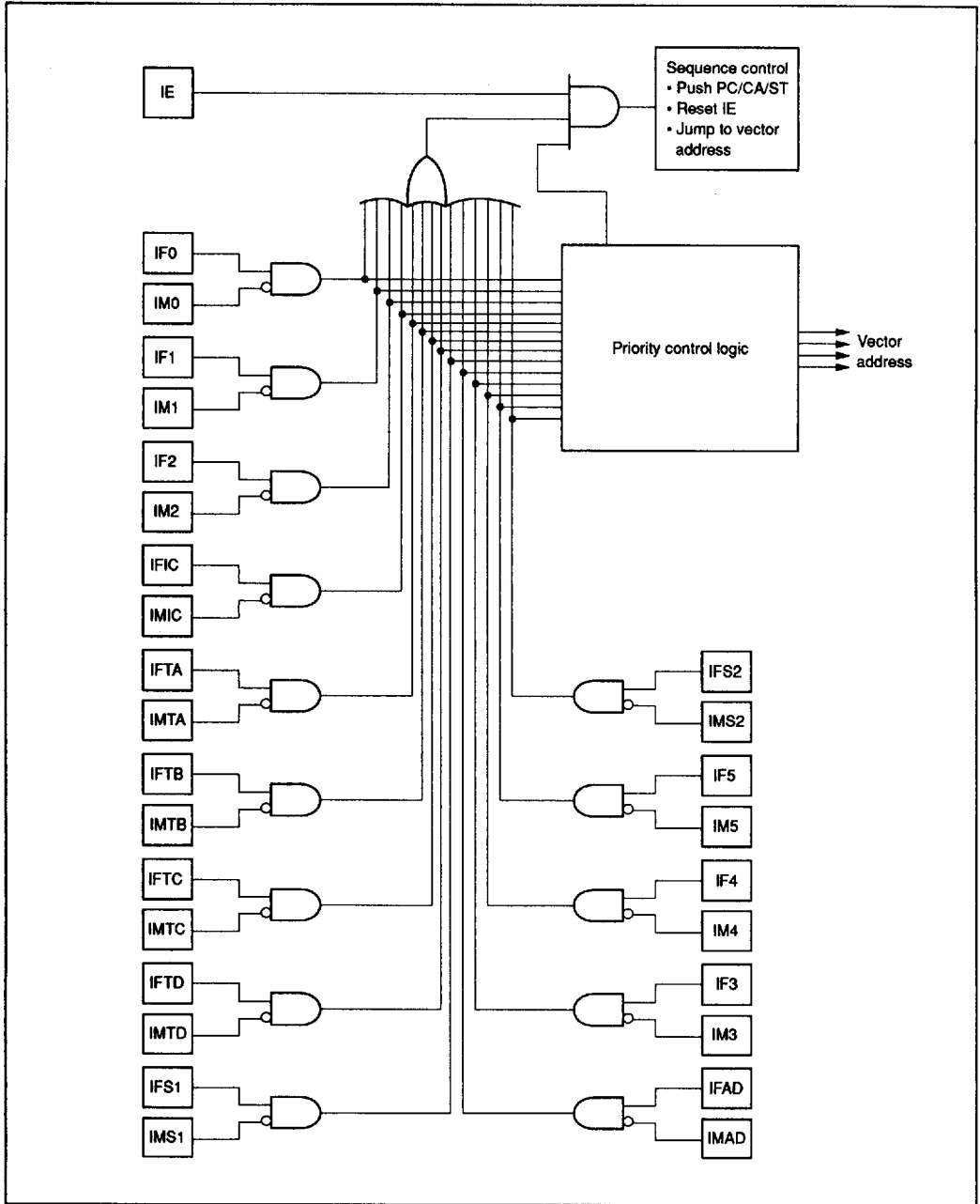


Figure 10 Block Diagram of Interrupt Control Circuit

# HD404710 Series

**Table 3 Interrupt Conditions**

Interrupt Control Bit	Interrupt Source						
	$\overline{INT}_0$	$\overline{INT}_1$	$\overline{INT}_2$	Input Capture	Timer A	Timer B	Timer C
IE	1	1	1	1	1	1	1
IF0 • $\overline{IM0}$	1	0	0	0	0	0	0
IF1 • $\overline{IM1}$	*	1	0	0	0	0	0
IF2 • $\overline{IM2}$	*	*	1	0	0	0	0
IFIC • $\overline{IMIC}$	*	*	*	1	0	0	0
IFTA • $\overline{IMTA}$	*	*	*	*	1	0	0
IFTB • $\overline{IMTB}$	*	*	*	*	*	1	0
IFTC • $\overline{IMTC}$	*	*	*	*	*	*	1
IFTD • $\overline{IMTD}$	*	*	*	*	*	*	*
IFS1 • $\overline{IMS1}$	*	*	*	*	*	*	*
IFAD • $\overline{IMAD}$	*	*	*	*	*	*	*
IF3 • $\overline{IM3}$	*	*	*	*	*	*	*
IF4 • $\overline{IM4}$	*	*	*	*	*	*	*
IF5 • $\overline{IM5}$	*	*	*	*	*	*	*
IFS2 • $\overline{IMS2}$	*	*	*	*	*	*	*

Note: Bits marked by \* can be either 0 or 1. Their values have no effect on operation.

Table 3 Interrupt Conditions (cont)

Interrupt Control Bit	Interrupt Source						
	Timer D	Serial 1	A/D	$\overline{\text{INT}}_3$	$\overline{\text{INT}}_4$	$\overline{\text{INT}}_5$	Serial 2
IE	1	1	1	1	1	1	1
IF0 • $\overline{\text{IM0}}$	0	0	0	0	0	0	0
IF1 • $\overline{\text{IM1}}$	0	0	0	0	0	0	0
IF2 • $\overline{\text{IM2}}$	0	0	0	0	0	0	0
IFIC • $\overline{\text{IMIC}}$	0	0	0	0	0	0	0
IFTA • $\overline{\text{IMTA}}$	0	0	0	0	0	0	0
IFTB • $\overline{\text{IMTB}}$	0	0	0	0	0	0	0
IFTC • $\overline{\text{IMTC}}$	0	0	0	0	0	0	0
IFTD • $\overline{\text{IMTD}}$	1	0	0	0	0	0	0
IFS1 • $\overline{\text{IMST}}$	*	1	0	0	0	0	0
IFAD • $\overline{\text{IMAD}}$	*	*	1	0	0	0	0
IF3 • $\overline{\text{IM3}}$	*	*	*	1	0	0	0
IF4 • $\overline{\text{IM4}}$	*	*	*	*	1	0	0
IF5 • $\overline{\text{IM5}}$	*	*	*	*	*	1	0
IFS2 • $\overline{\text{IMS2}}$	*	*	*	*	*	*	1

Note: Bits marked by \* can be either 0 or 1. Their values have no effect on operation.

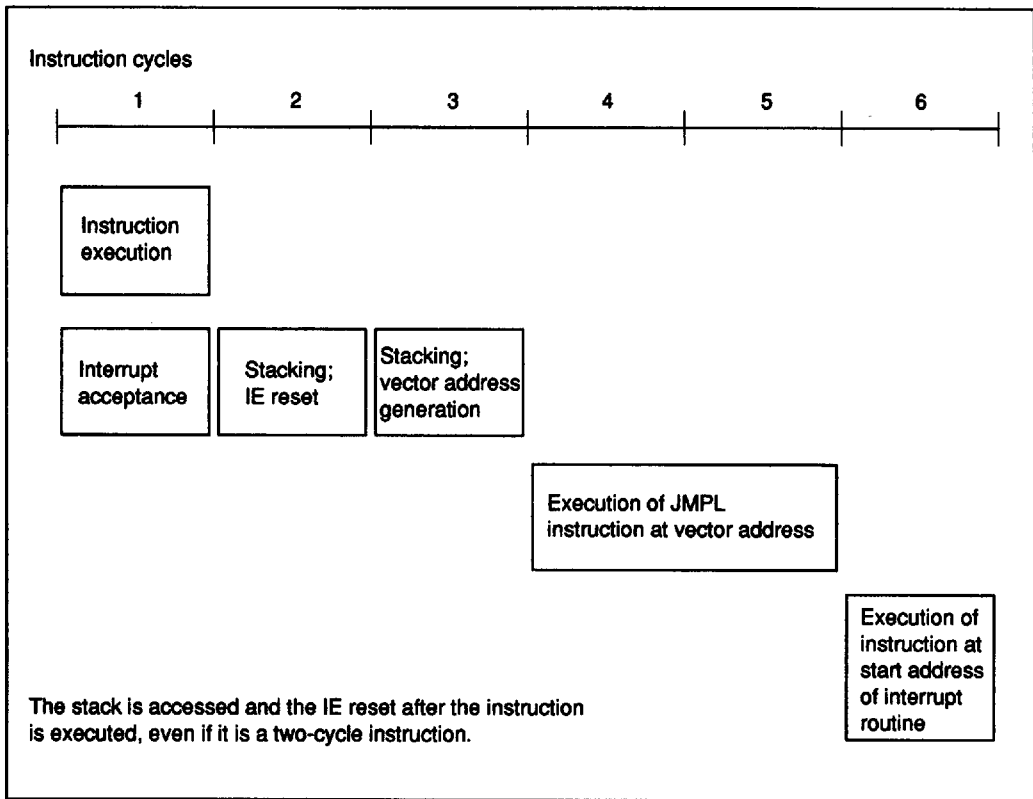


Figure 11 Interrupt Processing Sequence



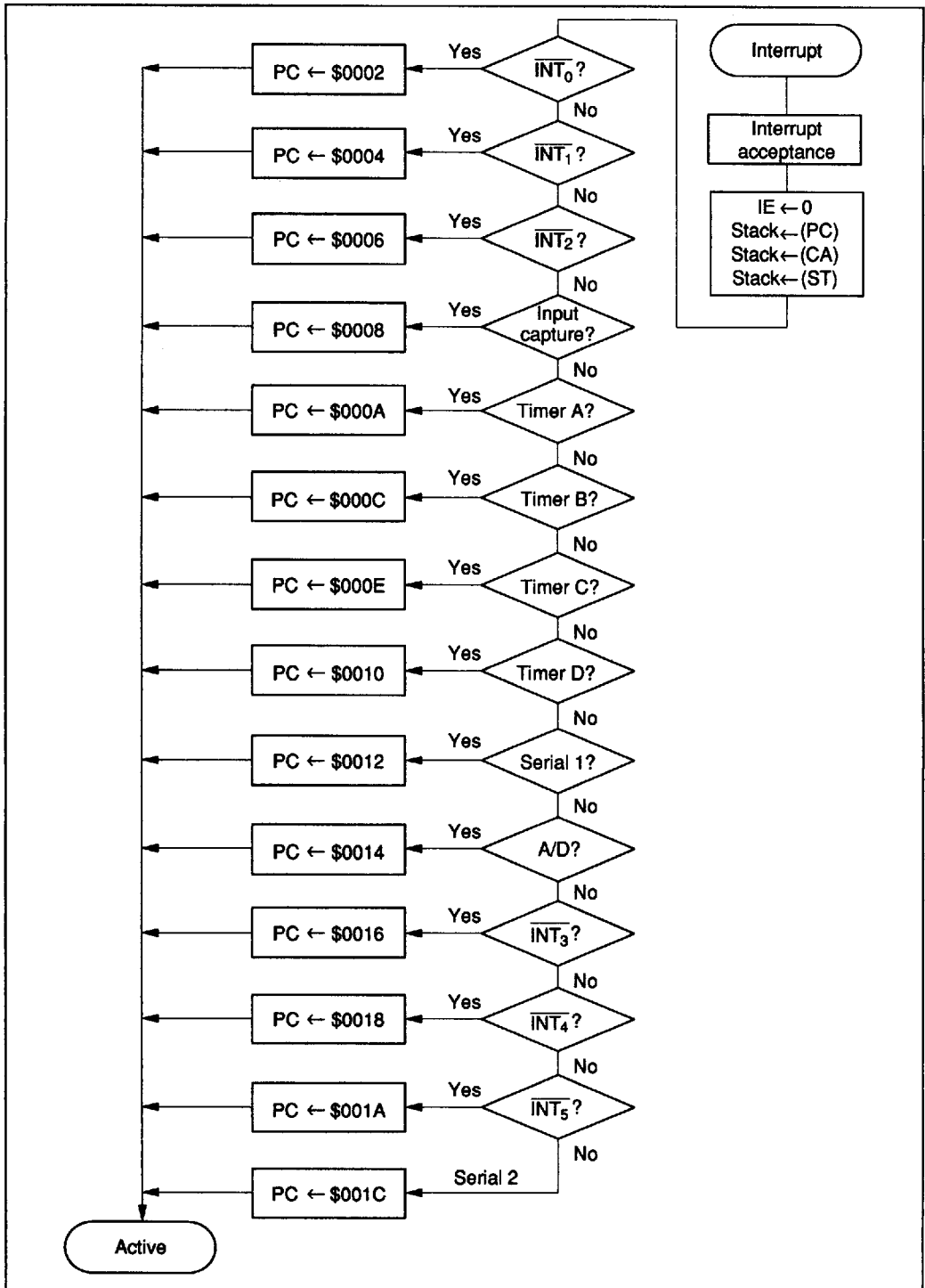


Figure 12 Interrupt Processing Flowchart

## HD404710 Series

**Interrupt Enable Flag (IE: \$000, Bit 0):** Controls all interrupts (table 4). IE is reset to 0 by the interrupt processing and set to 1 by the RTNI instruction.

**External Interrupts ( $\overline{INT}_0$ – $\overline{INT}_5$ ):** The MCU has six external interrupt pins.

The  $\overline{INT}_1$  input can be used as a clock input for timer B in which case timer B increments at each edge selected by the interrupt mode register (IMRA) (figure 13). In this case, the external interrupt request flag (IM1) must be set to inhibit the  $\overline{INT}_1$  interrupt request. The  $\overline{INT}_4$  input can be used as an external trigger for the output compare timer.

**External Interrupt Request Flags (IF0: \$000, Bit 2; IF1: \$001, Bit 0; IF2: \$001, Bit 2; IF3: \$022, Bit 2; IF4: \$023, Bit 0; IF5: \$023, Bit 2):** Set at the rising or falling edges of the corresponding  $\overline{INT}_0$  to  $\overline{INT}_5$  inputs (table 5).

IF0, IF4, and IF5 are set at the falling edges of  $\overline{INT}_0$ ,  $\overline{INT}_4$ , and  $\overline{INT}_5$ , respectively, and IF1, IF2, and IF3 are set at either the rising or falling edges of  $\overline{INT}_1$ ,  $\overline{INT}_2$ , and  $\overline{INT}_3$ , respectively. The active edge is selected by the interrupt mode register (IMRA, IMRB).

**External Interrupt Masks (IM0: \$000, Bit 3; IM1: \$001, Bit 1; IM2: \$001, Bit 3; IM3: \$022, Bit 3; IM4: \$023, Bit 1; IM5: \$023, Bit 3):** Mask interrupt requests caused by the corresponding external interrupt request flags (table 6).

**Input Capture Interrupt Request Flag (IFIC: \$002, Bit 0):** Set by an overflow from timer/counter F if bit 0 of the input capture status register (ICSR) is 0, and an input capture input if bit 0 of ICSR is 1 (table 7).

**Input Capture Interrupt Mask (IMIC: \$002, Bit 1):** Masks an interrupt request caused by the input capture interrupt request flag (table 8).

**Table 4 Interrupt Enable Flag**

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

**Table 5 External Interrupt Request Flags**

IF0–IF5	Interrupt Request
0	Disabled
1	Enabled

**Table 6 External Interrupt Masks**

IM0–IM5	Interrupt Request
0	Enabled
1	Disabled (Masked)

**Table 7 Input Capture Interrupt Request Flag**

IFIC	Interrupt Request
0	Disabled
1	Enabled

**Table 8 Input Capture Interrupt Mask**

IMIC	Interrupt Request
0	Enabled
1	Disabled (Masked)

**Timer A Interrupt Request Flag (IFTA: \$002, Bit 2):** Set by an overflow from timer A (table 9).

**Timer A Interrupt Mask (IMTA: \$002, Bit 3):** Masks an interrupt request caused by the timer A interrupt request flag (table 10).

**Timer B Interrupt Request Flag (IFTB: \$003, Bit 0):** Set by an overflow from timer B (table 11).

**Timer B Interrupt Mask (IMTB: \$003, Bit 1):** Masks an interrupt request caused by the timer B interrupt request flag (table 12).

**Timer C Interrupt Request Flag (IFTC: \$003, Bit 2):** Set by an overflow from timer C (table 13).

**Timer C Interrupt Mask (IMTC: \$003, Bit 3):** Masks an interrupt request caused by the timer C interrupt request flag (table 14).

**Timer D Interrupt Request Flag (IFTD: \$021, Bit 0):** Set by an overflow from timer D (table 15).

**Timer D Interrupt Mask (IMTD: \$021, Bit 1):** Masks an interrupt request caused by the timer D interrupt request flag (table 16).

**Table 9 Timer A Interrupt Request Flag**

IFTA	Interrupt Request
0	Disabled
1	Enabled

**Table 10 Timer A Interrupt Mask**

IMTA	Interrupt Request
0	Enabled
1	Disabled (Masked)

**Table 11 Timer B Interrupt Request Flag**

IFTB	Interrupt Request
0	Disabled
1	Enabled

**Table 12 Timer B Interrupt Mask**

IMTB	Interrupt Request
0	Enabled
1	Disabled (Masked)

**Table 13 Timer C Interrupt Request Flag**

IFTC	Interrupt Request
0	Disabled
1	Enabled

**Table 14 Timer C Interrupt Mask**

IMTC	Interrupt Request
0	Enabled
1	Disabled (Masked)

**Table 15 Timer D Interrupt Request Flag**

IFTD	Interrupt Request
0	Disabled
1	Enabled

**Table 16 Timer D Interrupt Mask**

IMTD	Interrupt Request
0	Enabled
1	Disabled (Masked)

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**Serial Interrupt Request Flags (IFS1: \$021, Bit 2; IFS2: \$024, Bit 0):** Set when the octal counter counts the eighth clock signal or when data transmission stops, resetting the octal counter (table 17).

**Serial Interrupt Masks (IMS1: \$021, Bit 3; IMS2: \$024, Bit 1):** Mask an interrupt request caused by the serial 1 and serial 2 interrupt request flags (table 18).

**A/D Interrupt Request Flag (IFAD: \$022, Bit 0):** Set by the completion of an A/D conversion (table 19).

**A/D Interrupt Mask (IMAD: \$022, Bit 1):** Masks an interrupt request caused by the A/D interrupt request flag (table 20).

**Table 17 Serial Interrupt Request Flags**

IFS1, IFS2	Interrupt Request
0	Disabled
1	Enabled

**Table 18 Serial Interrupt Masks**

IMS1, IMS2	Interrupt Request
0	Enabled
1	Disabled (Masked)

**Table 19 A/D Interrupt Request Flag**

IFAD	Interrupt Request
0	Disabled
1	Enabled

**Table 20 A/D Interrupt Mask**

IMAD	Interrupt Request
0	Enabled
1	Disabled (Masked)

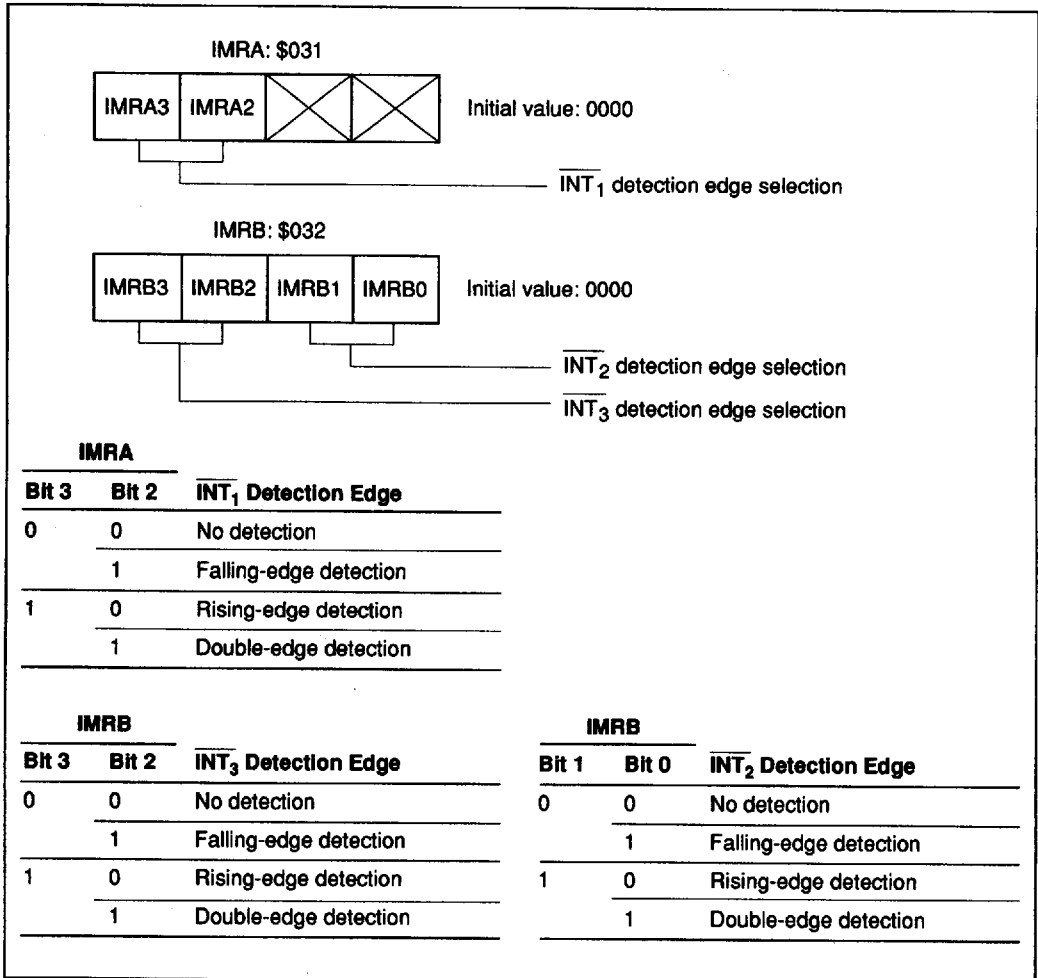


Figure 13 Interrupt Mode Register

## Operating Modes

Five operating modes are available, specified by how the clock is used, as shown in table 21. The functions available in each mode are listed in table 22, operations are listed in table 23, and transitions between operating modes are listed in figure 14.

**Active Mode:** The MCU operates according to the clock generated by the system oscillator.

**Standby Mode:** The MCU enters standby mode if the SBY instruction is executed in active mode.

In this mode, the oscillator remains active and the peripheral functions such as interrupts, timer/counters, and the serial interface are enabled, although

all instruction-control clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by a RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the instruction following the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and the program is resumed. A flowchart of operation in standby mode is shown in figure 15.

**Table 21 Low-Power Dissipation Modes**

		System Clock (@CPU)	
		Operating	Stopped
Non-time-base peripheral function clock (@PER)	Operating	Active mode (LSON = 0)	Standby mode
	Stopped	Subactive mode (optional) (LSON = 1)	Watch mode (TMA3 = 1) Stop mode (TMA3 = 0)

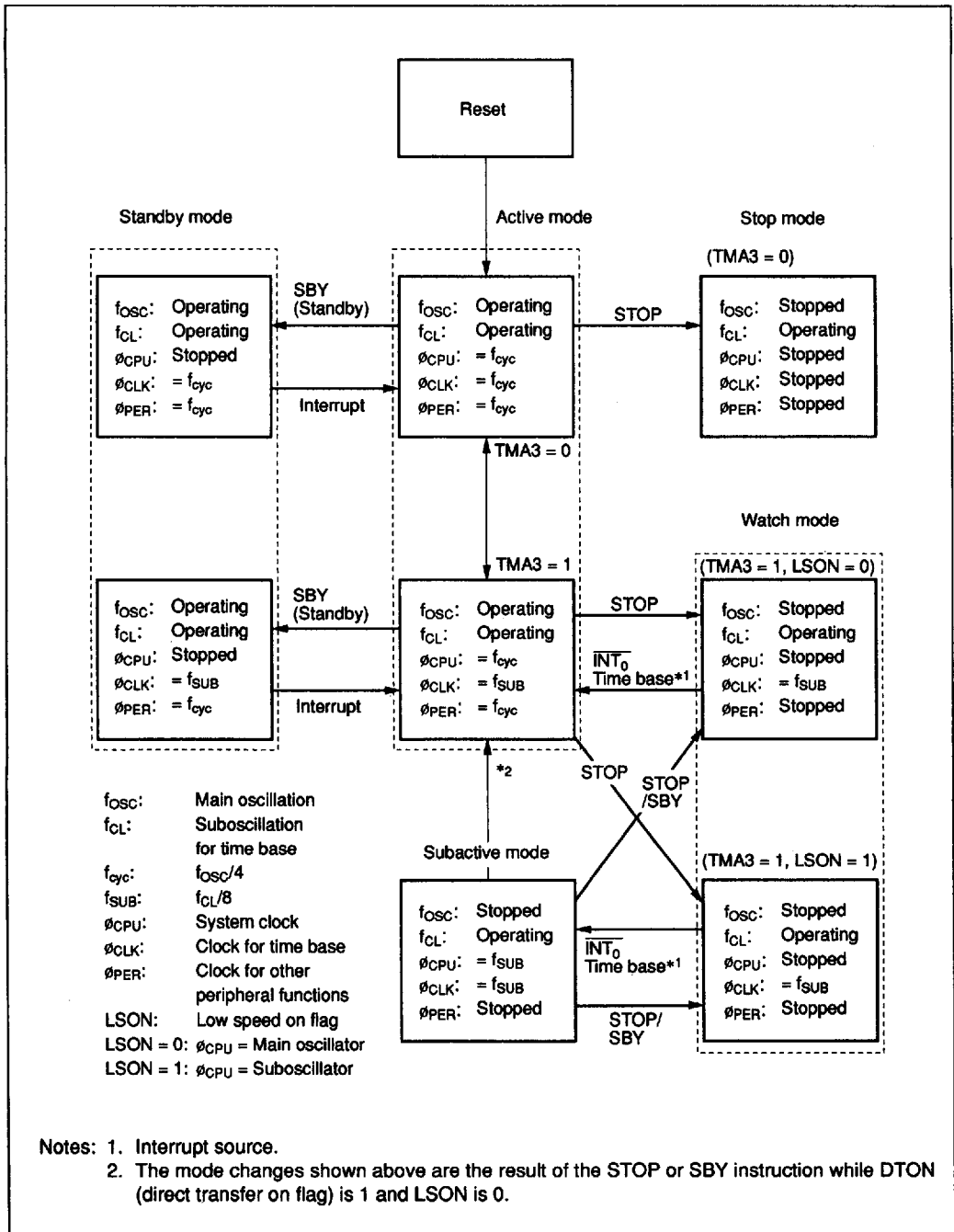


Figure 14 MCU Status Transitions

# HD404710 Series

**Table 22 Operations in Low-Power Dissipation Modes**

Function		Stop Mode	Watch Mode	Standby Mode	Active Mode	Subactive Mode <sup>*3</sup>
System oscillator		Stopped	Stopped			Stopped
Subsystem oscillator		*1				
CPU operation ( $\phi_{CPU}$ )	Instruction execution	Stopped	Stopped	Stopped		
	RAM	Retained	Retained	Retained		
	Registers, flags	Reset	Retained	Retained		
	I/O <sup>*2</sup>	Reset	Retained	Retained		
Peripheral functions, interrupts ( $\phi_{PER}$ )	$\overline{INT}_0$ – $\overline{INT}_5$	Reset	Retained			Retained
	Timer A	Reset	Retained			Retained
	Timer B	Reset	Retained			Retained
	Timer C	Reset	Retained			Retained
	Timer D	Reset	Retained			Retained
	Timer E (PWM)	Reset	Retained			Retained
	Input capture	Reset	Retained			Retained
	Output compare	Reset	Retained			Retained
	Serial 1, serial 2	Reset	Retained			Retained
A/D	Reset	Retained			Retained	
Time-base functions, interrupts ( $\phi_{CLK}$ )	$\overline{INT}_0$	Reset	*4	*5	*5	*4
	Time base	Reset	*4	*5	*5	*4

Notes:  indicates operating.

1. To reduce  $I_{CC}$ , stop oscillation in external circuits.
2. Refer to table 23.
3. Subactive mode is an optional function.
4. Refer to the Interrupt Frame section.
5. If TMA3 is set to 1, timer A and  $\overline{INT}_0$  are switched to time-base function and interrupt, respectively.

**Table 23 Input/Output in Low-Power Dissipation Modes**

	Output		Input
	Standby Mode	Stop/Watch/ Subactive Mode	All Modes (Input State)
$D_0$ – $D_{15}$	Retained/peripheral function output	High impedance	Input enabled
$RO$ – $RD$	Retained/peripheral function output	High impedance	Input enabled

Note: Applying a voltage between ( $V_{CC} - 0.3$ ) and ( $GND + 0.3$  V) to input-state pins increases the current between  $V_{CC}$  and GND.



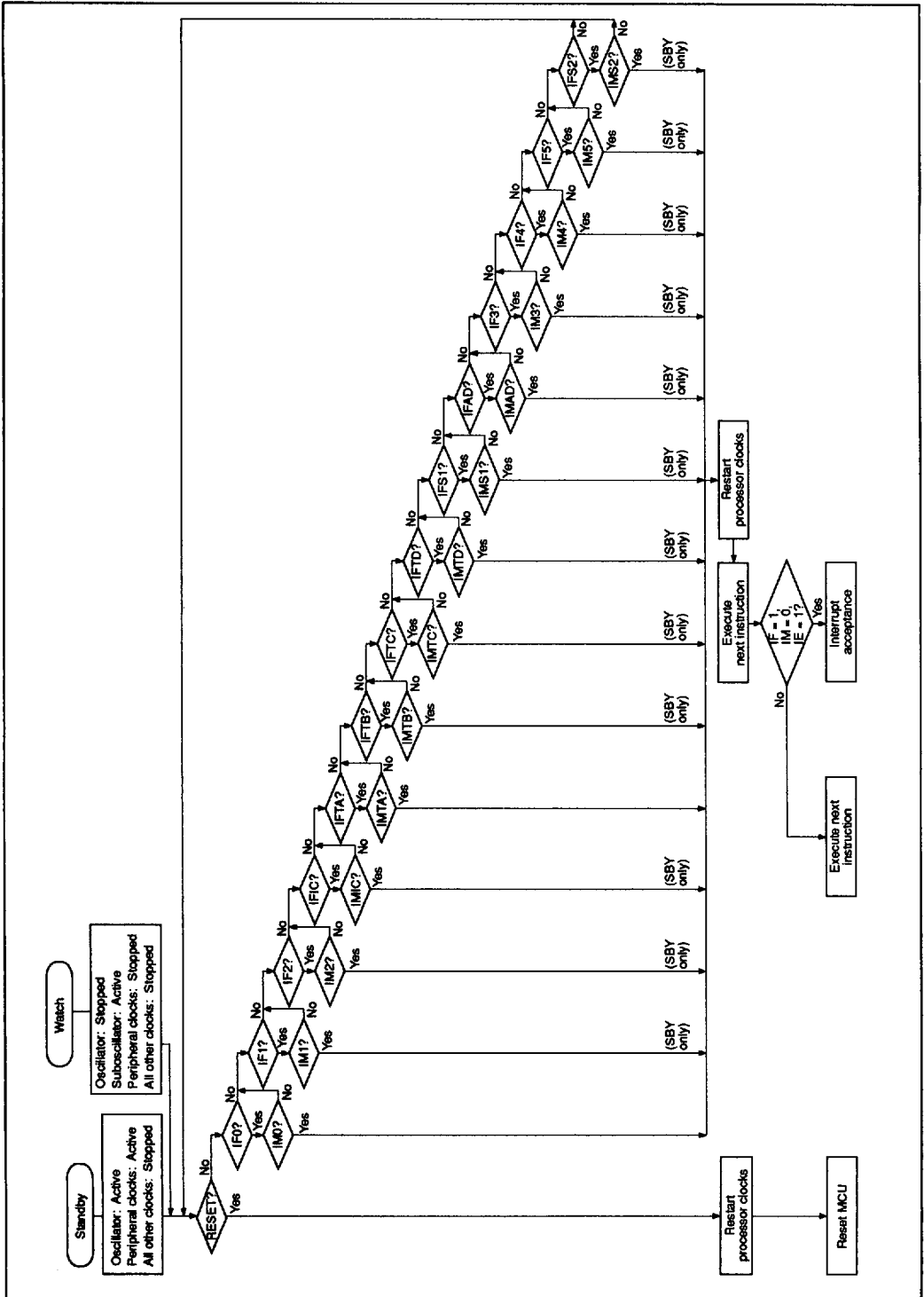


Figure 15 Flowchart of Watch and Standby Modes

# HD404710 Series

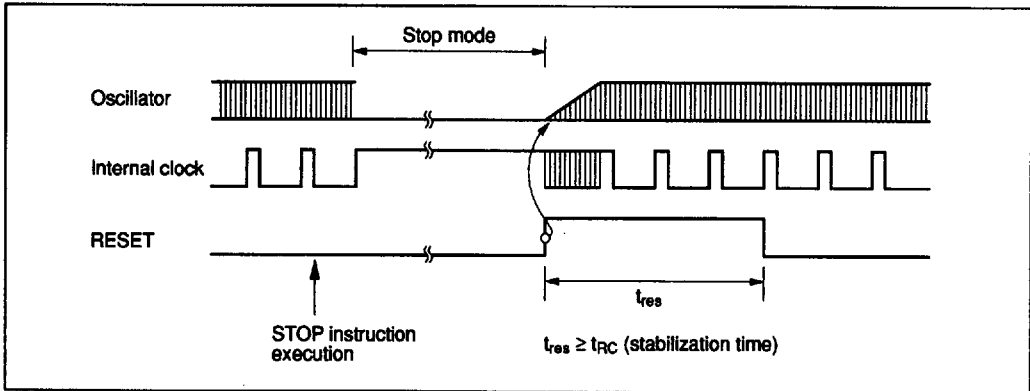
**Stop Mode:** The MCU enters stop mode if the STOP instruction is executed in active mode while TMA3 = 0. In this mode, the system oscillator stops, causing all MCU functions to stop as well.

Stop mode is terminated by a RESET input as shown in figure 16. RESET must be high for at least one  $t_{RC}$  to stabilize oscillation (refer to the AC Characteristics section). In stop mode, all RAM contents are retained.

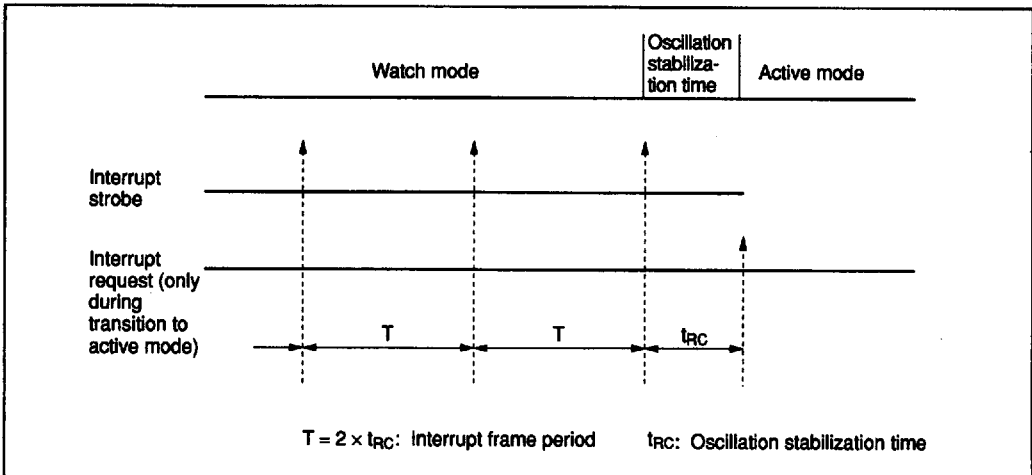
After stop mode is cancelled, the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register are not retained.

**Watch Mode:** The MCU enters watch mode if the STOP instruction is executed in active mode while TMA3 = 1, or if the STOP/SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input or a timer-A/ $\overline{INT}_0$  interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/ $\overline{INT}_0$  interrupt request, the MCU enters active mode if LSON is 0 or subactive mode if LSON is 1. Any interrupt request generated for the transition to active mode is delayed for half the interrupt frame period ( $t_{RC}$ ) to give the oscillation time to stabilize (figure 17). Operation during mode transition is the same as that at standby mode cancellation (figure 15).



**Figure 16 Timing of Stop Mode Cancellation**



**Figure 17 Interrupt Frame**

**Subactive Mode:** The CPU operates with a clock generated by the  $CL_1$  and  $CL_2$  oscillation circuits. Functions that can operate in subactive mode are listed in table 22. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

Subactive mode is an optional function that the user must specify on the function option list.

**Interrupt Frame:** In watch and subactive modes, timer A and  $\overline{INT}_0$  interrupts are generated in synchronism with the interrupt frame. The interrupt frame is repeated at the timing shown in figure 17. Three interrupt frame cycles can be selected by the settings of the miscellaneous register (figure 19).

The period from the interrupt strobe to the interrupt request generation is used as the oscillation time to stabilize during the transition from watch mode to active mode. Operation during the transition from watch mode to active mode is the same as a standby mode cancellation. The overflow timing during the transition to active mode by the

timer A interrupt request is the same as the interrupt strobe shown in figure 17.

**Direct Transfer:** By controlling the DTON, the MCU is placed directly from subactive to active mode. The detailed procedure is as follows (figure 18):

- Set the DTON flag in subactive mode while  $LSON = 0$ .
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode.

Note that DTON (\$020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time ( $t_D$ ) from subactive to active mode is  $t_{RC} < t_D < T + t_{RC}$ .

**MCU Operation Sequence:** The MCU operates in the sequence shown in figures 20 to 22. It is reset by a RESET input, regardless of its state.

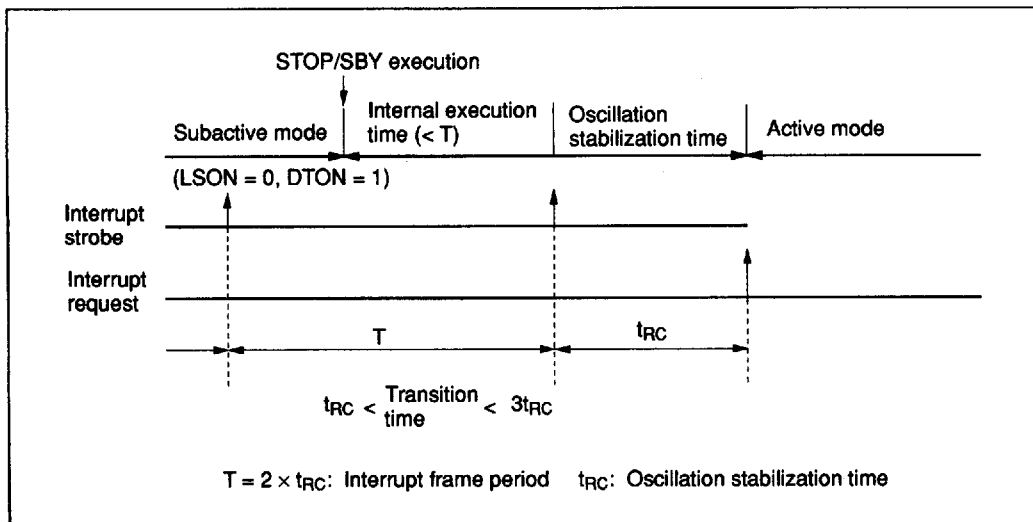


Figure 18 Timing of Subactive Mode Direct Transition

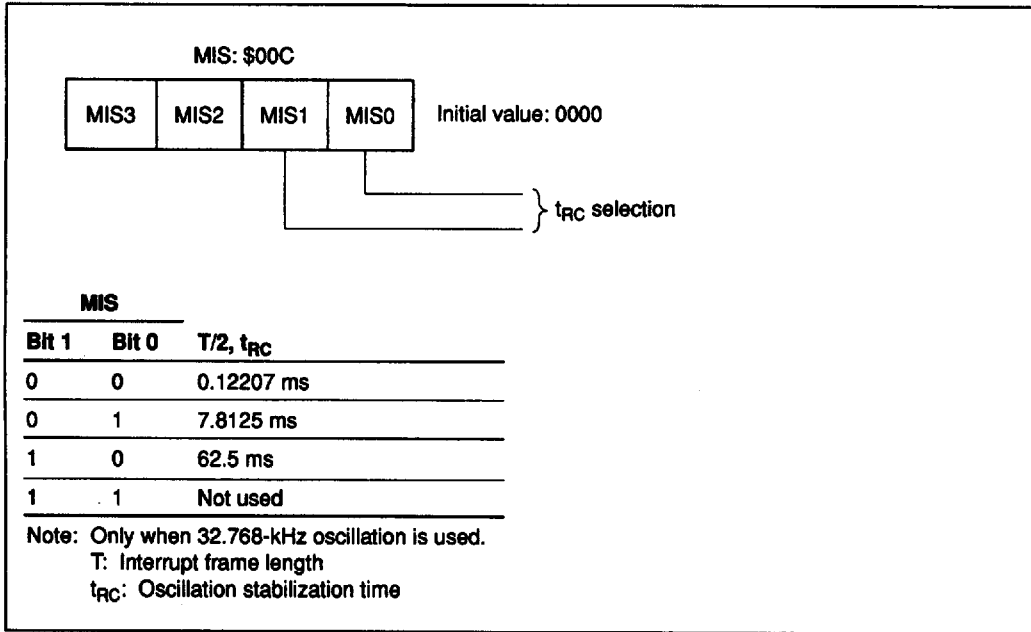


Figure 19 Miscellaneous Register

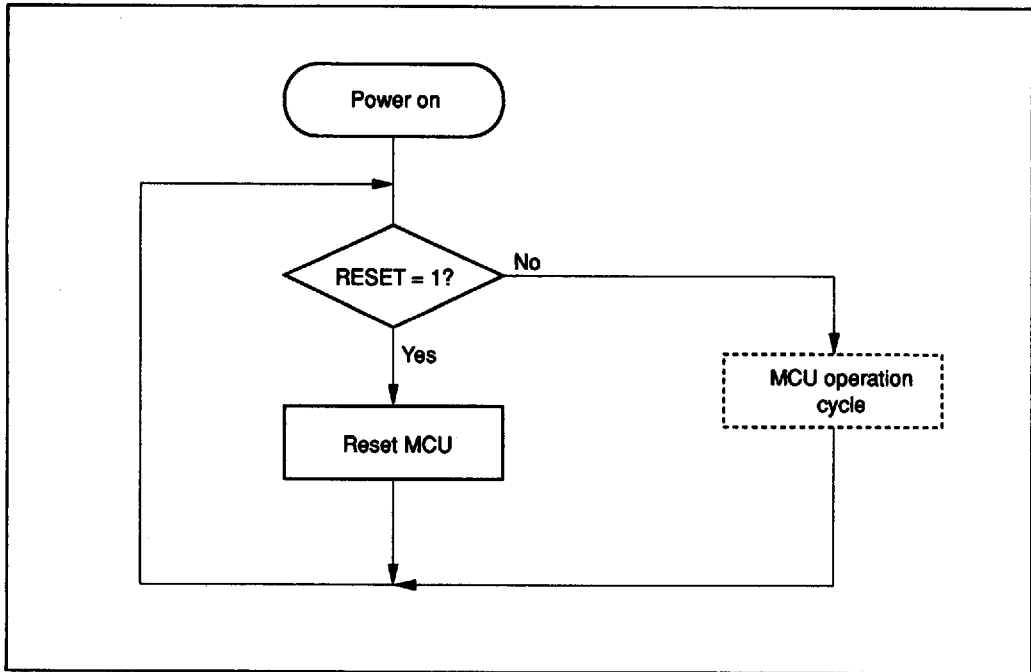


Figure 20 MCU Operation Flowchart (Power On)

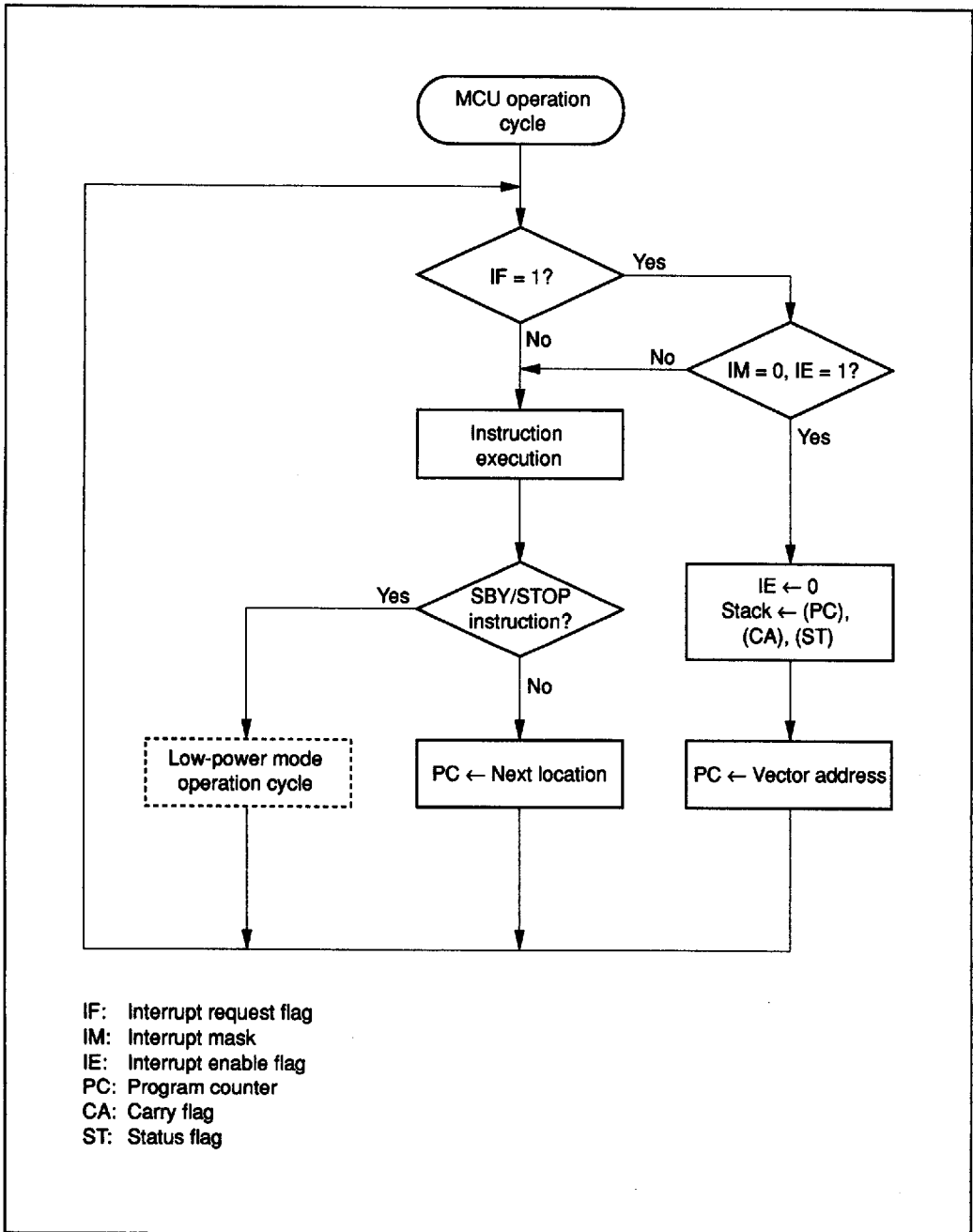


Figure 21 MCU Operation Flowchart (MCU Operation Cycle)

## HD404710 Series

The low-power mode operation sequence is shown in figure 22. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and

the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

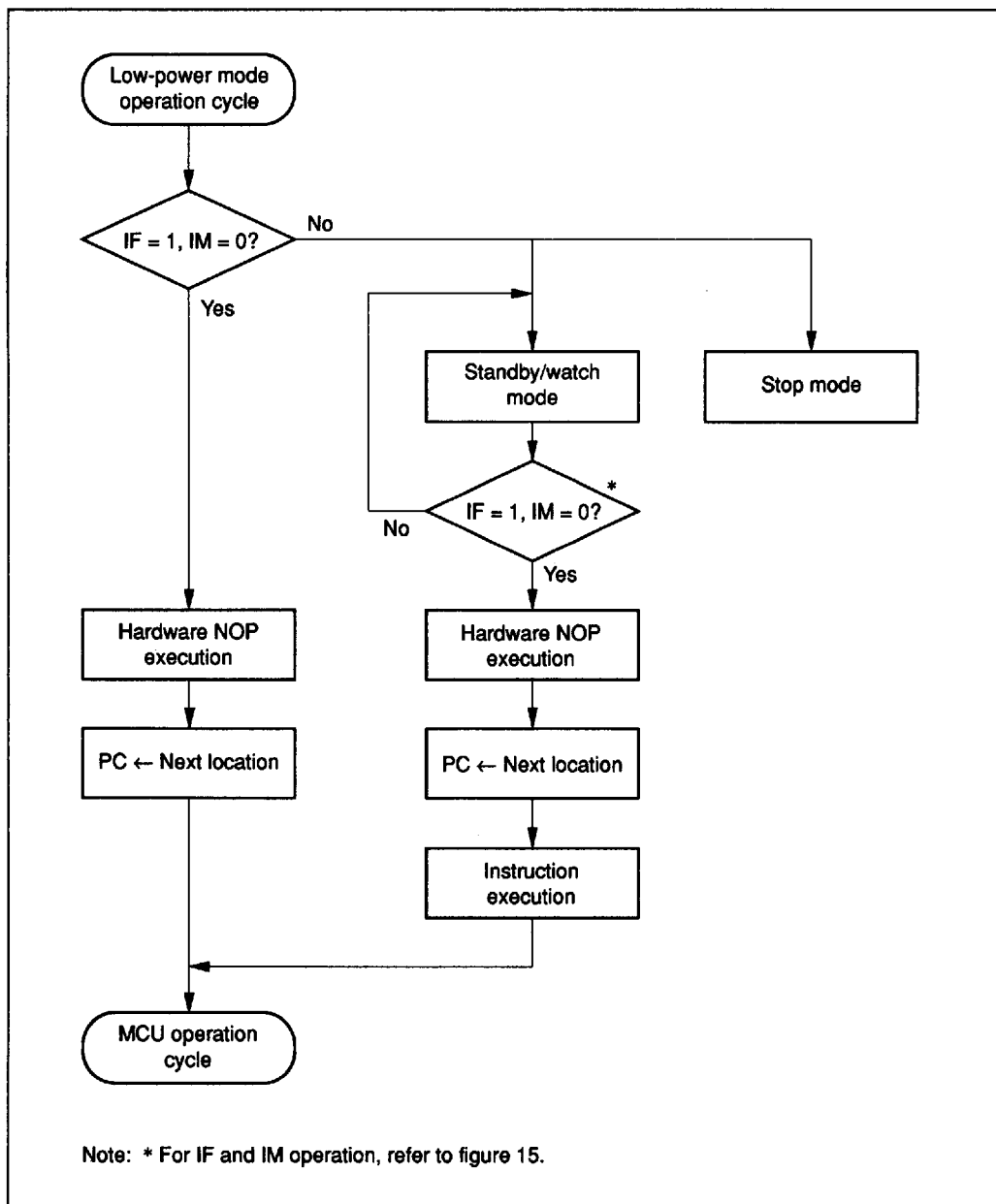
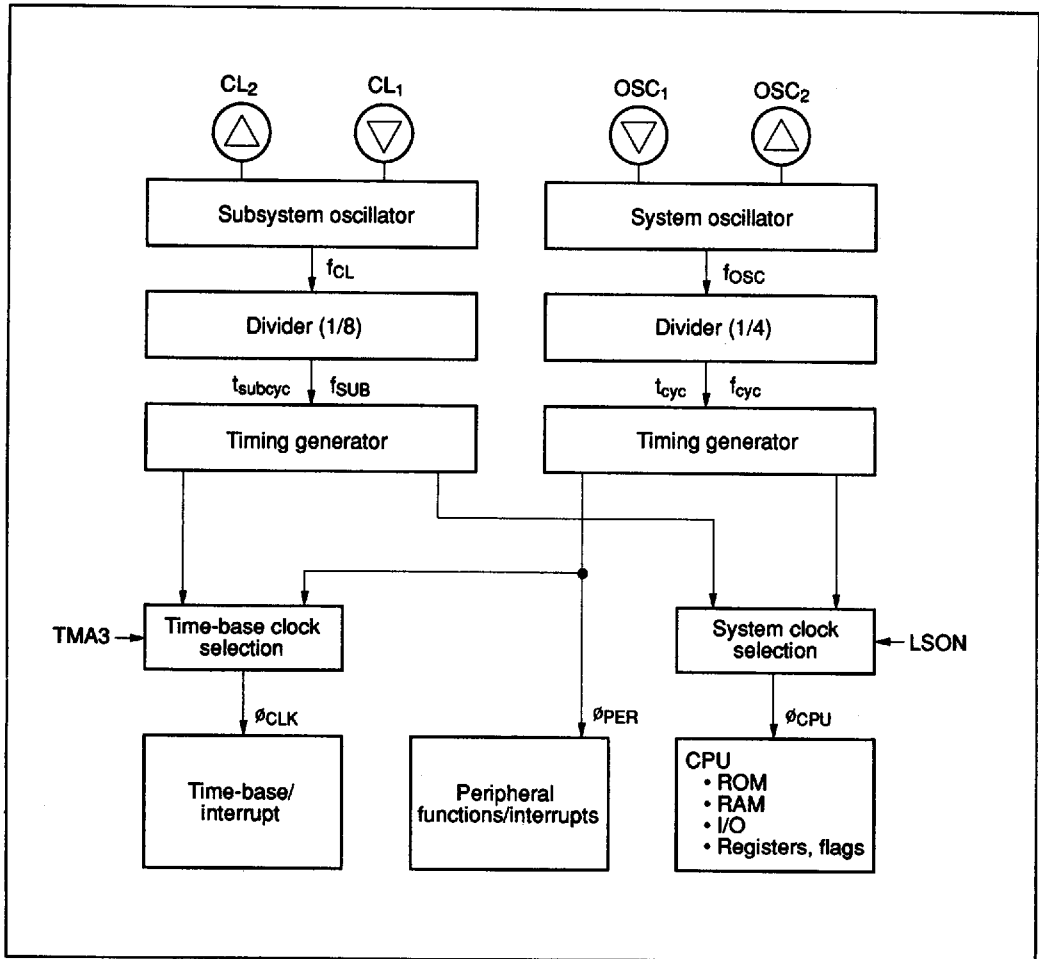


Figure 22 MCU Operation Flowchart (Low-Power Dissipation Mode Operation)

**Internal Oscillation Circuit**

A block diagram of the internal oscillation circuit is shown in figure 23. As shown in table 24, a crystal or a ceramic oscillator can be connected to OSC<sub>1</sub> and OSC<sub>2</sub>, and a 32.768-kHz crystal oscillator

can be connected to CL<sub>1</sub> and CL<sub>2</sub>. An external clock operation of the system oscillator is also available. If not using a subsystem oscillator, fix the CL<sub>1</sub> pin to V<sub>CC</sub> or GND.



**Figure 23 Internal Oscillation Circuit**

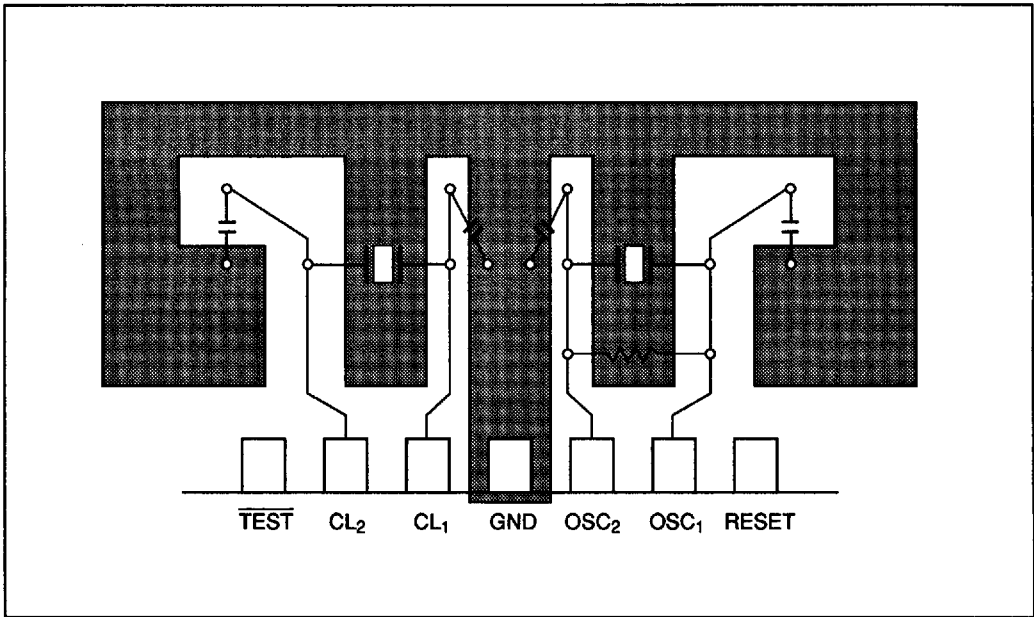


Figure 24 Typical Pattern Layout Example of Oscillation Circuit

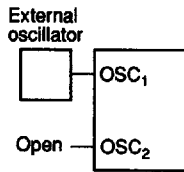


Table 24 Oscillator Circuit Examples

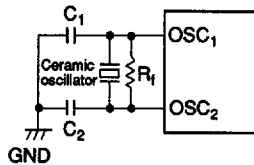
Circuit Configuration

Circuit Constants

External clock operation  
(OSC<sub>1</sub>, OSC<sub>2</sub>)

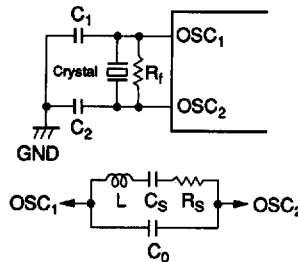


Ceramic oscillator  
(OSC<sub>1</sub>, OSC<sub>2</sub>)



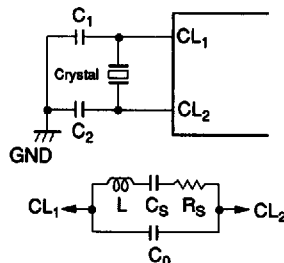
Ceramic oscillator:  
CSA4.00MG (Murata)  
 $R_f = 1\text{ M}\Omega \pm 20\%$   
 $C_1 = C_2 = 33\text{ pF} \pm 20\%$

Crystal oscillator  
(OSC<sub>1</sub>, OSC<sub>2</sub>)



$R_f = 1\text{ M}\Omega \pm 20\%$   
 $C_1 = C_2 = 22\text{ pF} \pm 20\%$   
Crystal: Equivalent to circuit  
shown at bottom left  
 $C_0 = 7\text{ pF, max.}$   
 $R_s = 100\ \Omega, \text{ max.}$   
 $f = 1.6\text{ to }4.5\text{ MHz}$

Crystal oscillator  
(CL<sub>1</sub>, CL<sub>2</sub>)



$C_1 = C_2 = 15\text{ pF} \pm 5\%$   
Crystal: MX38T  
(Nihon Dempa Kogyo)  
 $C_0 = 1.5\text{ pF, typ.}$   
 $R_s = 14\text{ k}\Omega, \text{ typ.}$   
 $f = 32.768\text{-kHz}$

- Notes:
1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, consult the crystal oscillator or ceramic oscillator manufacturer to determine the actual circuit parameters required.
  2. Wiring between the OSC<sub>1</sub>/OSC<sub>2</sub> pins and other elements must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the oscillation circuit in figure 24.
  3. If not using a 32.768-kHz crystal oscillator, fix the CL<sub>1</sub> pin to GND and leave the CL<sub>2</sub> pin open.

## Input/Output

The MCU (mask ROM version) has 70 input/output pins, 33 of the input/output pins being standard pins whose circuits can be selected as with pull-up MOS (B) or without pull-up MOS (C) option.

The HD404719 and HD404710 have 37 other high-voltage pins whose circuits can be selected as with pull-down MOS (E) or without pull-down MOS (D) option. If the former option is selected, the  $R5_0/V_{disp}$  pin must be set as  $V_{disp}$  by the mask option because the source of a pull-down MOS is connected to  $V_{disp}$ . The HD404719 and HD404710 have only pins without pull-up MOS (C) and without pull-down MOS (D).

**D Port:** The 16 out of 70 discrete I/O pins (D port) that are accessed individually. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions. Circuits of the D port are shown in table 25.

**R Ports:** Accessed in 4-bit units. Data is input to the ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions. The R6 to RB output buffers are turned on and off by R-port data control registers (DCR6–DCRB). Circuits of the R ports are shown

in table 25. The input/output buffer is shown in figure 25 and pin mode selection registers are shown in figure 26.

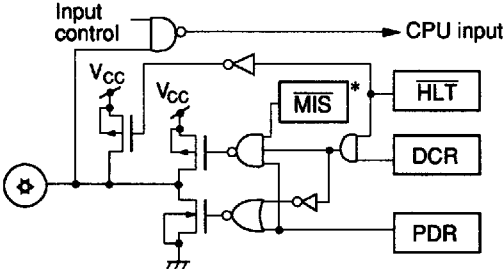
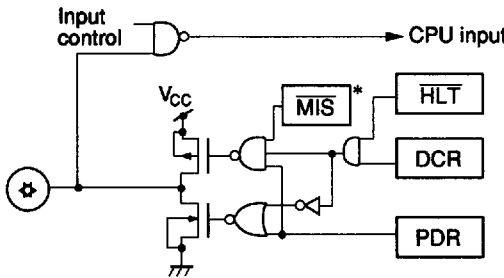
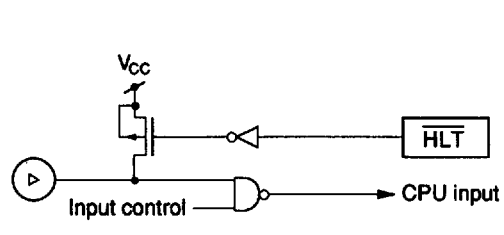
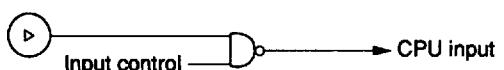
**Mask Options:** The circuits of the HD404719 and HD404710 are either without pull-up MOS (C) or without pull-down MOS (D), as shown in table 25 and figure 25. Options either with pull-up MOS (B) or with pull-down MOS (E) can be selected for the HD404719 and HD404710. However, note that these MCUs are not compatible with the HD4074719 and HD4074710.

**How to Deal with Unused I/O Pins:** I/O pins that are not needed by the user system must be fixed as follows to prevent LSI malfunctions due to noise. Note the following precautions:

- For high-voltage pins, the without pull-down MOS option must be selected. The pins are connected to the  $V_{CC}$  voltage of the user system.
- For standard pins, the without pull-down MOS option must be selected. The pins are connected to the GND voltage of the user system.
- Open-drain PMOS pins are connected to the  $V_{CC}$  voltage of the user system.

Table 25 Input/Output Pin Types

Standard Pins

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
I/O pins	 <p>Note: * Applies to R8<sub>2</sub> and R9<sub>2</sub>.</p>	R6 <sub>0</sub> –R6 <sub>3</sub> R7 <sub>0</sub> –R7 <sub>3</sub> R8 <sub>0</sub> –R8 <sub>3</sub> R9 <sub>0</sub> –R9 <sub>3</sub> RA <sub>0</sub> –RA <sub>3</sub> RB <sub>0</sub> –RB <sub>1</sub>
	 <p>Note: * Applies to R8<sub>2</sub> and R9<sub>3</sub>.</p>	
Input pins		R5 <sub>1</sub> –R5 <sub>3</sub> RC <sub>0</sub> –RC <sub>3</sub> RD <sub>0</sub> –RD <sub>3</sub>
		

# HD404710 Series

Table 25 Input/Output Pin Types (cont)

Standard Pins

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral I/O pins		$\overline{SCK_1}$ $\overline{SCK_2}$ (output) <sup>Note 1</sup>
Peripheral output pins	<p>Note: * Applies to SO<sub>1</sub> and SO<sub>2</sub>.</p>	SO <sub>1</sub> , SO <sub>2</sub> TOD TOE <sub>1</sub> , TOE <sub>2</sub> TOG BUZZ
	<p>Note: * Applies to SO<sub>1</sub> and SO<sub>2</sub>.</p>	

Table 25 Input/Output Pin Types (cont)

Standard Pins

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral input pins		$\overline{SCK}_1, \overline{SCK}_2$ (input) <sup>Note 1</sup> $SI_1, SI_2$ $\overline{INT}_0$ $\overline{INT}_1$ $\overline{INT}_2$ $\overline{INT}_3$ $\overline{INT}_4$ $ICT_0, ICT_1$
		$AN_0-AN_7$ $V_{ref} (R6_1)$

# HD404710 Series

**Table 25 Input/Output Pin Types (cont)**

**Standard Pins**

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
I/O pins	<p>Diagram (B) shows an I/O pin connected to a comparator. The pin is pulled up by a MOSFET. The comparator's output is connected to the CPU input. Mode selection signals HLT, DCR, and PDR are connected to the comparator's inputs.</p>	R6 <sub>0</sub> /COMP
	<p>Diagram (C) shows an I/O pin without a pull-up MOSFET. The pin is connected to a comparator. The comparator's output is connected to the CPU input. Mode selection signals HLT, DCR, and PDR are connected to the comparator's inputs.</p>	

**High-Voltage Pins**

Pin Type	Without Pull-Down MOS (D)/With Pull-Down MOS (E)	Pin Name
I/O pins	<p>Diagram (D) shows a high-voltage pin without a pull-down MOSFET. The pin is connected to a pull-up MOSFET. The input control gate is connected to the CPU input. Mode selection signals HLT and PDR are connected to the pull-up MOSFET's gate.</p>	D <sub>0</sub> -D <sub>15</sub> R <sub>0</sub> -R <sub>3</sub> R <sub>10</sub> -R <sub>13</sub> R <sub>20</sub> -R <sub>23</sub> R <sub>30</sub> -R <sub>33</sub> R <sub>40</sub> -R <sub>43</sub>
	<p>Diagram (E) shows a high-voltage pin with a pull-down MOSFET. The pin is connected to a pull-up MOSFET and a pull-down MOSFET. The input control gate is connected to the CPU input. Mode selection signals HLT and PDR are connected to the pull-up MOSFET's gate. The pull-down MOSFET's gate is connected to V<sub>disp</sub>.</p>	

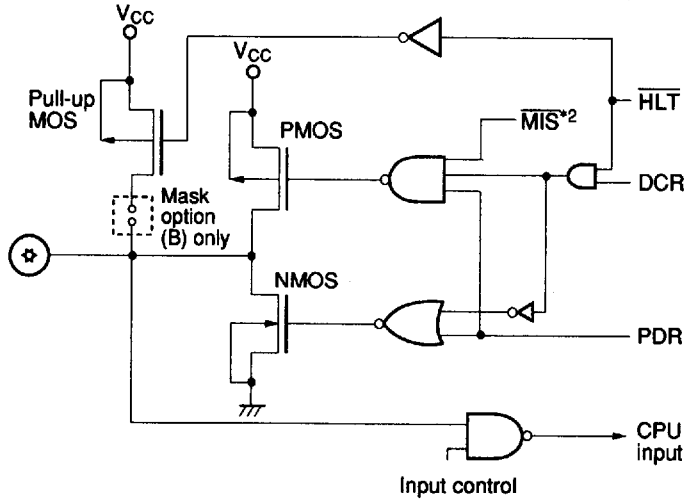
Table 25 Input/Output Pin Types (cont)

High-Voltage Pins

Pin Type	Without Pull-Down MOS (D)/With Pull-Down MOS (E)	Pin Name
Input pins		R5 <sub>0</sub>

- Notes:
1. If external clock mode is selected when the serial interface is used,  $\overline{SCK}_1$  and  $\overline{SCK}_2$  are used as input pins.
  2. In stop mode, the MCU is internally reset and peripheral functions are cancelled. The HLT signal goes high and the output pins are at high impedance.
  3. In watch/subactive mode, the HLT signal goes high and the output pins are at high impedance. The input level of I/O pins selected for peripheral functions must be fixed since these pins are in input state.
  4. Select the circuit type for a mask ROM MCU as shown below. A mask ROM MCU is compatible with a ZTAT™ MCU only when C- and D-type circuits are selected for the mask ROM MCU.

Product Type	Circuit Type			
	B	C	D	E
Mask ROM (HD404719, HD404710)			Optional	
ZTAT™ (HD4074719, HD4074710)		Fixed		



Mask Option	With Pull-Up MOS (B)				Without Pull-Up MOS (C)			
	0		1		0		1	
DCR								
PDR	0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	On	—
Pull-up MOS (C)	On	On	On	On	—	—	—	—

- Notes: 1. —: Off  
 2. For the R8<sub>2</sub>/SO<sub>1</sub> and R9<sub>3</sub>/SO<sub>2</sub> pins, the PMOSs are off when bits 2 and 3 of the miscellaneous register are set to 1.

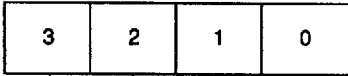
MIS	R8 <sub>2</sub> /SO <sub>1</sub>
Bit 2	PMOS Mode
0	On
1	Off

MIS	R9 <sub>3</sub> /SO <sub>2</sub>
Bit 3	PMOS Mode
0	On
1	Off

Figure 25 Input/Output Buffer



MIS (Miscellaneous register): \$00C

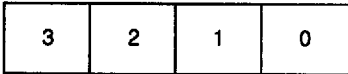


Initial value: 0000

R8<sub>2</sub>/SO<sub>1</sub> pin PMOS mode selection

R9<sub>3</sub>/SO<sub>2</sub> pin PMOS mode selection

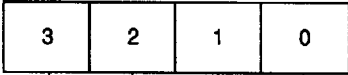
SMR1 (Serial mode register 1): \$005



Initial value: 0000

R9<sub>0</sub>/SCK<sub>1</sub> pin mode selection

PMRA (Port mode register A): \$004



Initial value: 0000

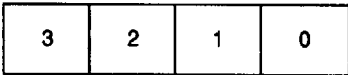
R8<sub>2</sub>/SO<sub>1</sub> pin mode selection

R8<sub>3</sub>/SI<sub>1</sub> pin mode selection

R7<sub>0</sub>/INT<sub>0</sub> pin mode selection

R7<sub>1</sub>/INT<sub>1</sub> pin mode selection

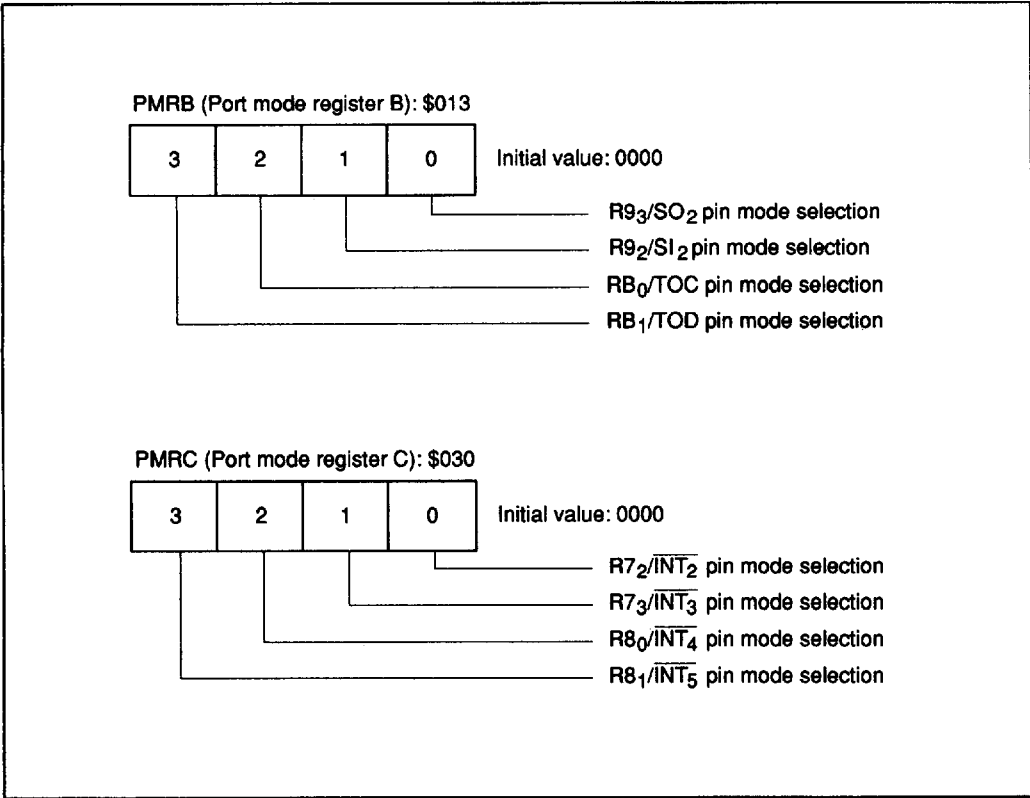
SMR2 (Serial mode register 2): \$014



Initial value: 0000

R9<sub>1</sub>/SCK<sub>2</sub> pin mode selection

Figure 26 Pin Mode Selection Registers



**Figure 26 Pin Mode Selection Registers (cont)**

**Timers**

The MCU has two prescalers (S and W) and five timer/counters (A, B, C, D, and E). Block diagrams of the timers are shown in figures 27, 28, 30, and 33.

**Prescaler S:** Eleven-bit counter that inputs a system clock signal. After being initialized to \$000 by MCU reset, prescaler S divides the system clock frequency. Only at MCU reset or during watch and stop modes does prescaler S stop counting. Of the prescaler S outputs, the timer A input

clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and serial mode register (SMR), respectively.

**Prescaler W:** Five-bit counter that inputs the CL<sub>1</sub> input clock signal divided by 8. Prescaler W output can be selected as a timer A input clock by timer mode register A.

**Table 26 Timers A, B, and C Function Selection**

<b>Timer A</b>	
<b>Condition</b>	<b>Function</b>
TMA3 = 0	System clock-base interval timer
TMA3 = 1	Clock time-base

<b>Timer B</b>	
<b>Condition</b>	<b>Function</b>
TMB2–TMB0 ≠ 111	Automatic reloading timer
TMB2–TMB0 = 111 and PMRA3 = 1	Event counter (Pin R7 <sub>1</sub> /INT <sub>1</sub> is specified as INT <sub>1</sub> )

<b>Timer C</b>	
<b>Condition</b>	<b>Function</b>
WDON = 0 (PMRB2 = 1)	Automatic reloading timer (Pin RB <sub>0</sub> /TOC is specified as TOC)
WDON = 1	Watchdog timer

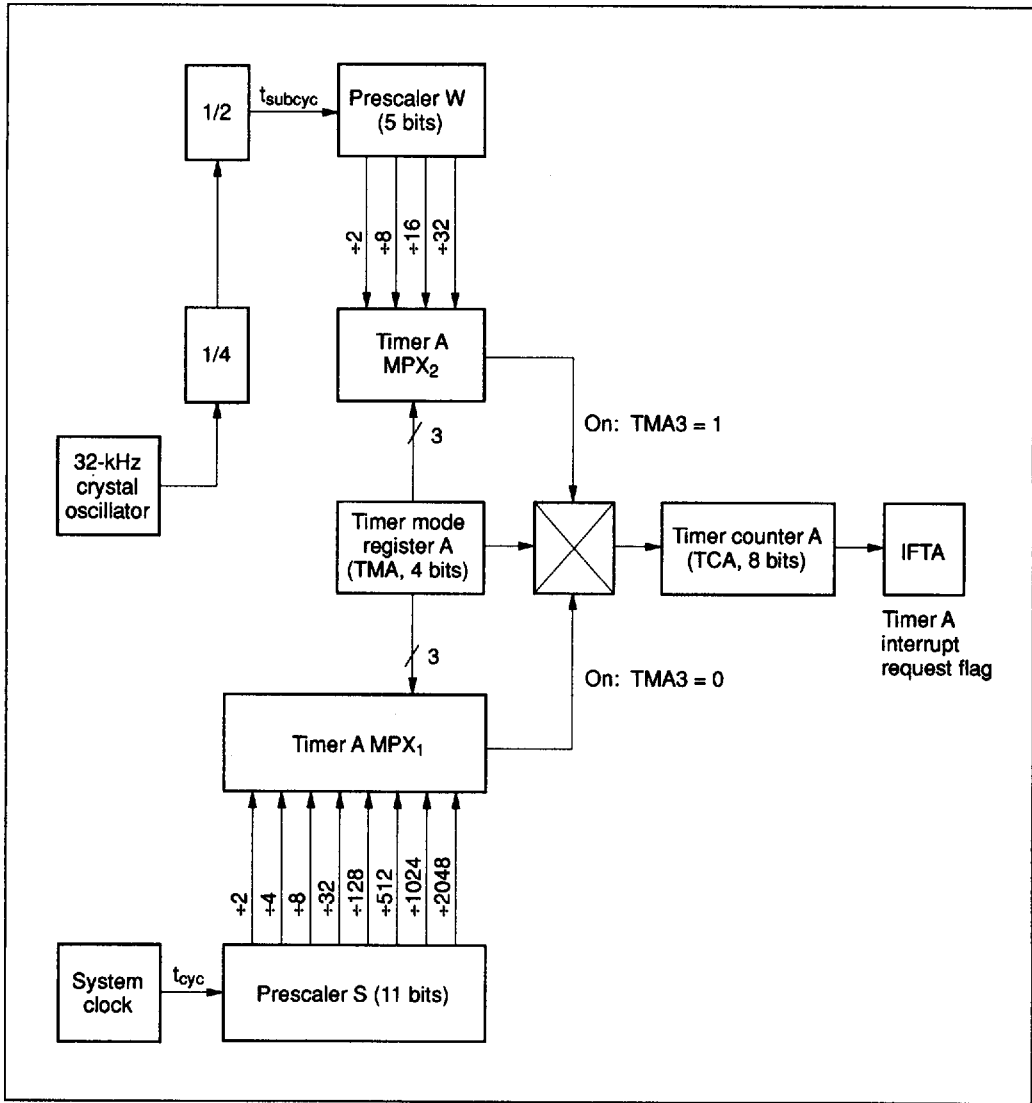


Figure 27 Block Diagram of Timer A

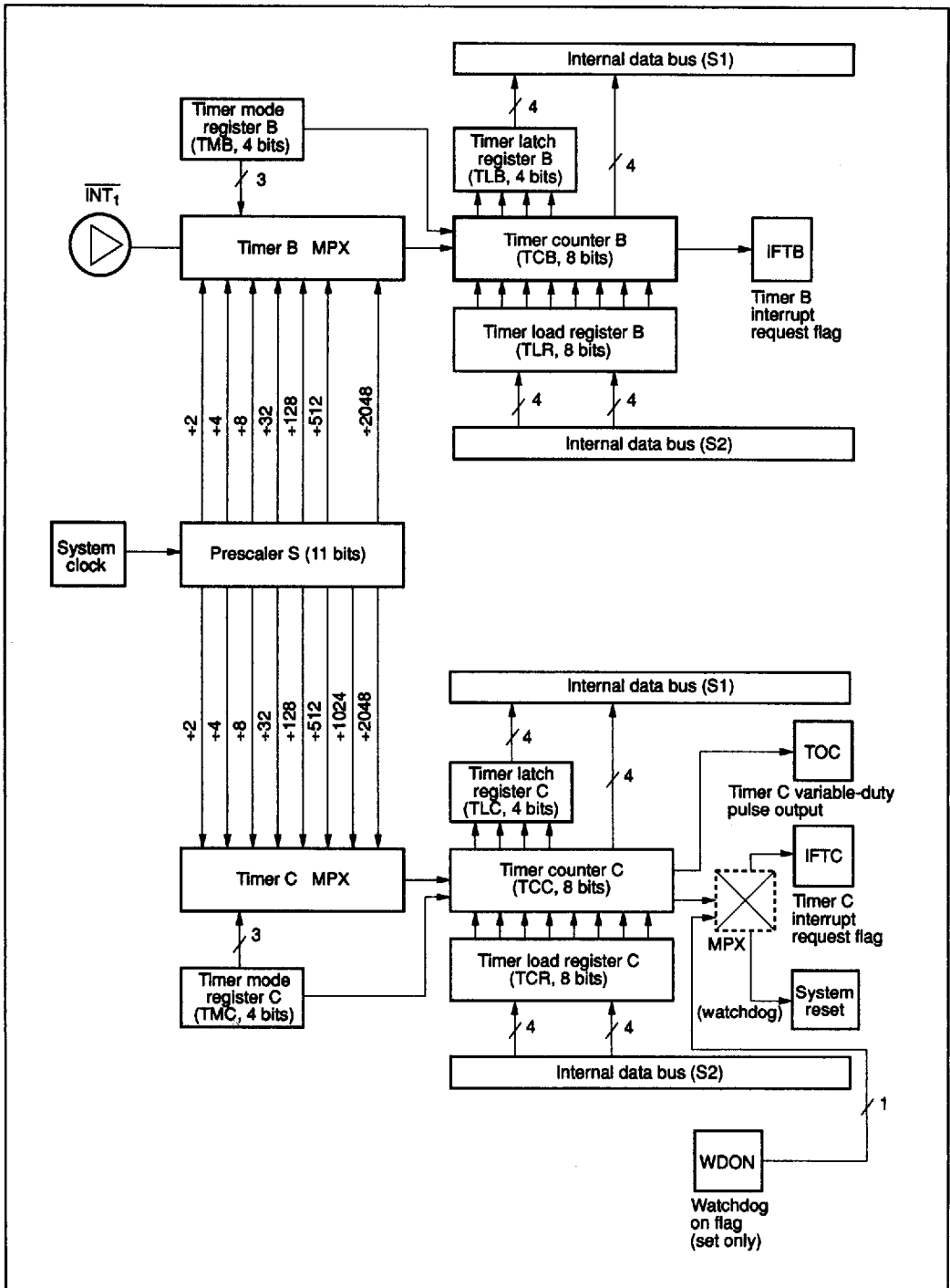


Figure 28 Block Diagram of Timers B and C

## HD404710 Series

**Timer A:** Eight-bit timer which can be used as a clock time-base. Timer A is initialized to \$00 by reset, then incremented by each input clock. If an input clock is applied to timer A after it has reached \$FF, an overflow that sets the timer A interrupt request flag (IFTA: \$002, bit 2) is generated, and timer A restarts from \$00. Timer A is an interval timer which overflows every 256 clock inputs.

Timer A can also be used as a clock time-base when the TMA3 bit of timer mode register A (TMA) is set to 1. The timer is driven by the 32.768-kHz oscillator clock frequency divided by prescaler W. In this case, prescaler W and timer A can be initialized by software. The input clock of timer A is controlled by TMA.

**Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B):** Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

Timer counter B is initialized by writing data to timer load register B (TLR). In this case, the lower digit must be written first. Both the upper and lower digits of TLR are loaded into the timer counter at the same time the upper digit is written to TLR. TLR is initialized to \$00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched at the same time the upper digit is read.

An automatic reloading function, input clock source, and prescaler division ratio of timer B are selected by timer mode register B (TMB). When an external event input is used as the input clock source of timer B, the  $R7_1/\overline{INT}_1$  pin must be specified as  $\overline{INT}_1$  by port mode register A (PMRA: \$004) and the external interrupt mask (IM1) must be set to inhibit any  $\overline{INT}_1$  interrupt request.

Timer B is initialized to the value set in timer load register B (TLR) by software, and is then incremented by one every clock input. If an input clock is applied to timer B after it has reached \$FF, an

overflow is generated. In this case, if the automatic reloading function is enabled, timer B is initialized to its initial value; if reloading is disabled, the timer is initialized to \$00. The overflow sets the timer B interrupt request flag (IFTB: \$003, bit 0).

**Timer C (TCCL: \$00E, TCCU: \$00F, TCRL: \$00E, TCRU: \$00F):** Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

An automatic reloading function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in the TMC by software, and is then incremented by one every clock input. If an input clock is applied to timer C after it has reached \$FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer C is initialized to its initial value; if the function is disabled, the timer is initialized to \$00. The overflow sets the timer C interrupt request flag (IFTC: \$003, bit 2).

Timer C also functions as a watchdog timer. The watchdog timer functions while the watchdog on flag (WDON) is set, and the MCU is reset by an overflow from timer C. If a program routine goes out of control, it can be detected by controlling the timer C reset before the count has reached \$FF. Only a 1 can be written to the watchdog on flag. It can be cleared to 0 only by an MCU reset; it cannot be cleared by writing 0.

Timer C has a variable-duty pulse output (TOC) whose output waveform depends on the status of timer mode register C (TMC) and timer load register C (TCR) as shown in figure 29. For pulse output, the  $RB_0/TOC$  pins must be specified as TOC by port mode register B (PMRB).

**Timer Mode Register A (TMA: \$008):** Four-bit write-only register which controls timer A as shown in table 27. It is initialized to \$0 by MCU reset.

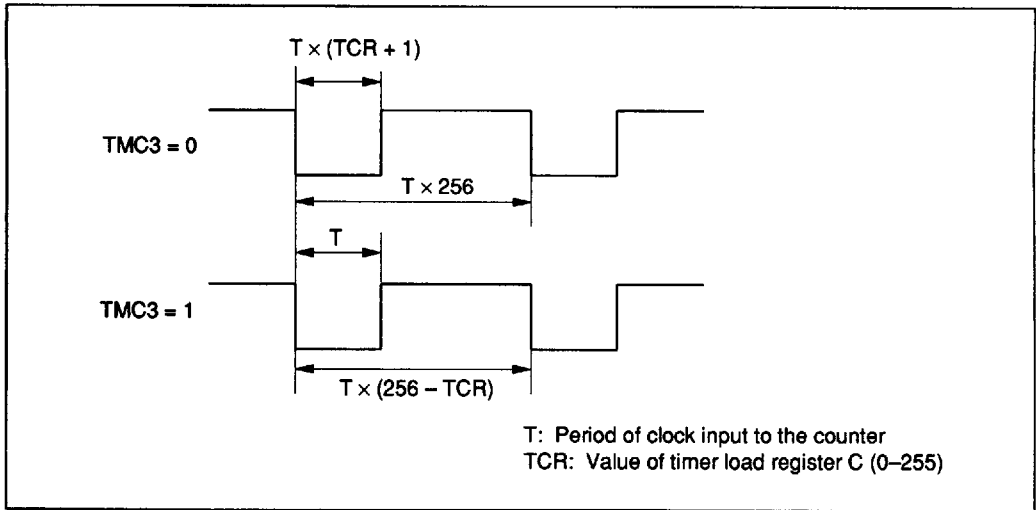


Figure 29 Variable-Duty Pulse Output Waveform

Table 27 Timer Mode Register A

TMA				Source Prescaler, Input Clock Period, Operating Mode	
Bit 3	Bit 2	Bit 1	Bit 0		
0	0	0	0	PSS, 2048 $t_{cyc}$	Timer A mode
			1	PSS, 1024 $t_{cyc}$	
		1	0	PSS, 512 $t_{cyc}$	
			1	PSS, 128 $t_{cyc}$	
	1	0	0	PSS, 32 $t_{cyc}$	
			1	PSS, 8 $t_{cyc}$	
		1	0	PSS, 4 $t_{cyc}$	
			1	PSS, 2 $t_{cyc}$	
1	0	0	0	PSW, 32 $t_{subcyc}$	Time-base mode
			1	PSW, 16 $t_{subcyc}$	
		1	0	PSW, 8 $t_{subcyc}$	
			1	PSW, 2 $t_{subcyc}$	
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

- Notes: 1.  $t_{subcyc} = 244.14 \mu s$  (when a 32.768-kHz crystal oscillator is used)  
 2.  $t_{cyc} = 0.9536 \mu s$  (when a 4.1943-MHz crystal oscillator is used)  
 3. Timer counter overflow output period(s) = Input clock period(s)  $\times$  256  
 4. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

## HD404710 Series

**Timer Mode Register B (TMB: \$009):** Four-bit write-only register which selects the automatic reloading function, input clock source, and the prescaler division ratio for timer B as shown in table 28. It is initialized to \$0 by MCU reset.

Changes made to TMB are valid from the second instruction cycle after the write instruction is executed. Timer B must be programmed so that it is initialized by a write instruction to timer load register B (TLR) after a mode change becomes valid.

**Table 28 Timer Mode Register B**

### TMB

Bit 3	Automatic Reloading
0	Disabled
1	Enabled

### TMB

Bit 2	Bit 1	Bit 0	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
0	0	1	$512t_{cyc}$
0	1	0	$128t_{cyc}$
0	1	1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
1	0	1	$4t_{cyc}$
1	1	0	$2t_{cyc}$
1	1	1	$\overline{INT}_1$ (external event input)

Note:  $t_{cyc} = 0.9536 \mu s$  (when a 4.1943-MHz crystal oscillator with 1/4 division is used)



**Timer Mode Register C (TMC: \$00D):** Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer C as shown in table 29. It is initialized to \$0 by MCU reset.

Changes made to TMC are valid from the second instruction cycle after the write instruction is executed. Timer C must be programmed so that it is initialized by a write instruction to timer load register C (TCR) after a mode change becomes valid.

**Table 29 Timer Mode Register C**

**TMC**

Bit 3	Automatic Reloading
0	Disabled
1	Enabled

**TMC**

Bit 2	Bit 1	Bit 0	Input Clock Period
0	0	0	2048 $t_{cyc}$
0	0	1	1024 $t_{cyc}$
0	1	0	512 $t_{cyc}$
0	1	1	128 $t_{cyc}$
1	0	0	32 $t_{cyc}$
1	0	1	8 $t_{cyc}$
1	1	0	4 $t_{cyc}$
1	1	1	2 $t_{cyc}$

Note:  $t_{cyc} = 0.9536 \mu s$  (when a 4.1943-MHz crystal oscillator with 1/4 division is used)

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**Timer D (TCDL: \$011, TCDU: \$012, TDRL: \$011, TDRU: \$012):** Eight-bit write-only timer load register (TDRL and TDRU) and read-only timer counter (TCDL and TCDU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

An automatic reloading function and prescaler division ratio of timer D are selected by timer mode register D (TMD). Timer D is initialized to the value set in timer load register D (TDR) by software, and is then incremented by one every clock input. If an input clock is applied to timer D after it has reached \$FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer D is initialized to its initial value; if reloading is disabled, the timer is initialized to \$00. The overflow sets the timer D interrupt request flag (IFTD: \$021, bit 0).

Timer D has a variable-duty pulse output (TOD), whose output waveform depends on the states of timer mode register D (TMD) and timer load register D (TDR) as shown in figure 31. For pulse output, the RB<sub>1</sub>/TOD pin must be specified as TOD by port mode register B (PMRB).

**Timer Mode Register D (TMD: \$010):** Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer D as shown in figure 32. It is initialized to \$0 by MCU reset.

Changes made to TMD are valid from the second instruction cycle after the write instruction is executed. Timer D must be programmed so that it is initialized by a write instruction to timer load register D (TDR) after a mode change becomes valid.

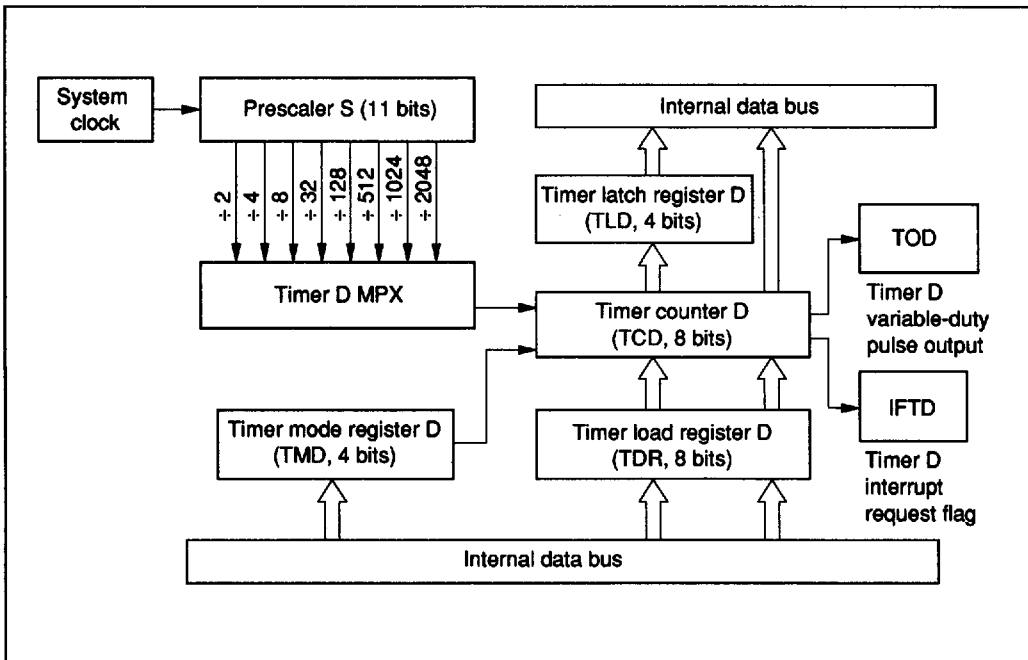


Figure 30 Block Diagram of Timer D

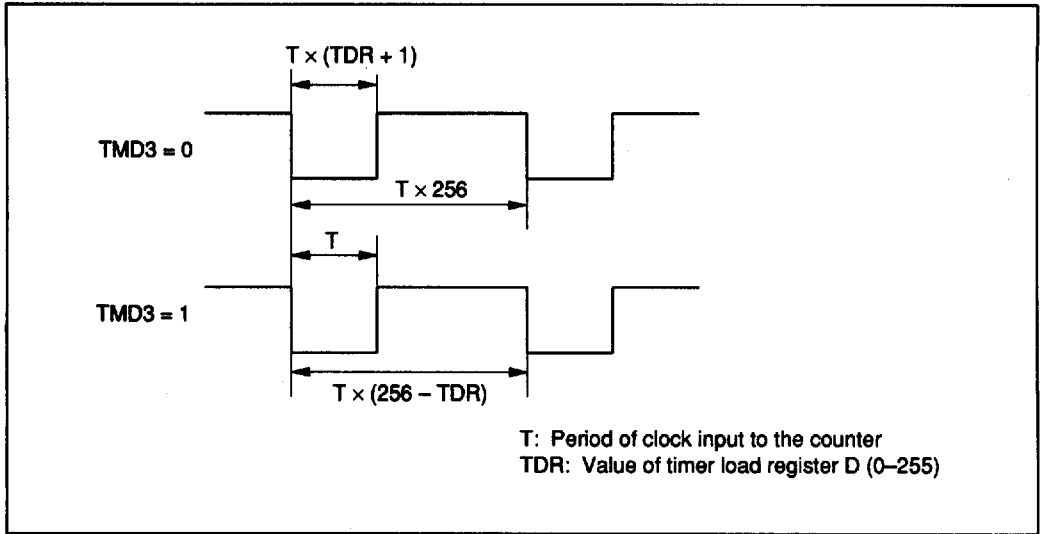


Figure 31 Variable-Duty Pulse Output Waveform

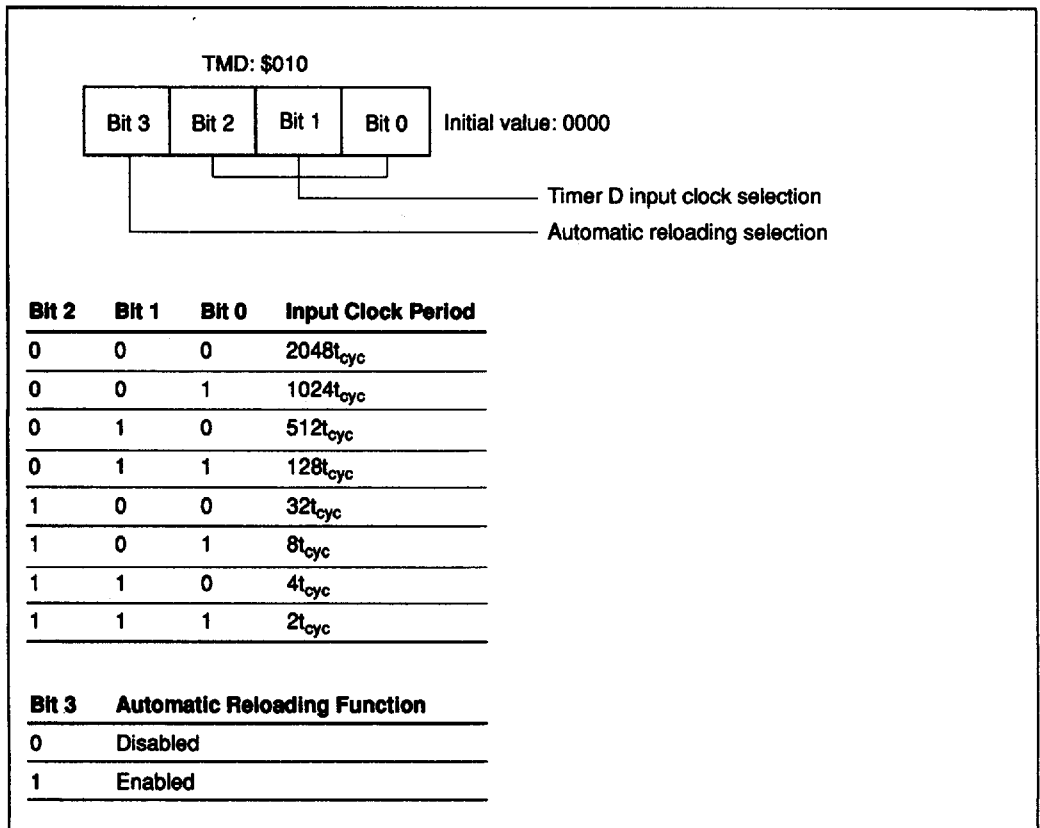


Figure 32 Timer Mode Register D

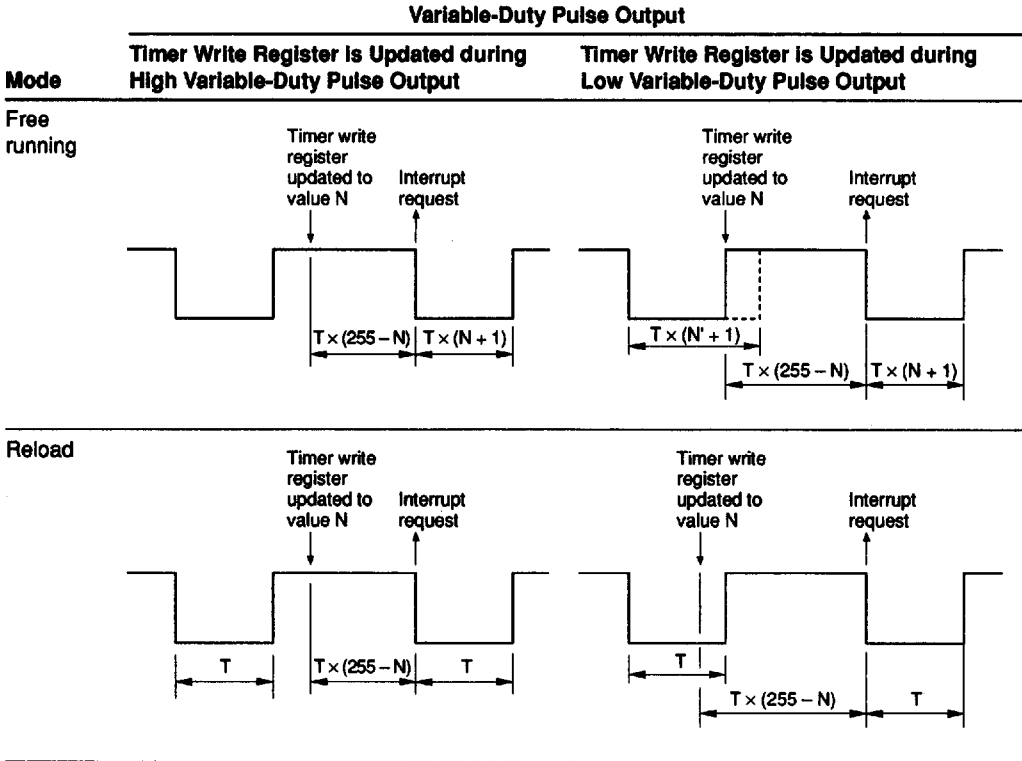
# HD404710 Series

## Notes on Use

When using the timer output as variable-duty pulse output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the variable-duty pulse output differs from the period and duty settings, as

shown in table 30. The variable-duty pulse output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the variable-duty pulse output will have the set period and duty cycle.

**Table 30 Variable-Duty Pulse Output Following Update of Timer Write Register**



**Timer E:** Outputs two variable-duty pulses (PWM). The block diagram is shown in figure 33. The duty ratio can be selected by the setting of the load register (figure 34). To write data into the load register, timer buffer register E must be written to first. Data written to the buffer register is transferred to the load register by an overflow from the prescaler. Since the two channels use the same buffer register, the destination load register is selected by the bit 2 setting of the timer mode register (TME). The completion of data transfer from the buffer register to the load register can be checked by reading bit 3 of TME.

**Timer Mode Register E (TME: \$025):** Four-bit register including three write-only bits and one read-only bit which selects the port and the load register and indicates the buffer register status (figure 35).

**Timer Buffer Register E (TBEL: \$026, TBEU: \$027):** Eight-bit write-only register. The lower digit must be written first. When the upper digit is written, bit 3 of timer mode register E is automatically set to 1. When the data in timer mode register E is loaded to the load register, bit 3 of timer mode register E is automatically reset to 0.

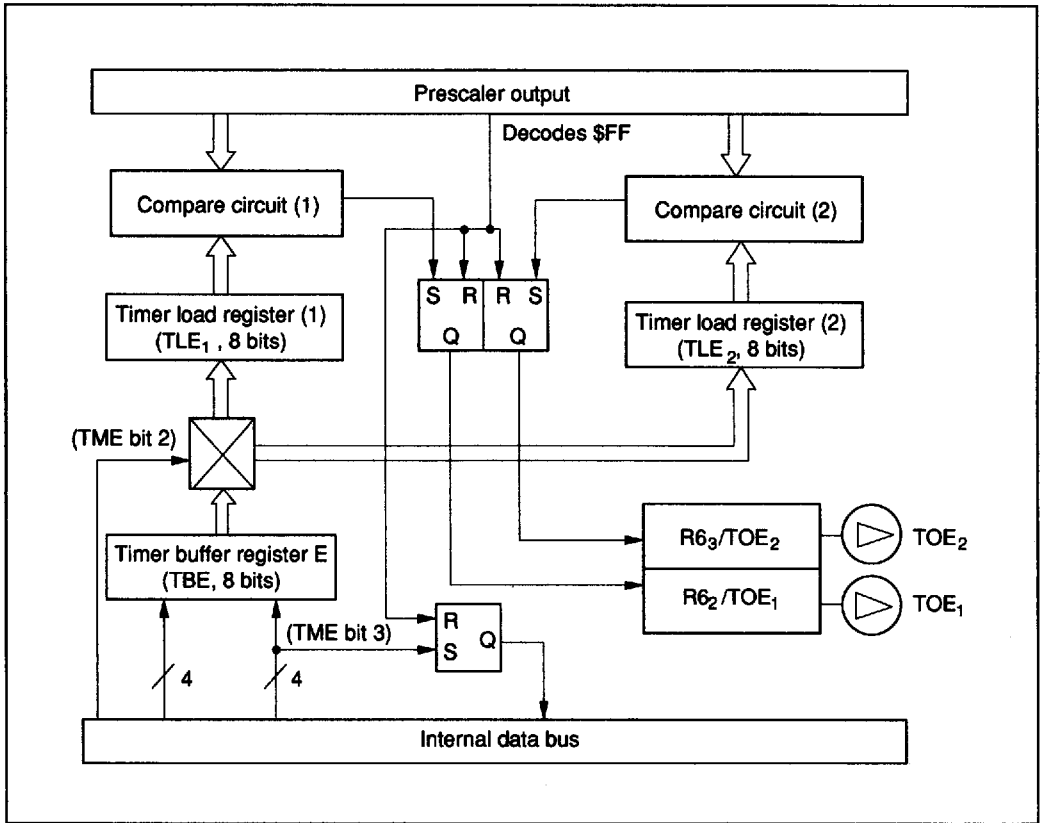


Figure 33 Block Diagram of Timer E

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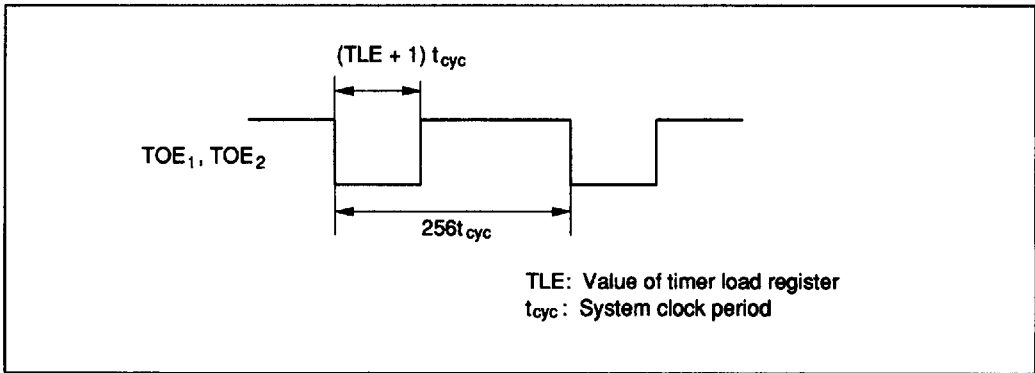


Figure 34 Variable-Duty Pulse Output Waveform

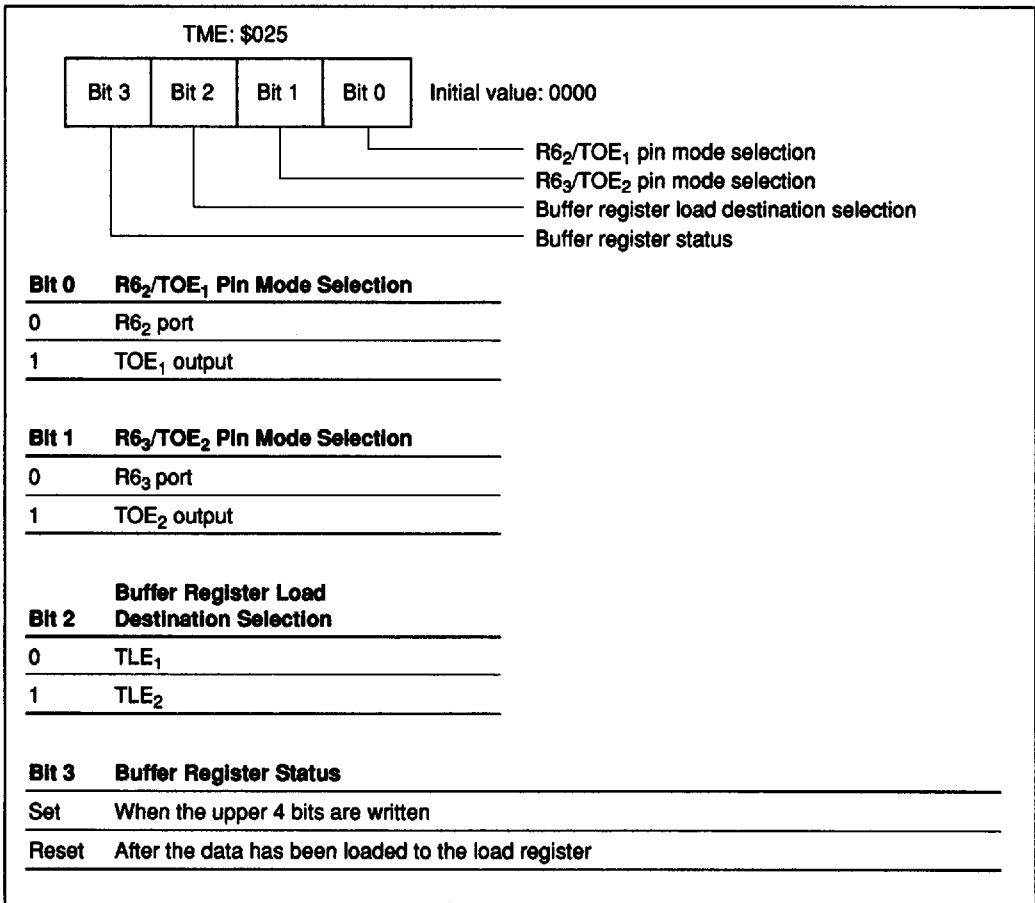


Figure 35 Timer Mode Register E

**Input Capture Timer:** Eight-bit counter and 8-bit input capture register. The block diagram is shown in figure 36. Free-running counter operation or input capture operation can be selected by setting the input capture status register.

When the free-running counter operation is selected, the counter is incremented by one every prescaler clock input, whose division ratio is specified by the input capture control register. If an overflow is generated from the counter, the input capture interrupt request flag is set, and the counter is initialized to \$00. It is then incremented.

When the input capture operation is selected, the count of the 8-bit counter is loaded into the input capture register by every trigger edge input of  $ICT_0$  or  $ICT_1$ . At this point, the input capture interrupt request flag and input capture status flag are set and the counter is initialized to \$00, and is

then incremented. An external trigger input while the status flag is 1 or an overflow from the counter (when the counter continues to increment without receiving trigger input) sets bit 3 of the status register.

**Input Capture Control Register (ICC: \$017):** Four-bit write-only register which selects the pin function and the prescaler division ratio (figure 37).

**Input Capture Status Register (ICSR: \$018):** Four-bit register which selects the input capture operation and the trigger input edge, and holds the operation status (figure 38).

**Input Capture Register (ICRL: \$019, ICRU: \$01A):** Eight-bit read-only register which loads the contents of the counter by a trigger edge input of  $ICT_0$  or  $ICT_1$ .

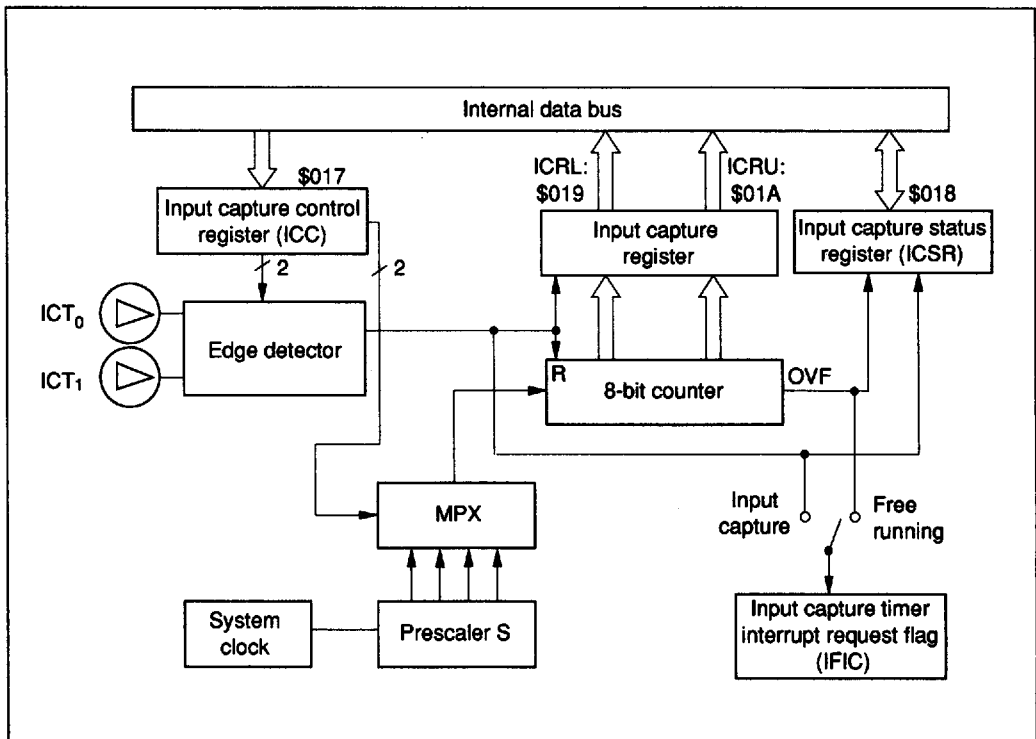
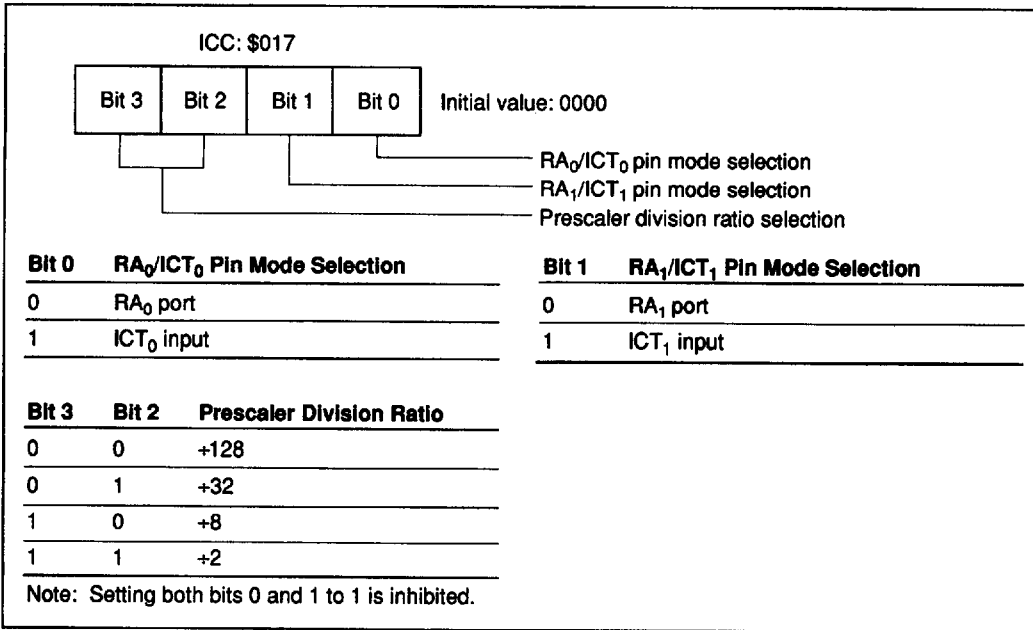
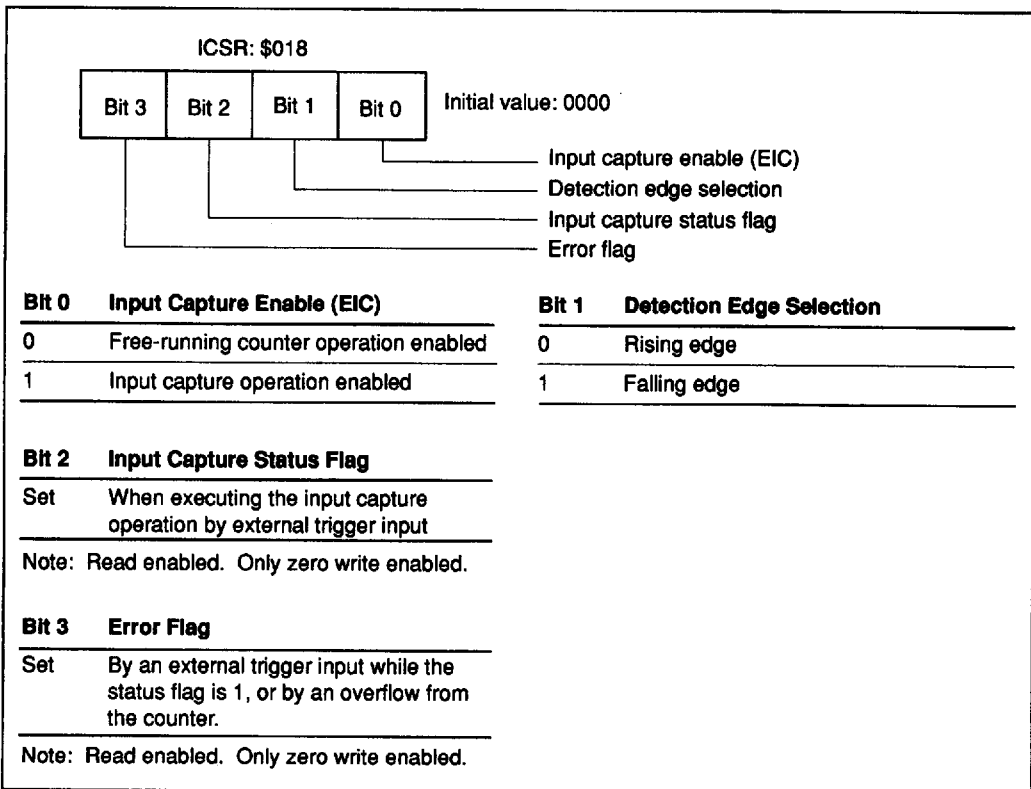


Figure 36 Block Diagram of Input Capture Timer



**Figure 37 Input Capture Control Register**



**Figure 38 Input Capture Status Register**



**Output Compare Timer:** Sixteen-bit counter and 16-bit register. The output compare timer outputs a wave whose form changes at a specified timing. This timing to change the waveform can be selected as an overflow from the 16-bit counter, an input edge of  $\overline{INT}_4$ , or a trigger by software. An output of 1, an output of 0, or a toggle (inversion of the previous output value) can be selected as the output of pin TOG. The block diagram is shown in figure 39.

Timer counter G, the counter for output compare, is a 16-bit counter. The system clock or the system clock divided by 2 can be selected as the clock

source. Timer counter G is a reloading counter. At the time of a counter overflow, an  $\overline{INT}_4$  edge input or a software trigger, and the contents of timer load register G are loaded into timer counter G. An output compare interrupt is generated at the falling edge of  $\overline{INT}_4$  or a counter overflow, depending on the selection set with bit 3 of the output compare control register.

When selecting a software trigger, set both bits 2 and 3 of the output compare control register to 1 (figure 40). At the same time the bits are set, pin TOG outputs a specified value and the contents of the load register are loaded into the counter.

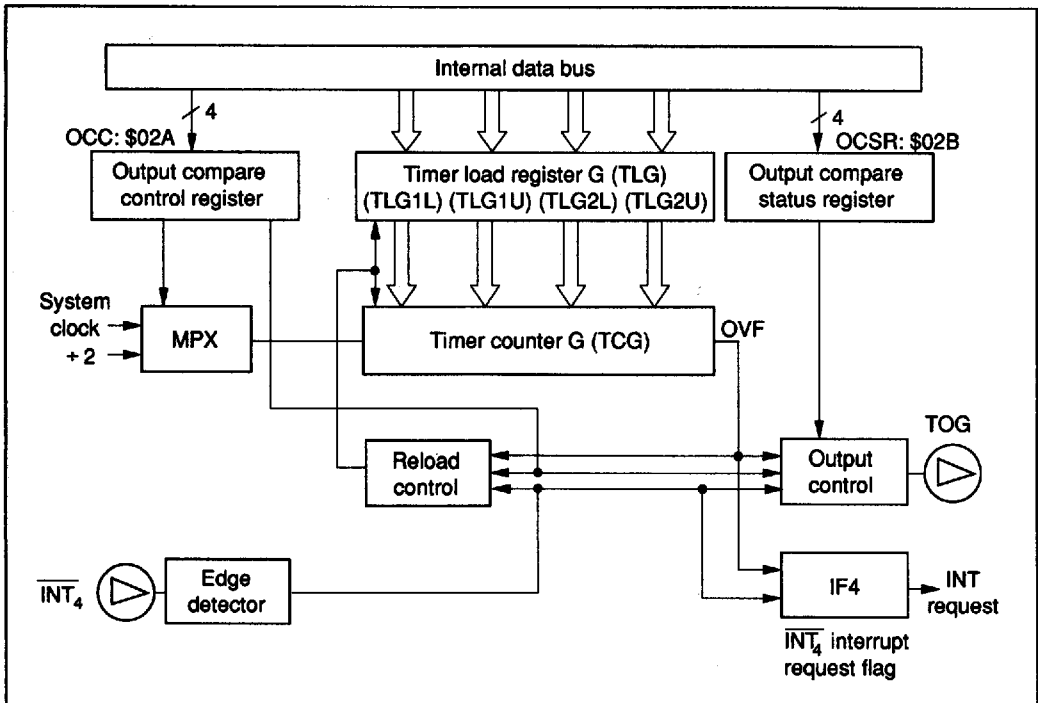
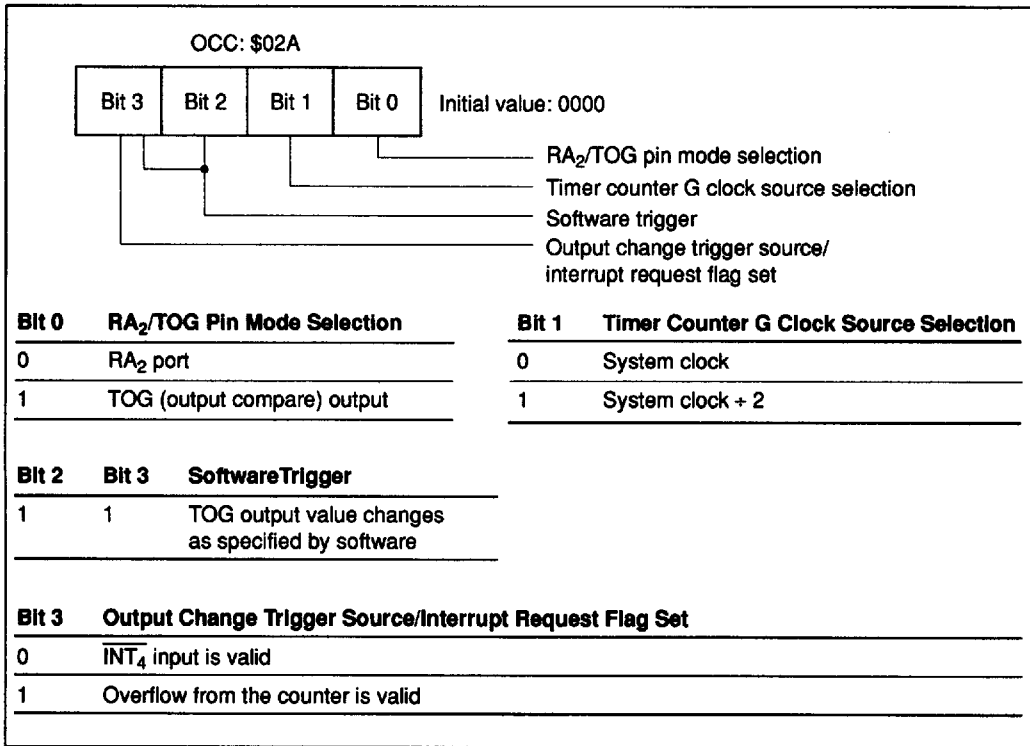
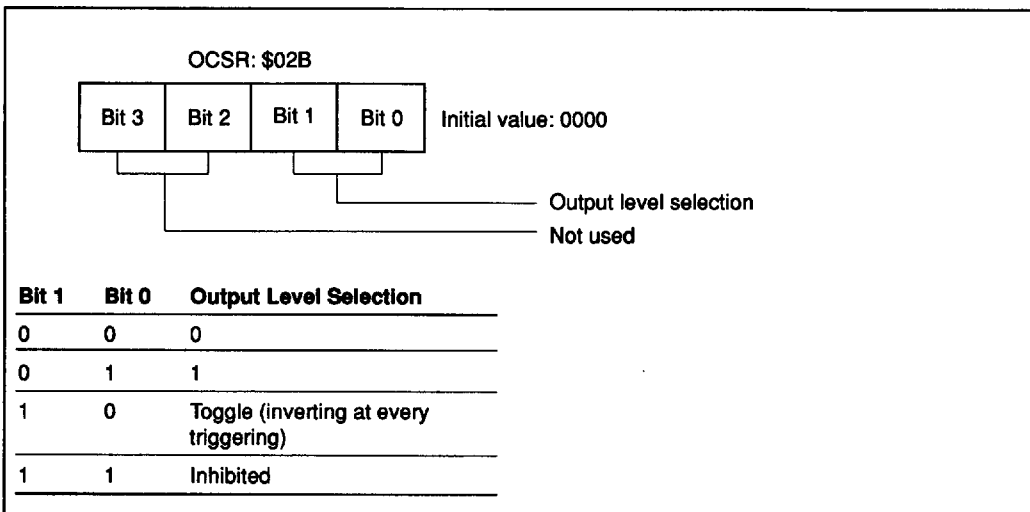


Figure 39 Block Diagram of Output Compare Timer

# HD404710 Series



**Figure 40 Output Compare Control Register**

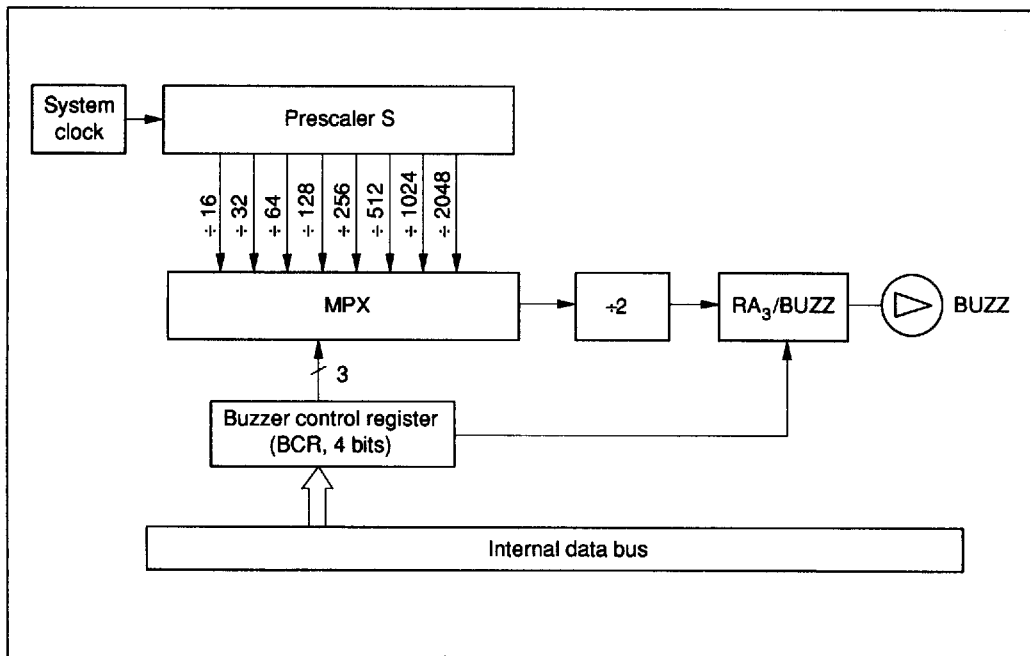


**Figure 41 Output Compare Status Register**

**Buzzer**

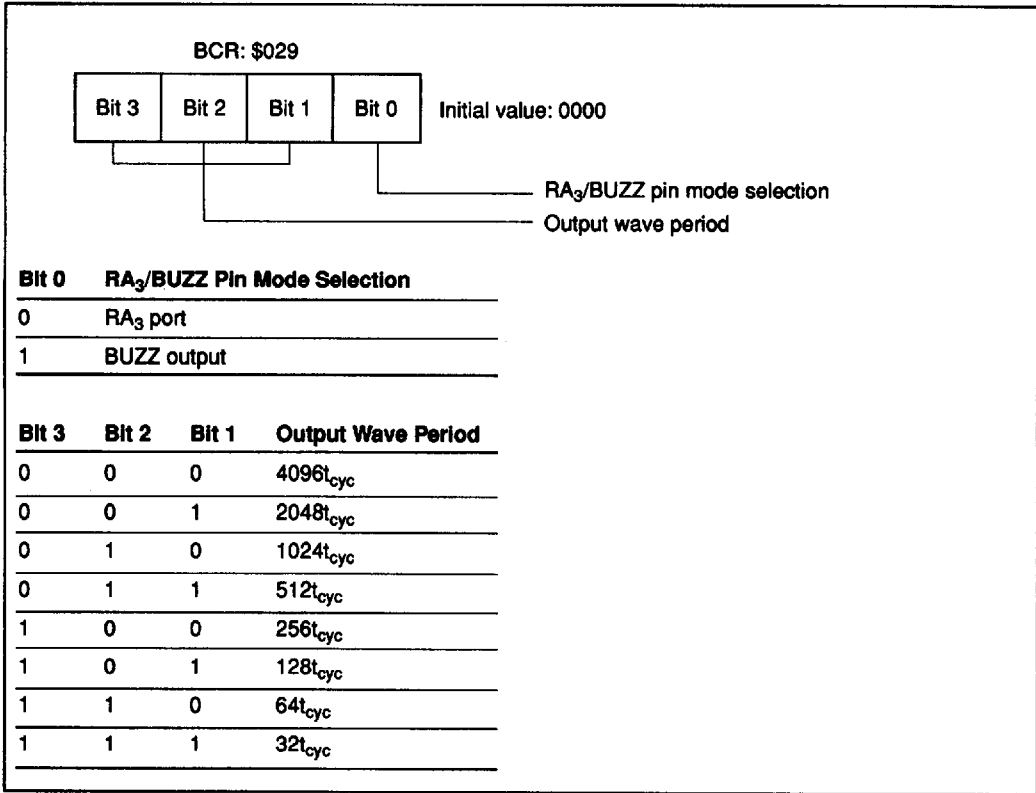
**Buzzer Output Function:** Outputs a wave which has a duty ratio of 50% of the clock rate specified by the buzzer control register (BCR). To output a buzzer, the RA<sub>3</sub>/BUZZ pin must be fixed as BUZZ by setting bit 3 of the buzzer control register. The block diagram of buzzer output is shown in figure 42.

**Buzzer Control Register (BCR: \$029):** Four-bit write-only register which selects the port and the output wave frequency (figure 43).



**Figure 42 Block Diagram of Buzzer Output**

# HD404710 Series



**Figure 43 Buzzer Control Register**

**Serial Interface**

The MCU has two clock-synchronous 8-bit serial interfaces (serial interfaces 1 and 2). The clock source is a prescaler, which is also used by the timers.

**Serial Interface 1:** Used to serially transmit and receive 8-bit data. It consists of serial data register 1 (SR1), serial mode register 1 (SMR1), port mode register A (PMRA), an octal counter, and a multiplexer as shown in figure 44. The  $R9_0/\overline{SCK}_1$  pin and the transmit clock are controlled by writing data to SMR1. The transmit clock shifts the con-

tents of SR1, which can be read and written to by software. In this way, 8-bit data is transferred.

Serial interface 1 is activated by the STS instruction. The octal counter is reset to \$0 by the STS instruction, it starts counting at the falling edge of the transmit clock ( $\overline{SCK}_1$ ), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 1 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 1 interrupt request flag (IFS1) is set.

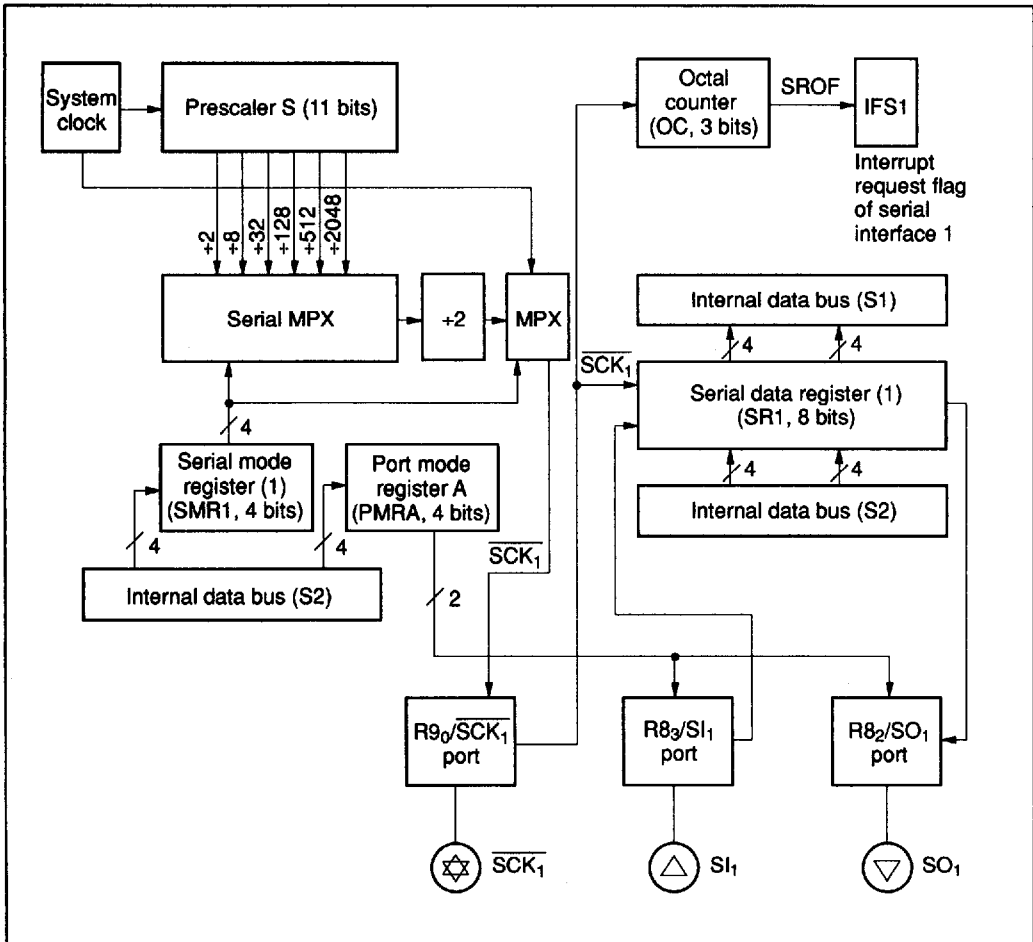


Figure 44 Serial Interface 1 Block Diagram

## HD404710 Series

**Serial Mode Register 1 (SMR1: \$005):** Four-bit write-only register which controls the  $R9_0/\overline{SCK}_1$  pin, transmit clock, and prescaler division ratio for serial interface 1 as shown in figure 45. Writing to SMR1 initializes serial interface 1.

A write signal input to SMR1 discontinues the input of the transmit clock to serial data register 1 (SR1) and the octal counter. Therefore, if a write occurs during data transmission, the octal counter

is reset to \$0 to stop transmission, and, at the same time, the serial 1 interrupt request flag (IFS1) is set.

The contents of the serial mode register are not valid until the second instruction cycle after the write instruction execution. The user must program the STS instruction to be executed after this instruction cycle. The serial mode register is initialized to \$0 by the MCU reset.

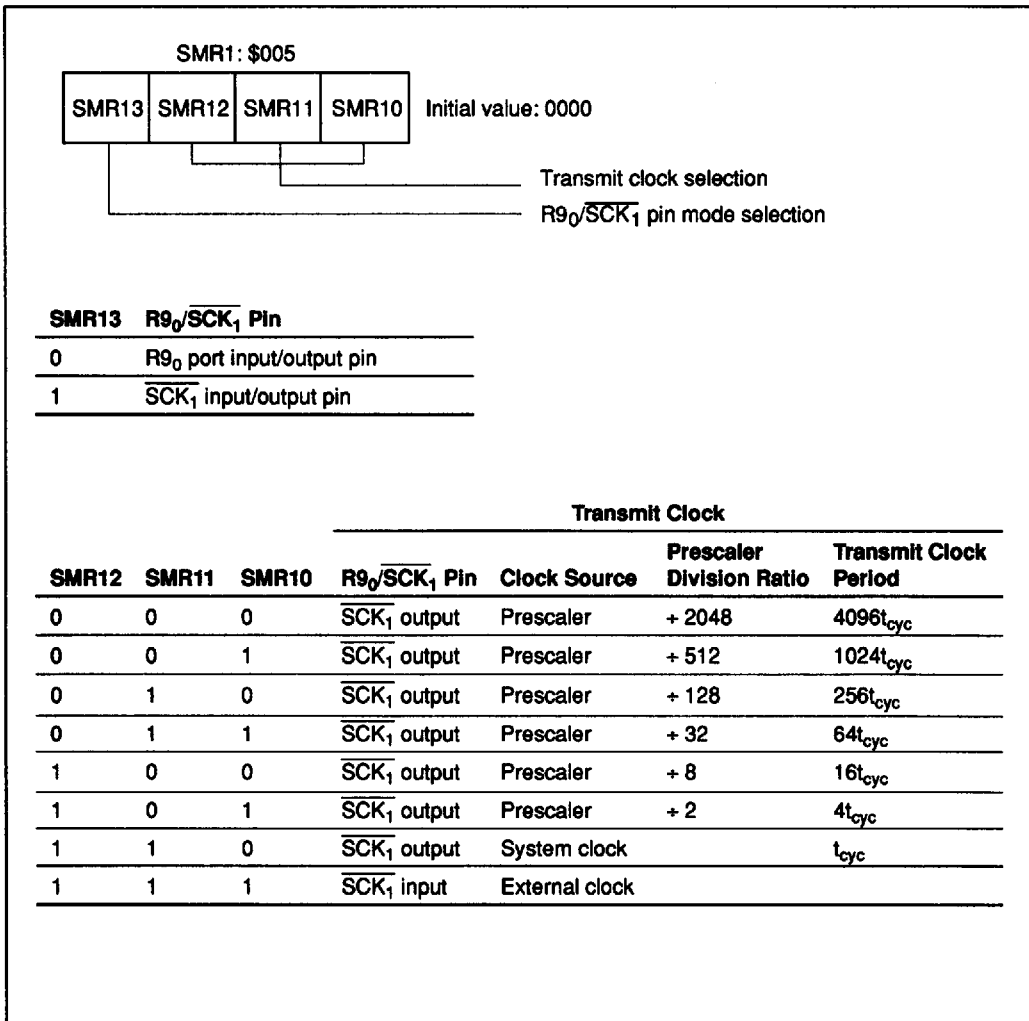


Figure 45 Serial Mode Register 1

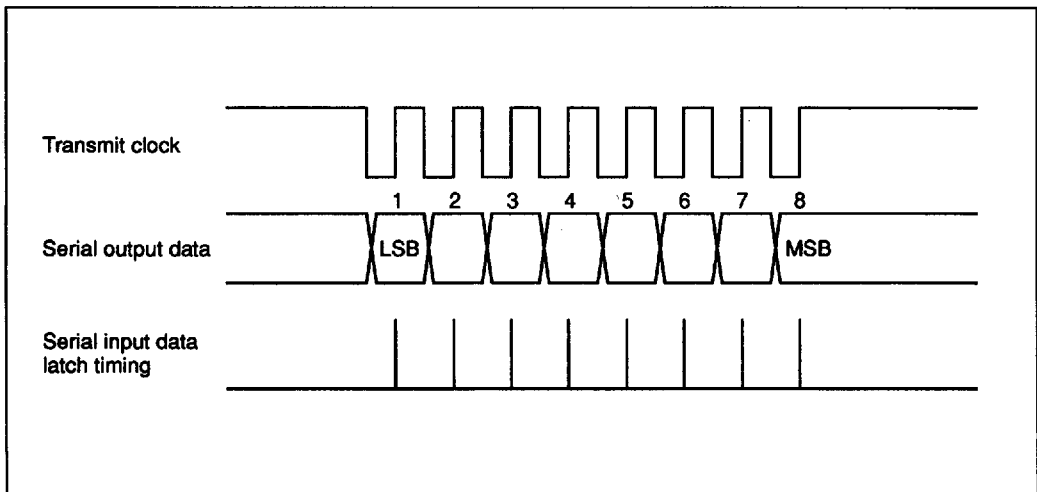
**Serial Data Register 1 (SR1L: \$006, SR1U: \$007):** Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO<sub>1</sub> pin LSB first, synchronously with the falling edge of the transmit clock, and data is input LSB first to the SI<sub>1</sub> pin at the rising edge of the transmit clock. Input/output timing is shown in figure 46.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

**Selecting and Changing Operating Modes:** The operating modes of serial interface 1 are shown in table 31. The combination of port mode register A (PMRA) and serial mode register 1 (SMR1) must be specified as shown in the table. To change the operating mode of serial interface 1, internally initialize serial interface 1 by writing to SMR1.

**Table 31 Operating Modes of Serial Interface 1**

SMR1 Bit 3	PMRA		Operating Mode
	Bit 1	Bit 0	
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode



**Figure 46 Serial Interface 1 Timing**

## HD404710 Series

**Serial Interface 1 Operation:** Three operating modes are provided for serial interface 1; transitions between them are shown in figure 47.

In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed, serial interface 1 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts serial data register 1 (SR1), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and serial interface 1 enters transmit clock wait state. If an external transmit clock is further applied, serial interface 1 enters the transfer state. In this state, if the internal clock has been selected, the serial 1 interrupt flag is set, serial interface 1 enters STS instruction wait state, and serial transmission is stopped after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, serial mode register 1 (SMR1) must be written to, to initialize serial interface 1, after which serial interface 1 enters STS wait state.

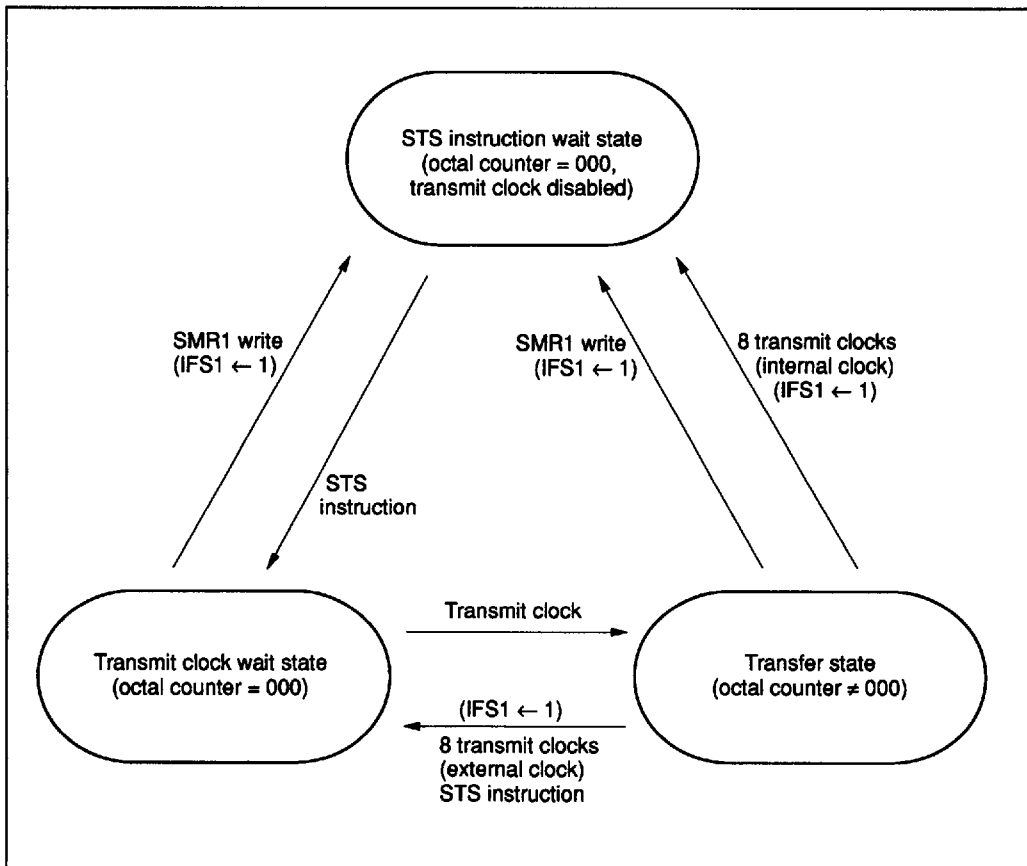


Figure 47 Serial Interface 1 Mode Transitions



**Transmit Clock Error Detection:** Serial interface 1 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock. Such errors can be detected as shown in figure 48.

changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 1 is set to STS wait state by writing data to SMR1 during transmission after the serial 1 interrupt request flag (IFS1) has been reset, the flag is set again.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 1's state

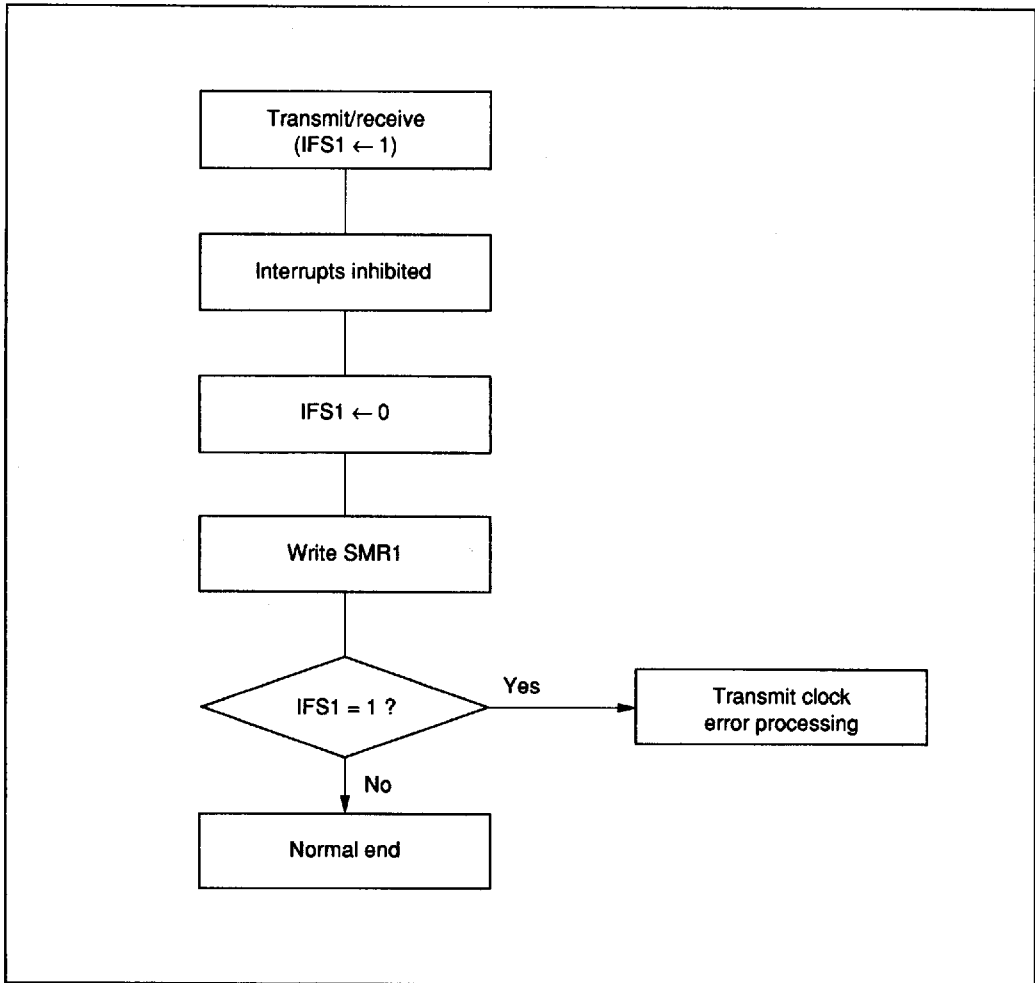


Figure 48 Transmit Clock Error Detection

## HD404710 Series

**Serial Interface 2:** Used to serially transmit and receive 8-bit data. It consists of serial data register 2 (SR2), serial mode register 2 (SMR2), port mode register B (PMRB), an octal counter, and a multiplexer as shown in figure 49. The  $R9_1/\overline{SCK}_2$  pin and the transmit clock are controlled by writing data to SMR2. The transmit clock shifts the contents of the SR2, which can be read and written to by software, and then transmission starts between two MCUs.

Serial interface 2 is activated by a read instruction for SMR2. The octal counter is reset to \$0 by the

read instruction for SMR2, it starts counting at the falling edge of the transmit clock ( $\overline{SCK}_2$ ), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 2 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 2 interrupt request flag (IFS2) is set.

To start serial interface 2 by an SMR2 read, execute a compare instruction on SMR2 and the accumulator. Note that 0000 is read when write-only register SMR2 is accessed.

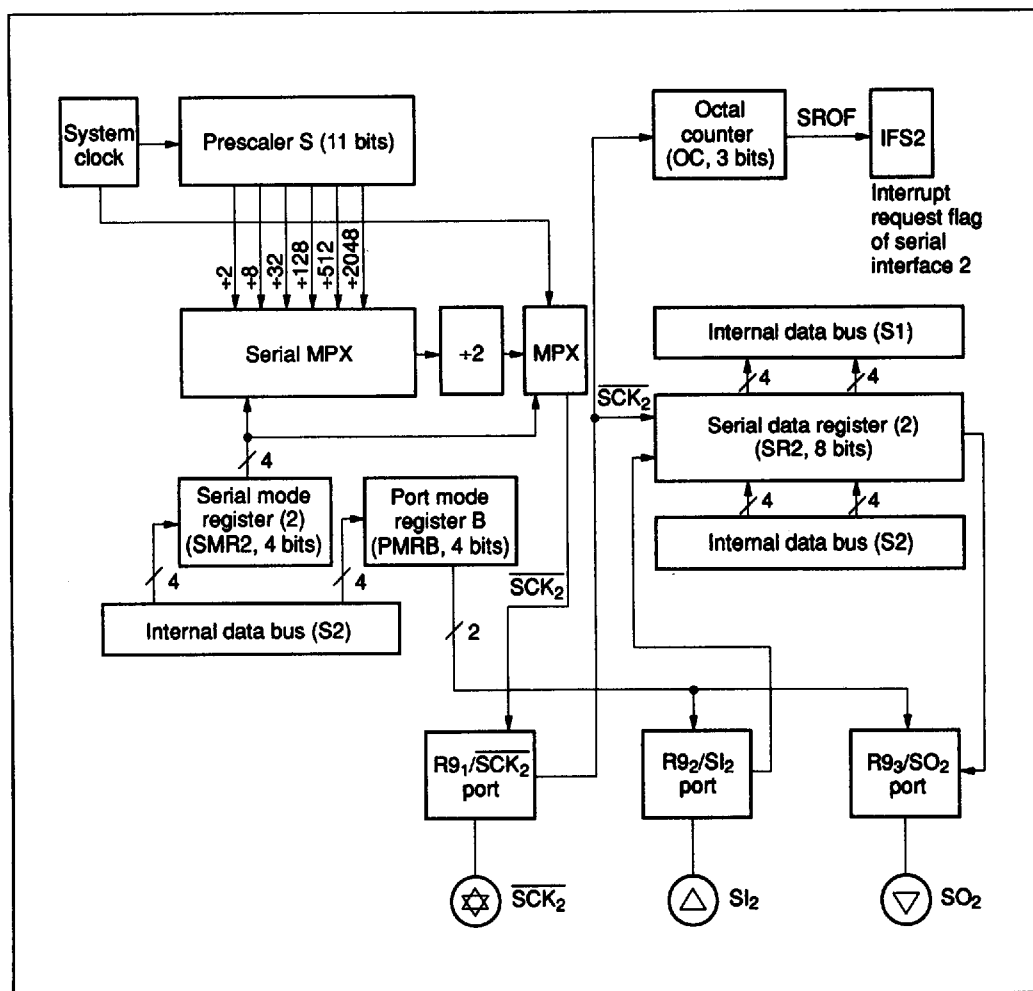


Figure 49 Serial Interface 2 Block Diagram

**Serial Mode Register 2 (SMR2: \$014):** Four-bit write-only register which controls the  $R9_1/\overline{SCK}_2$  pin, transmit clock, and prescaler division ratio as shown in figure 50. Writing to SMR2 initializes serial interface 2.

A write signal input to SMR2 discontinues the input of the transmit clock to serial data register 2 (SR2) and the octal counter. Therefore, if a write occurs during data transmission, the octal

counter is reset to \$0 to stop transmission, and, at the same time, the serial 2 interrupt request flag (IFS2) is set.

The contents of the serial mode register are not valid until the second instruction cycle after the write instruction execution. The user must program the SMR2 read instruction to be executed after this instruction cycle. The serial mode register is initialized to \$0 by the MCU reset.

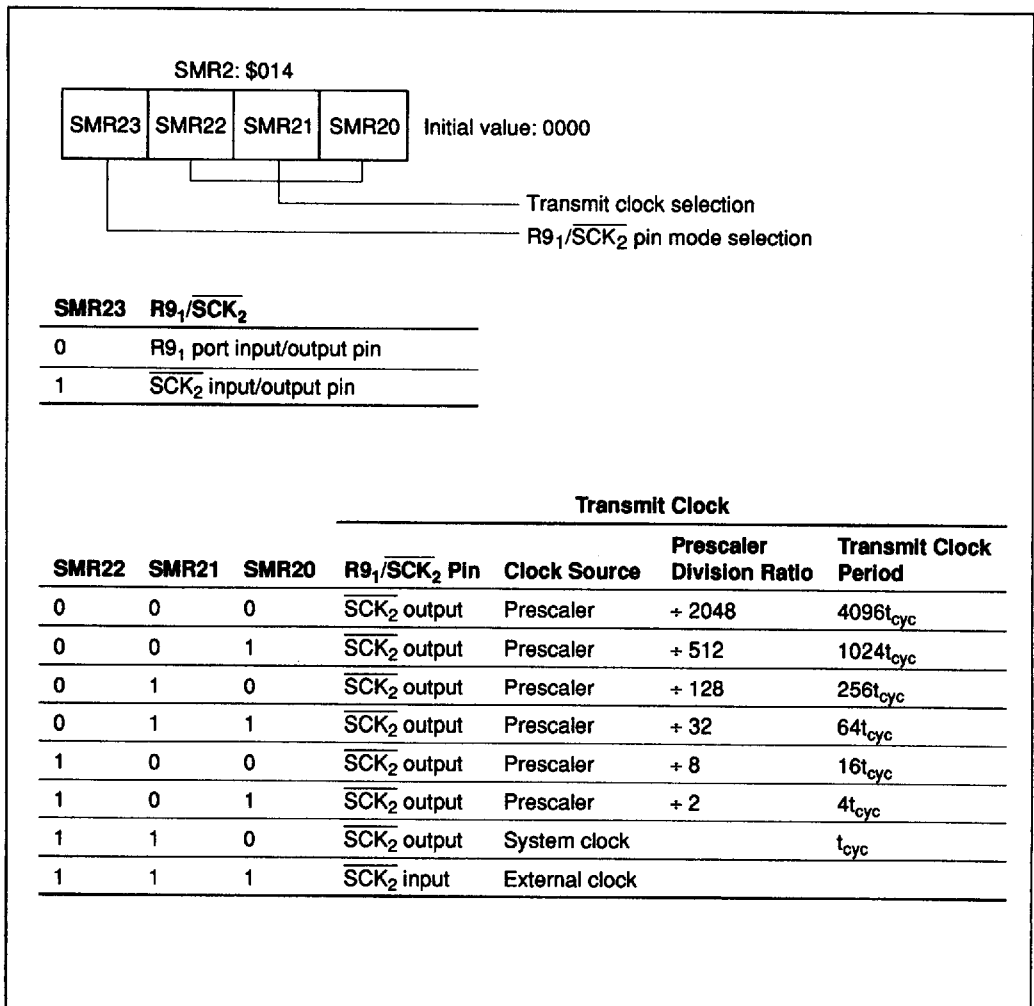


Figure 50 Serial Mode Register 2

## HD404710 Series

**Serial Data Register 2 (SR2L: \$015, SR2U: \$016):** Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO<sub>2</sub> pin LSB first, synchronously with the falling edge of the transmit clock, and data is input LSB first to the SI<sub>2</sub> pin at the rising edge of the transmit clock. Input/output timing is shown in figure 51.

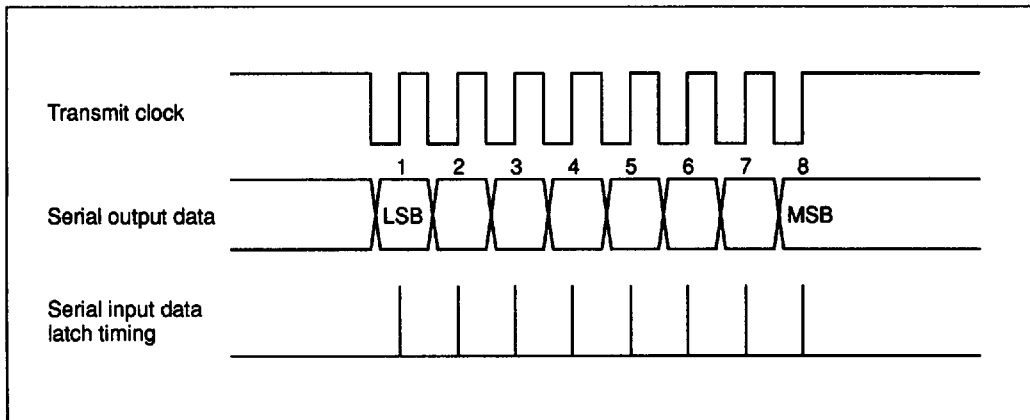
Data cannot be read or written during serial data transmission. If data is read or written during

transmission, it cannot be guaranteed.

**Selecting and Changing Operating Modes:** Table 32 lists the operating modes of serial interface 2. The combination of port mode register B (PMRB) and serial mode register 2 (SMR2) must be specified as shown in the table. To change the operating mode of serial interface 2, internally initialize serial interface 2 by writing to SMR2.

**Table 32 Operating Modes of Serial Interface 2**

SMR2 Bit 3	PMRB		Operating Mode
	Bit 1	Bit 0	
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode



**Figure 51 Serial Interface 2 Timing**

**Serial Interface 2 Operation:** Three operating modes are provided for serial interface 2; transitions between them are shown in figure 52.

In SMR2 read wait state, serial interface 2 is initialized and the transmit clock is ignored. If an SMR2 read is executed, serial interface 2 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts serial data register 2 (SR2), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of 8 clocks or an SMR2 read sets the octal counter to 000, and serial interface 2 enters transmit clock wait state. If an external transmit clock is further applied, serial interface 2 enters transfer state. If the internal clock has been selected, the serial 2 interrupt flag is set, serial interface 2 enters SMR2 read wait state, and serial transmission is stopped after the eighth clock is output.

If port mode register B (PMRB) is written to in transmit clock wait state or during transmission, SMR2 must be written to, to initialize serial interface 2, after which serial interface 2 enters SMR2 read (serial start) wait state.

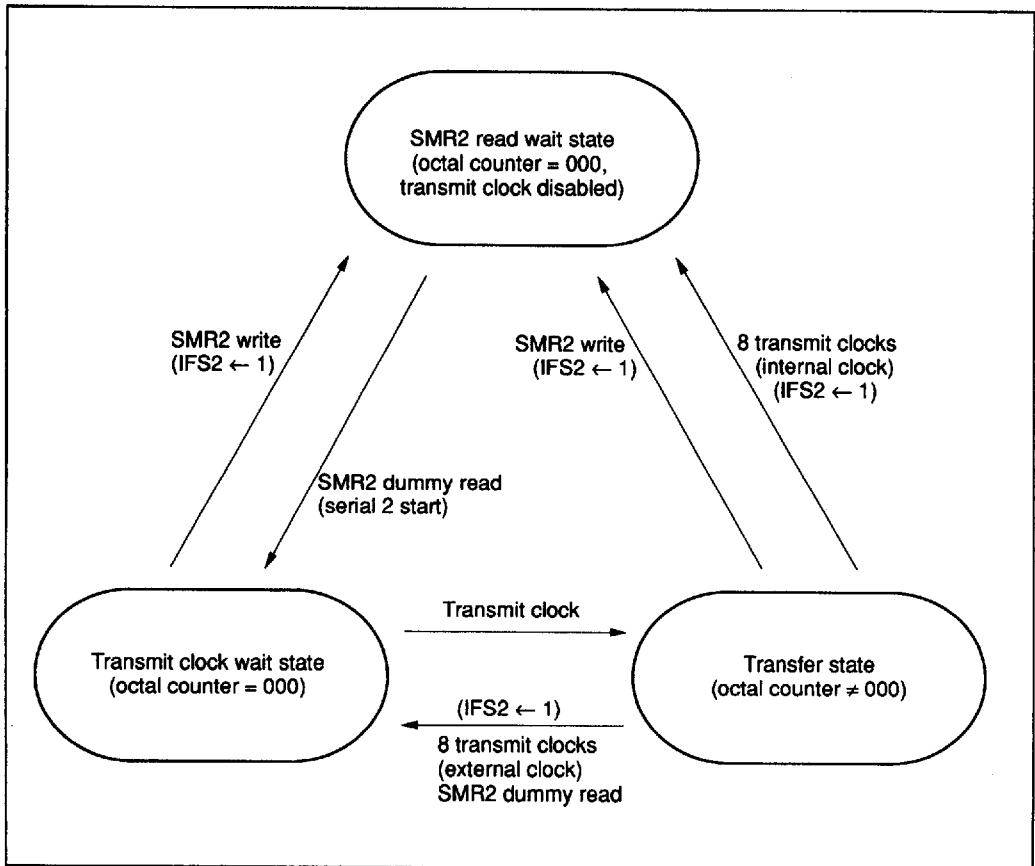


Figure 52 Serial Interface 2 Mode Transitions

## HD404710 Series

**Transmit Clock Error Detection:** Serial interface 2 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock. Such errors can be detected as shown in figure 53.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 2's state

changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 2 is set to SMR2 read wait state by writing data to SMR2 at transfer state after the serial interface 2 interrupt request flag (IFS2) has been reset, the flag is set again.

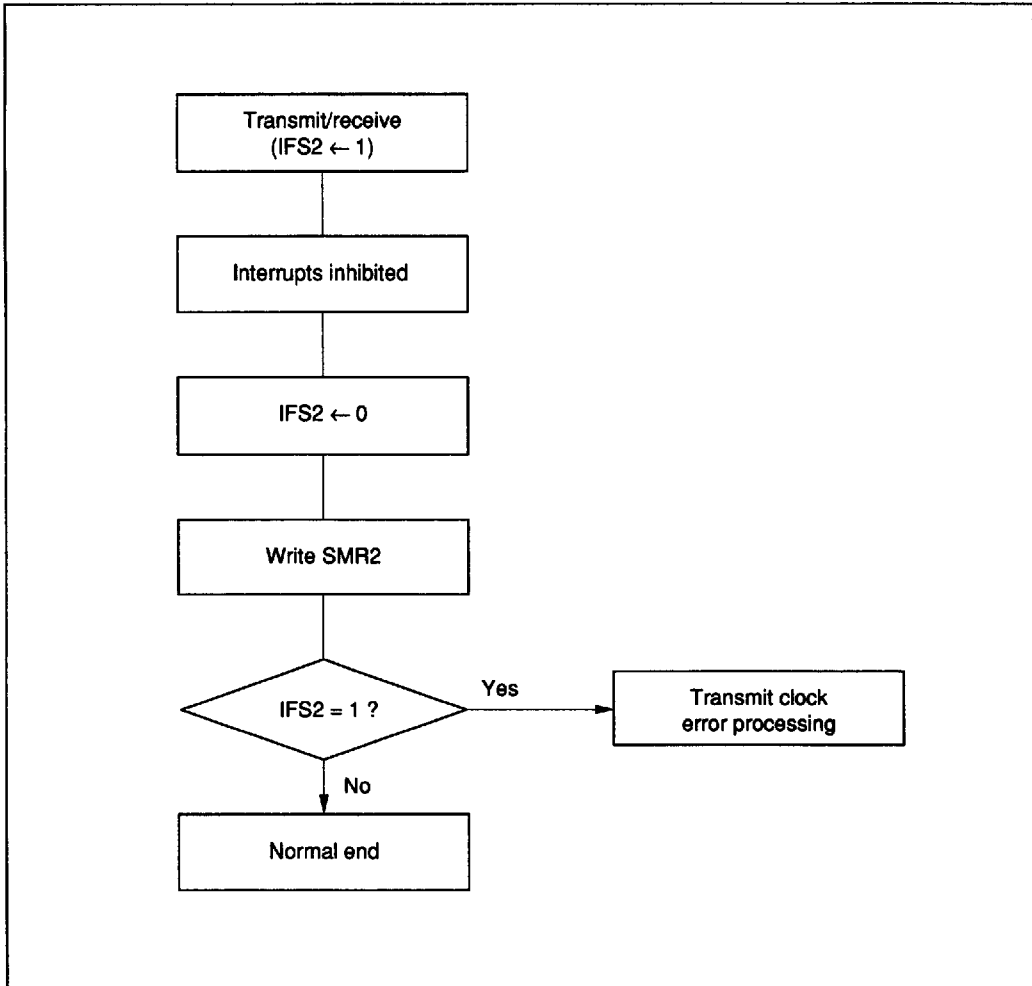


Figure 53 Transmit Clock Error Detection

### A/D Converter

The MCU has an 8-bit A/D converter of serial comparison type. It has eight input channels. The block diagram is shown in figure 54.

**A/D Control Register (ADCR: \$01B):** Selects the analog input pin or digital input port and selects one of eight analog input channels (figure 55). The eight input pins ( $RC_0/AN_0$ – $RC_3/AN_3$ ,  $RD_0/AN_4$ – $RD_3/AN_7$ ) must not include analog input mode pins and port input mode pins at the same time; all the pins must be set to the same mode. When selecting analog input mode for these pins, select without pull-up MOS option for the pins.

**A/D Status Register (ADSR: \$01F):** A/D conversion is started by setting 1 to the A/D start flag. At

conversion completion, the converted data is set to the A/D data register and the A/D start flag is reset (figure 56).

**A/D Mode Register (AMR: \$01C):** Two-bit write-only register which selects the A/D conversion speed (figure 57).

**A/D Data Register (ADRL: \$01D, ADRU: \$01E):** Eight-bit read-only register separated into lower and upper digits (figure 58). Eight-bit A/D converted data is set to the register at conversion completion, and is held until the next conversion starts. Data read during conversion is invalid. The register cannot be cleared by MCU reset.

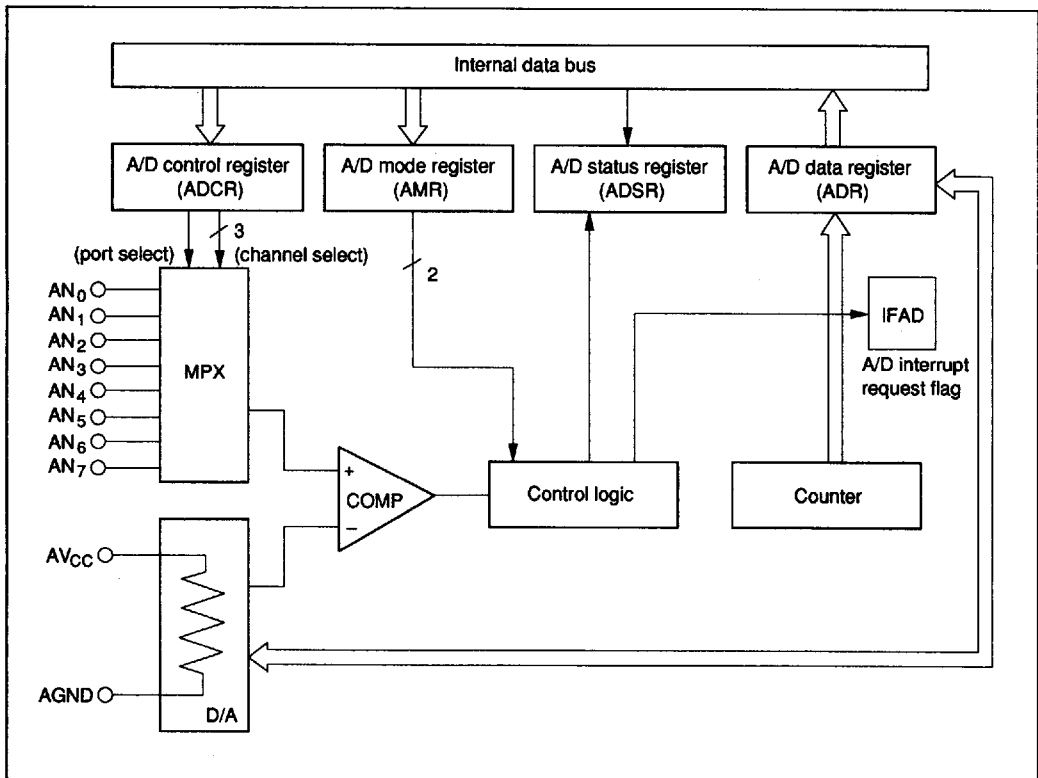
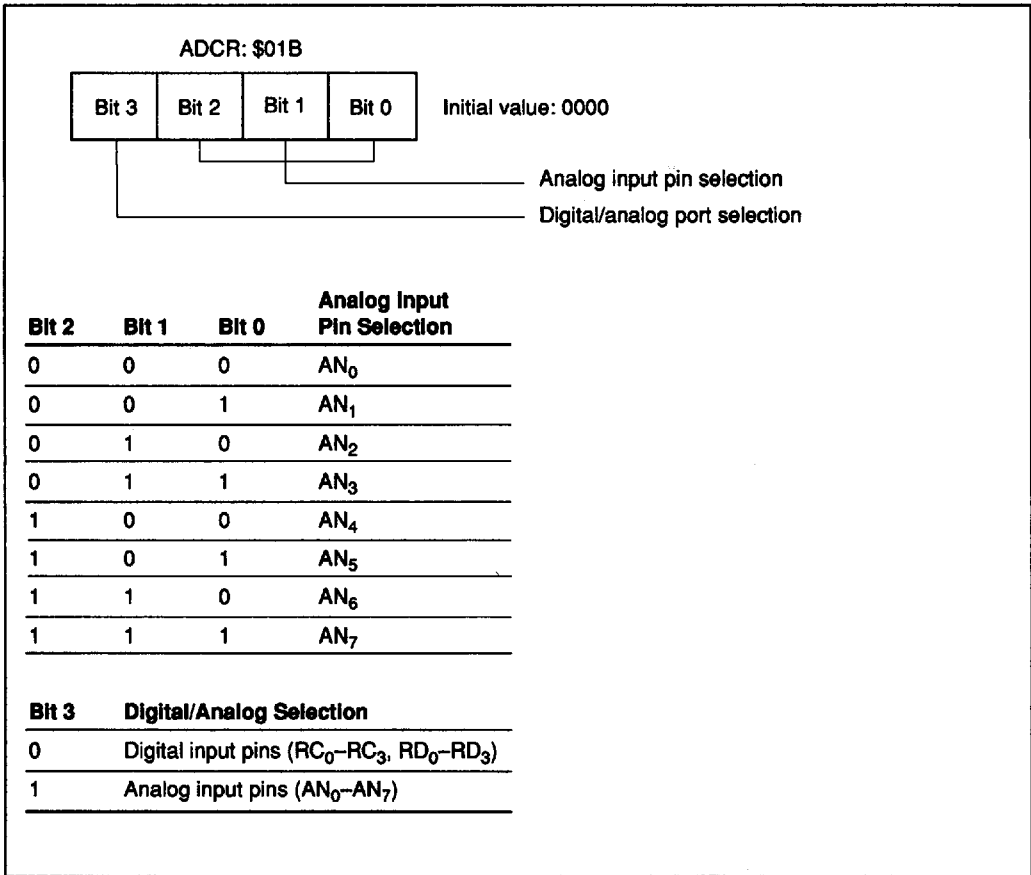
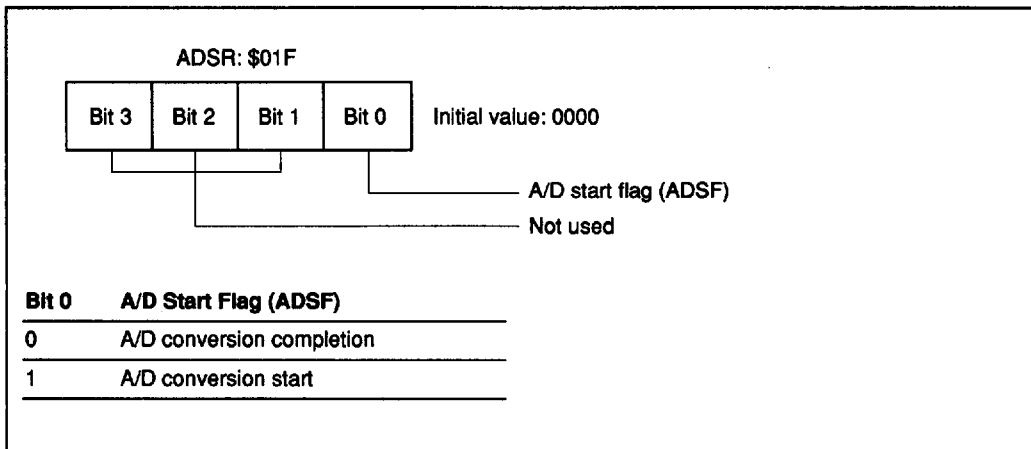


Figure 54 Block Diagram of A/D Converter

# HD404710 Series



**Figure 55 A/D Control Register**



**Figure 56 A/D Status Register**



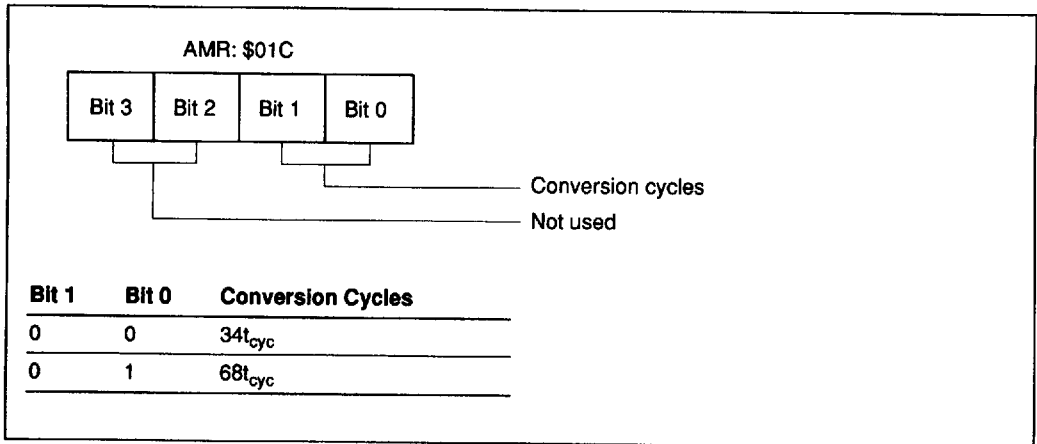


Figure 57 A/D Mode Register

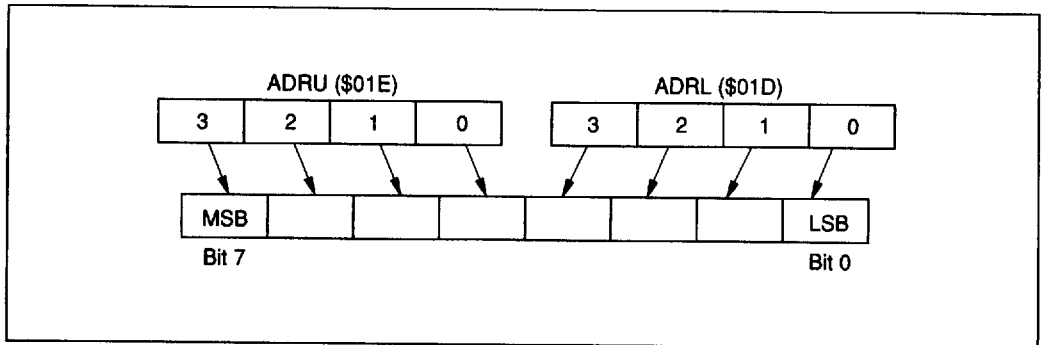


Figure 58 A/D Data Register

## Comparator

The block diagram of the comparator is shown in figure 59. The comparator compares input voltage with the reference voltage. Internal voltage or external input voltage can be selected as the reference. Internal reference voltage is selected from seven levels. When bits 0, 1, and 2 of the compare control register are 0, external reference voltage is input.

The LAR instruction executes a voltage comparison. When the COMP input voltage is higher than

the reference voltage, data 0 is read from port R6<sub>0</sub>.

The power supply for the comparator is the digital V<sub>CC</sub> and GND. When using the comparator, select with pull-up MOS option for pins R6<sub>0</sub> and R6<sub>1</sub>.

**Compare Control Register (CCR: \$03E):** Four-bit write-only register which enables comparator operation and selects internal reference voltage sources (figure 60).

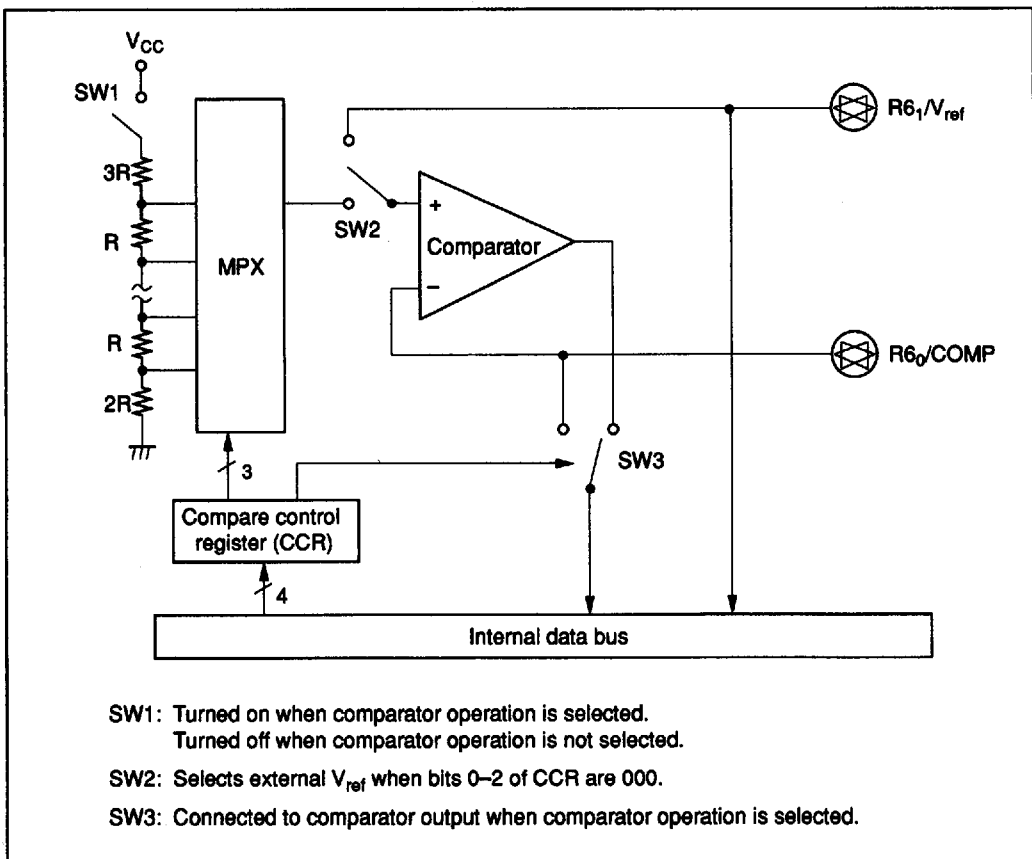


Figure 59 Block Diagram of Comparator

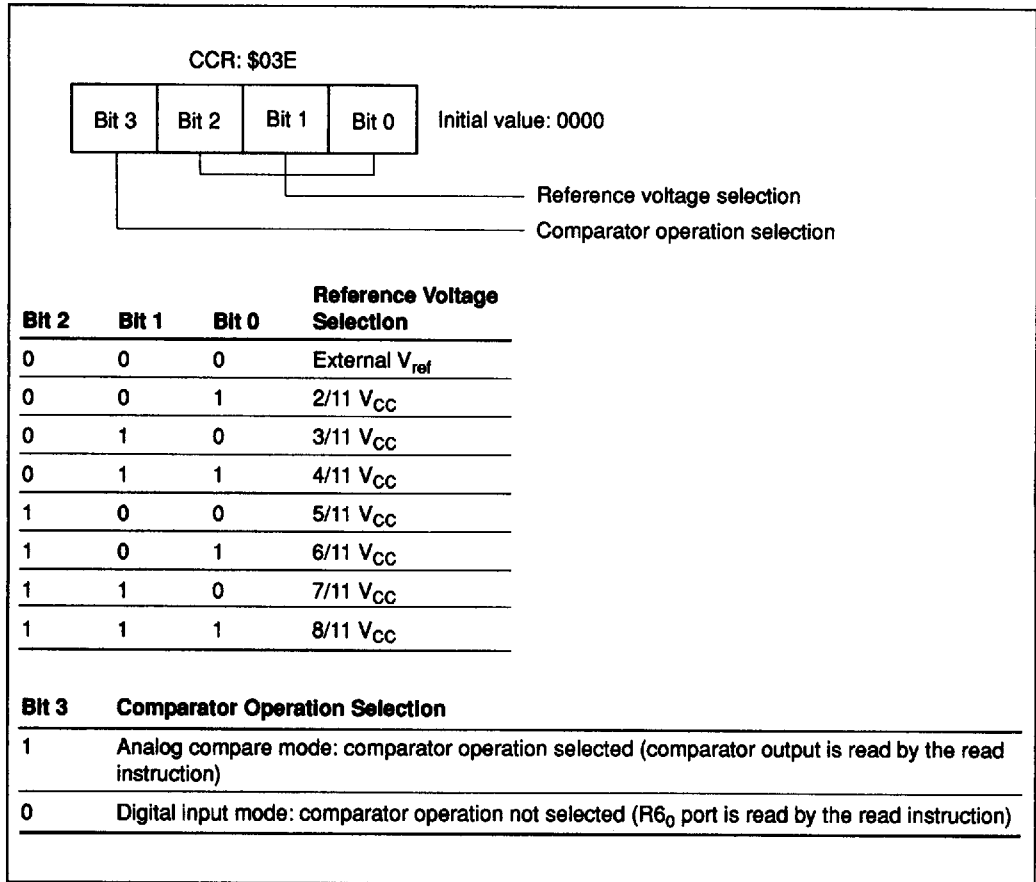


Figure 60 Compare Control Register

# HD404710 Series

## Programmable ROM (HD4074710)

The HD4074719 and HD4074710 are ZTAT™ microcomputers with built-in PROM that can be programmed in PROM mode.

### PROM Mode Pin Description

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	RD <sub>1</sub> /AN <sub>5</sub>	I			31	29	R0 <sub>2</sub>	I/O	A <sub>3</sub>	I
2	80	RD <sub>2</sub> /AN <sub>6</sub>	I			32	30	R0 <sub>3</sub>	I/O	A <sub>4</sub>	I
3	1	RD <sub>3</sub> /AN <sub>7</sub>	I			33	31	R1 <sub>0</sub>	I/O	A <sub>5</sub>	I
4	2	AGND		GND		34	32	R1 <sub>1</sub>	I/O	A <sub>6</sub>	I
5	3	RESET	I	RESET	I	35	33	R1 <sub>2</sub>	I/O	A <sub>7</sub>	I
6	4	OSC <sub>1</sub>	I	GND		36	34	R1 <sub>3</sub>	I/O	A <sub>8</sub>	I
7	5	OSC <sub>2</sub>	O			37	35	R2 <sub>0</sub>	I/O	A <sub>0</sub>	I
8	6	GND		GND		38	36	R2 <sub>1</sub>	I/O	A <sub>10</sub>	I
9	7	CL <sub>1</sub>	I	GND		39	37	R2 <sub>2</sub>	I/O	A <sub>11</sub>	I
10	8	CL <sub>2</sub>	O			40	38	R2 <sub>3</sub>	I/O	A <sub>12</sub>	I
11	9	TEST	I	TEST	I	41	39	R3 <sub>0</sub>	I/O	A <sub>13</sub>	I
12	10	V <sub>CC</sub>		V <sub>CC</sub>		42	40	R3 <sub>1</sub>	I/O	A <sub>14</sub>	I
13	11	D <sub>0</sub>	I/O			43	41	R3 <sub>2</sub>	I/O		
14	12	D <sub>1</sub>	I/O			44	42	R3 <sub>3</sub>	I/O		
15	13	D <sub>2</sub>	I/O			45	43	R4 <sub>0</sub>	I/O		
16	14	D <sub>3</sub>	I/O			46	44	R4 <sub>1</sub>	I/O		
17	15	D <sub>4</sub>	I/O			47	45	R4 <sub>2</sub>	I/O		
18	16	D <sub>5</sub>	I/O			48	46	R4 <sub>3</sub>	I/O		
19	17	D <sub>6</sub>	I/O			49	47	R5 <sub>0</sub> /V <sub>disp</sub>	I		
20	18	D <sub>7</sub>	I/O			50	48	R5 <sub>1</sub>	I	V <sub>CC</sub>	
21	19	D <sub>8</sub>	I/O			51	49	R5 <sub>2</sub>	I	V <sub>PP</sub>	
22	20	D <sub>9</sub>	I/O			52	50	R5 <sub>3</sub>	I	A <sub>9</sub>	I
23	21	D <sub>10</sub>	I/O			53	51	R6 <sub>0</sub> /COMP	I/O	$\overline{\text{CE}}$	I
24	22	D <sub>11</sub>	I/O			54	52	R6 <sub>1</sub> /V <sub>ref</sub>	I/O	$\overline{\text{OE}}$	I
25	23	D <sub>12</sub>	I/O			55	53	R6 <sub>2</sub> /TOE <sub>1</sub>	I/O	V <sub>CC</sub>	
26	24	D <sub>13</sub>	I/O			56	54	R6 <sub>3</sub> /TOE <sub>2</sub>	I/O	V <sub>CC</sub>	
27	25	D <sub>14</sub>	I/O			57	55	R7 <sub>0</sub> /INT <sub>0</sub>	I/O	O <sub>0</sub>	I/O
28	26	D <sub>15</sub>	I/O			58	56	R7 <sub>1</sub> /INT <sub>1</sub>	I/O	O <sub>1</sub>	I/O
29	27	R0 <sub>0</sub>	I/O	A <sub>1</sub>	I	59	57	R7 <sub>2</sub> /INT <sub>2</sub>	I/O	O <sub>2</sub>	I/O
30	28	R0 <sub>1</sub>	I/O	A <sub>2</sub>	I	60	58	R7 <sub>3</sub> /INT <sub>3</sub>	I/O	O <sub>3</sub>	I/O

- Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin  
 2. O<sub>0</sub>-O<sub>4</sub> each have 2 pins; connect each pair together for use.

## HD404710 Series

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
61	59	R8 <sub>0</sub> /INT <sub>4</sub>	I/O	O <sub>4</sub>	I/O	71	69	RA <sub>2</sub> /TOG	I/O	O <sub>7</sub>	I/O
62	60	R8 <sub>1</sub> /INT <sub>5</sub>	I/O	O <sub>4</sub>	I/O	72	70	RA <sub>3</sub> /BUZZ	I/O	PSEL*	I*
63	61	R8 <sub>2</sub> /SO <sub>1</sub>	I/O	O <sub>3</sub>	I/O	73	71	RB <sub>0</sub> /TOC	I/O	M <sub>0</sub>	I
64	62	R8 <sub>3</sub> /SI <sub>1</sub>	I/O	O <sub>2</sub>	I/O	74	72	RB <sub>1</sub> /TOD	I/O	M <sub>1</sub>	I
65	63	R9 <sub>0</sub> /SCK <sub>1</sub>	I/O	O <sub>1</sub>	I/O	75	73	AV <sub>CC</sub>		V <sub>CC</sub>	
66	64	R9 <sub>1</sub> /SCK <sub>2</sub>	I/O	O <sub>0</sub>	I/O	76	74	RC <sub>0</sub> /AN <sub>0</sub>	I		
67	65	R9 <sub>2</sub> /SI <sub>2</sub>	I/O			77	75	RC <sub>1</sub> /AN <sub>1</sub>	I		
68	66	R9 <sub>3</sub> /SO <sub>2</sub>	I/O			78	76	RC <sub>2</sub> /AN <sub>2</sub>	I		
69	67	RA <sub>0</sub> /ICT <sub>0</sub>	I/O	O <sub>5</sub>	I/O	79	77	RC <sub>3</sub> /AN <sub>3</sub>	I		
70	68	RA <sub>1</sub> /ICT <sub>1</sub>	I/O	O <sub>6</sub>	I/O	80	78	RD <sub>0</sub> /AN <sub>4</sub>	I		

Notes: I/O: Input/output pin, I: Input pin, O: Output pin  
 O<sub>0</sub>–O<sub>4</sub> each have 2 pins; connect each pair together for use.

\* Applies to HD4074710.

# HD404710 Series

## PROM Mode Pin Functions

**V<sub>pp</sub>**: Applies the programming voltage (12.5 V ± 0.3 V) to the built-in PROM.

**$\overline{CE}$** : Inputs a control signal to enable PROM programming and verification.

**$\overline{OE}$** : Inputs a data output control signal for verification.

**A<sub>0</sub>-A<sub>14</sub>**: Address input pins of the built-in PROM.

**O<sub>0</sub>-O<sub>7</sub>**: Data bus input pins of the built-in PROM.

**$\overline{M}_0, \overline{M}_1$** : Used to set PROM mode. The MCU is set to the PROM mode by pulling  $\overline{M}_0, \overline{M}_1$ , and  $\overline{TEST}$  low, and RESET high.

**PSEL (HD404710)**: Inputs a signal which selects the program ROM (16,384 words) or pattern ROM (8,192 words).

PSEL	EPROM Select
0	Program ROM (16,384 words)
1	Pattern ROM (8,192 words)

The pin arrangement in PROM mode is shown in figure 61.

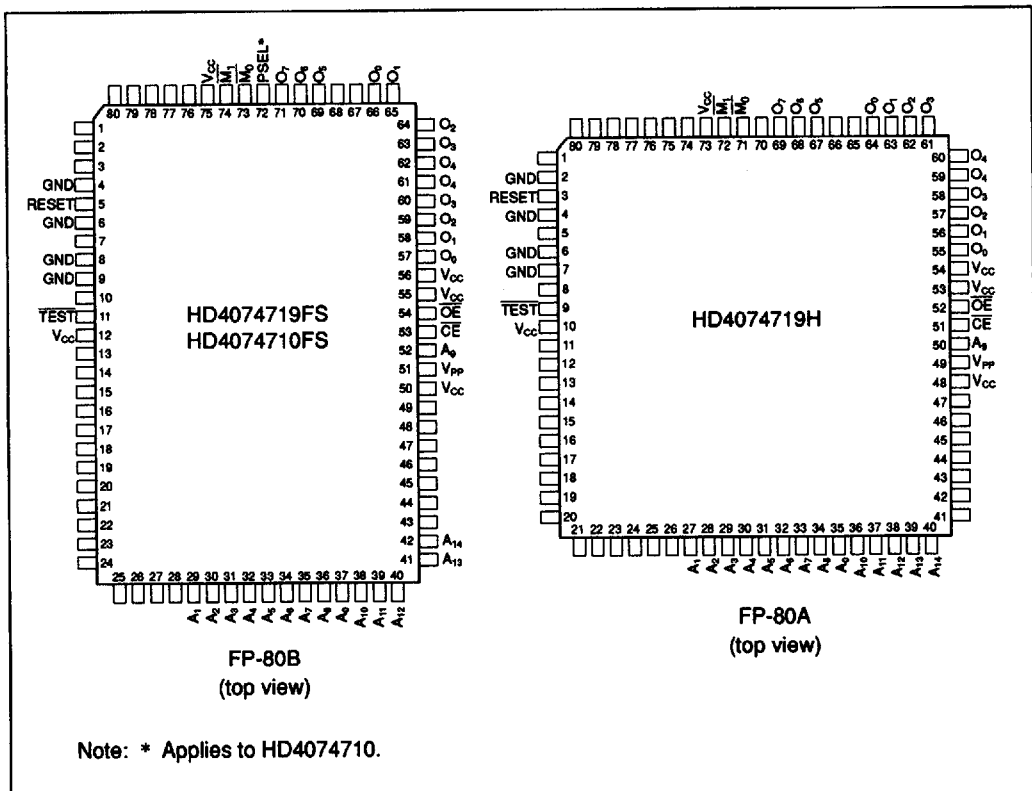


Figure 61 Pin Arrangement in PROM Mode

## Programming the Built-in PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling  $\overline{\text{TEST}}$ ,  $\overline{\text{M}}_0$ , and  $\overline{\text{M}}_1$  low, and RESET high, as shown in figure 62. In PROM mode, the MCU does not operate, but the 16-kword PROM and 8-kword PROM (HD404710) can both be programmed in the same way as any other commercial 27256 EPROM using a standard PROM programmer and an 80-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 34. For HD404710, these socket adapters have PSEL select switches, which select the 16-kword PROM or 8-kword PROM by setting PSEL low or high.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower 5 bits and an upper 5 bits that are read from or written to consecutive addresses, as shown in figure 63. This means that if, for example, a 16-kword built-in PROM is to be programmed by a general-purpose PROM programmer, a 32-kbyte address space (\$0000-\$7FFF) must be specified.

**Programming and Verification:** The built-in PROM of the MCU can be programmed at high-speed programming sequence without risk of voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 33, and the memory map in

PROM mode is shown in figure 63.

For details of PROM programming, refer to the Notes on PROM Programming section.

### Warnings

1. Always specify addresses \$0000 to \$7FFF when programming with a PROM programmer. For 8-kword PROM (HD404710), the data in addresses \$4000 to \$7FFF must be \$FF. If address \$8000 (\$4000 in the 8-kword PROM) or higher is accessed in the 16-kword PROM, the PROM may not be programmed or verified correctly. Set all data in unused addresses to \$FF.

Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.
3. PROM programmers have two voltages ( $V_{PP}$ ): 12.5 V and 21 V. Remember that ZTAT™ devices require a  $V_{PP}$  of 12.5 V—the 21-V setting will damage them. A voltage of 12.5 V is the Intel's 27256 setting.

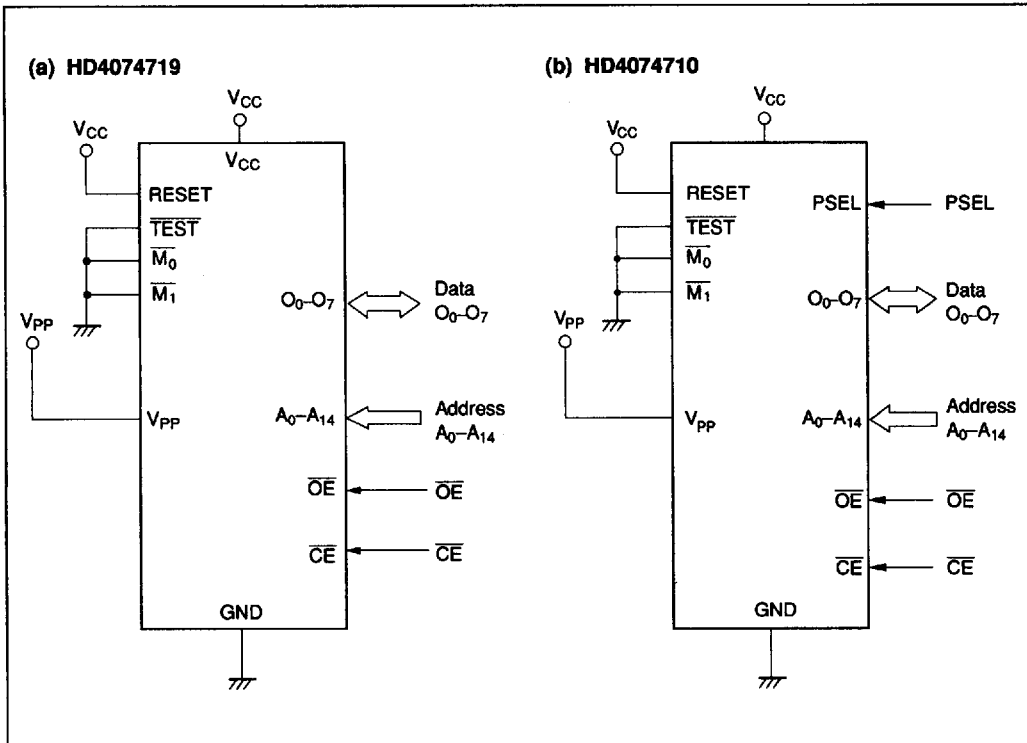
Table 33 PROM Mode Selection

Mode	Pin			
	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$V_{PP}$	$\text{O}_0\text{--O}_7$
Programming	Low	High	$V_{PP}$	Data input
Verification	High	Low	$V_{PP}$	Data output
Programming inhibition	High	High	$V_{PP}$	High impedance

# HD404710 Series

**Table 34 Recommended PROM Programmers and Socket Adapters**

Product Name	PROM Programmer		Socket Adapter		
	Manufacturer	Model Name	Package	Model Name	Manufacturer
HD4074719	DATA I/O Corp.	29B Unisite	FP-80A	HS471ESH01H	Hitachi
			FP-80B	HS471ESF01H	
	AVAL Data Corp.	PKW1100 PKW3100	FP-80A	HS471ESH01H	
			FP-80B	HS471ESF01H	
HD4074710	DATA I/O Corp.	29B Unisite	FP-80B	HS4710ESF01H	Hitachi
	AVAL Data Corp.	PKW1100 PKW3100	FP-80B	HS4710ESF01H	



**Figure 62 Connections for PROM Mode**



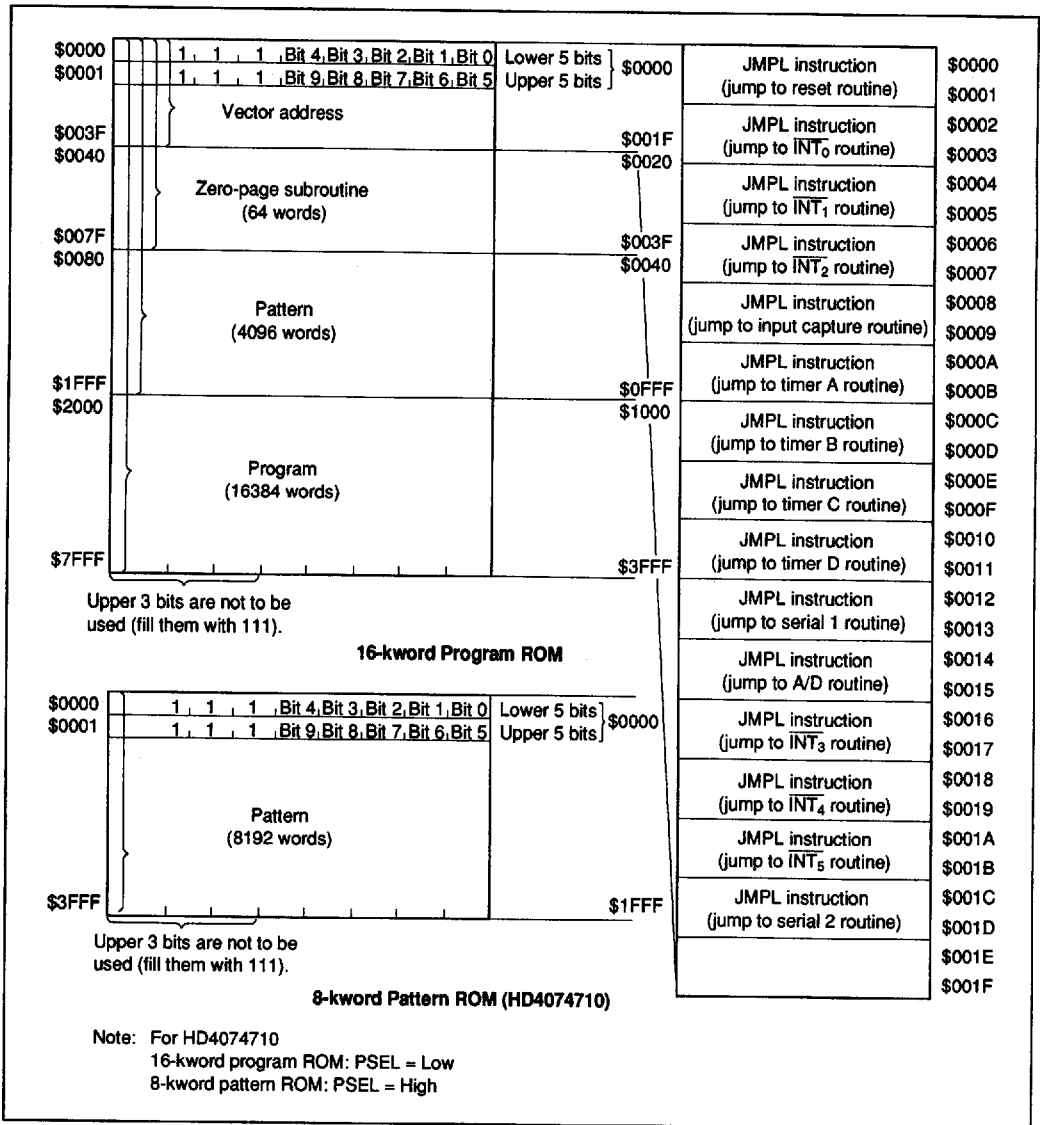


Figure 63 Memory Map in PROM Mode

## Addressing Modes

### RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 64 and described below.

**Register Indirect Addressing Mode:** The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

**Direct Addressing Mode:** A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

**Memory Register Addressing Mode:** The memory registers (MR), located in 16 digits from \$040 to \$04F, are accessed with the LAMR and XMRA instructions.

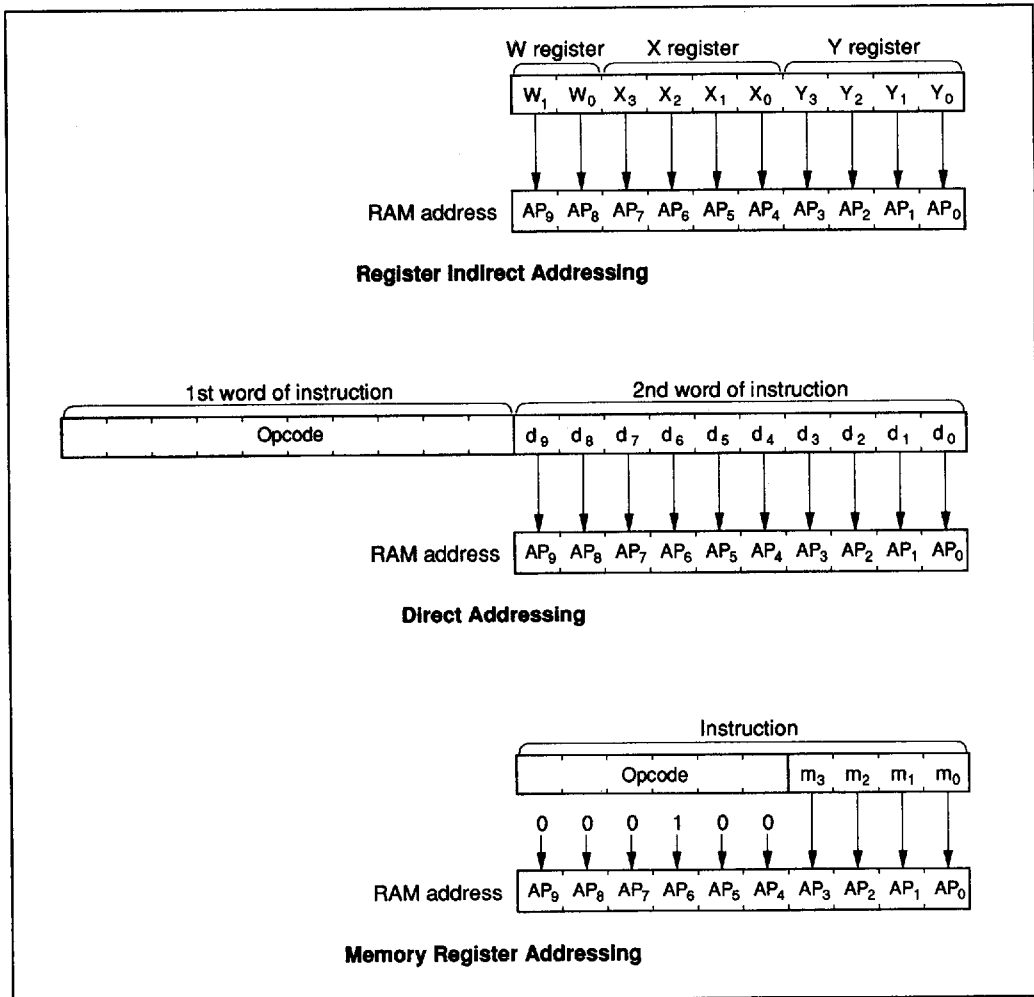


Figure 64 RAM Addressing Modes

**ROM Addressing Modes and the P Instruction**

The MCU has four ROM addressing modes, as shown in figure 65, and the P instruction shown in figures 66-1 and 66-2.

**Direct Addressing Mode:** A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC<sub>13</sub>-PC<sub>0</sub>) with 14-bit immediate data.

**Current Page Addressing Mode:** The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC<sub>7</sub>-PC<sub>0</sub>) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 67. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

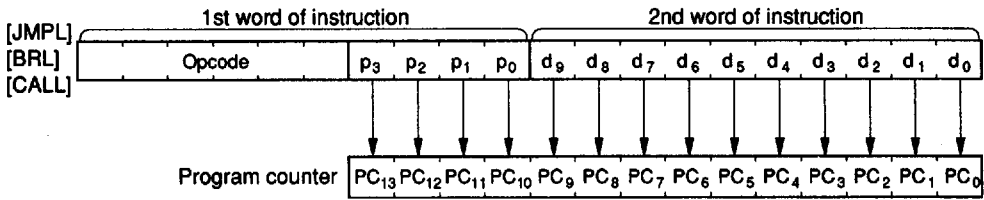
Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

**Zero-Page Addressing Mode:** A program can branch to the zero-page subroutine area located at \$0000-\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC<sub>5</sub>-PC<sub>0</sub>), and 0s are placed in the eight high-order bits (PC<sub>13</sub>-PC<sub>6</sub>).

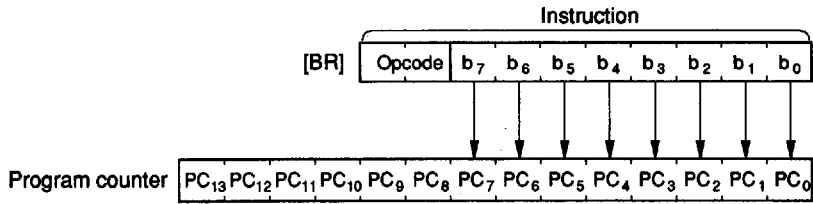
**Table Data Addressing Mode:** A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

**P Instruction:** ROM data addressed in table data addressing mode can be referenced by the P instruction as shown in figure 65. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

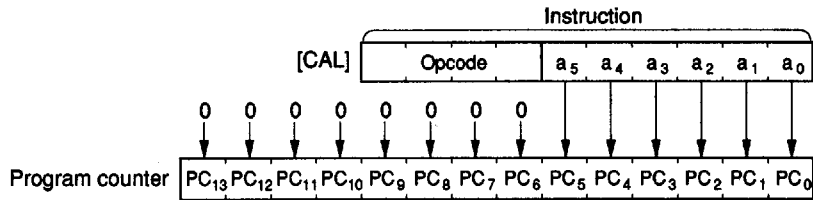
The P instruction has no effect on the program counter.



Direct Addressing



Current Page Addressing



Zero Page Addressing

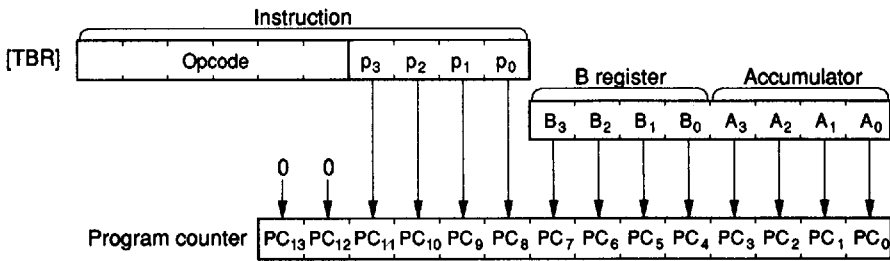


Table Data Addressing

Figure 65 ROM Addressing Modes

HD404719, HD4074719

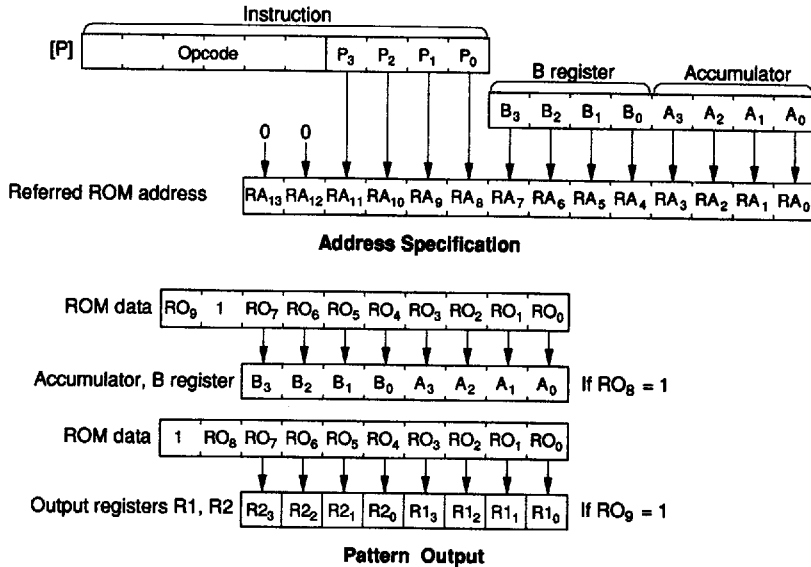


Figure 66-1 P Instruction (HD404719, HD4074719)

HD404710, HD4074710

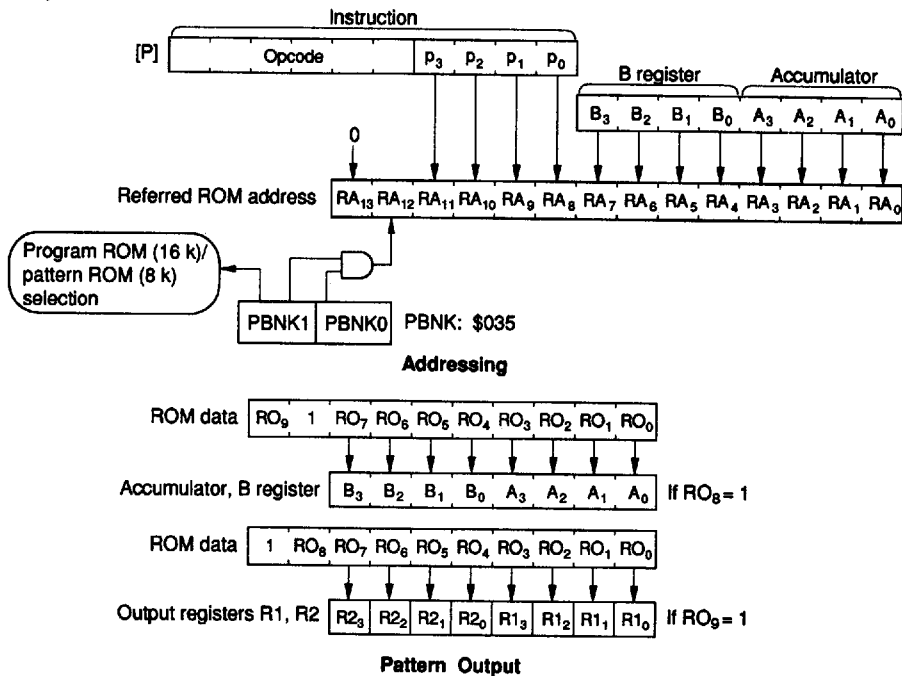


Figure 66-2 P Instruction (HD404710, HD4074710)

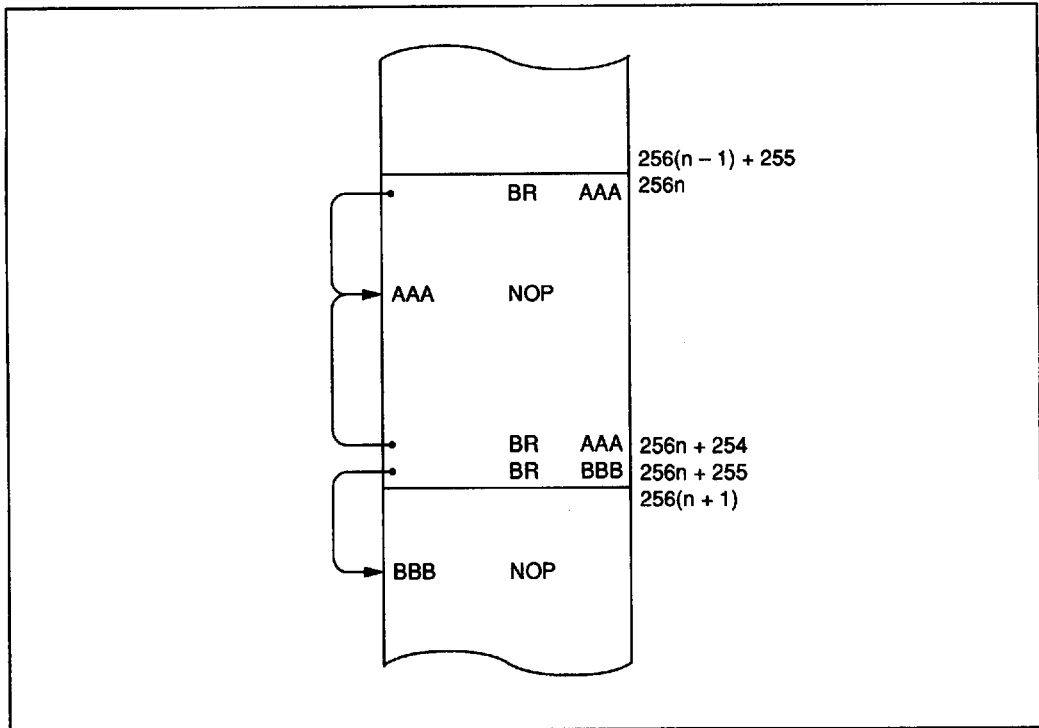


Figure 67 Branching when BR Instruction is on a Page Boundary

**Absolute Maximum Ratings**

Item	Symbol	Value	Unit	Notes
Supply voltage	$V_{CC}$	-0.3 to +7.0	V	
Programming voltage	$V_{PP}$	-0.3 to +14.0	V	12
Pin voltage	$V_T$	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total permissible input current	$\Sigma I_o$	50	mA	5
Total permissible output current	$-\Sigma I_o$	150	mA	6
Maximum input current	$I_o$	15	mA	7, 8
Maximum output current	$-I_o$	4	mA	9, 10
		30	mA	9, 11
Operating temperature	$T_{opr}$	-20 to +75	°C	
Storage temperature	$T_{stg}$	-55 to +125	°C	

- Notes:
1. Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
  2. All voltages are with respect to GND.
  3. Standard pins.
  4. High-voltage pins.
  5. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
  6. The total permissible output current is the total of output currents simultaneously flowing out from  $V_{CC}$  to all I/O pins.
  7. The maximum input current is the maximum current flowing from any I/O pin to GND.
  8. Applies to R5-RD.
  9. The maximum output current is the maximum current flowing from  $V_{CC}$  to any I/O pin.
  10. Applies to R6-RB.
  11. Applies to  $D_0$ - $D_{15}$  and R0-R4.
  12. Applies to HD4074719 and HD4074710.

# HD404710 Series

## HD404710 Series Electrical Characteristics

### DC Characteristics

HD404710, HD404719:  $V_{CC} = 3.0\text{ V to }6.0\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ ;  
 HD4074710, HD4074719:  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  
 $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes	
Input high voltage	$V_{IH}$	RESET, $\overline{SCK}_1$ , $\overline{SCK}_2$ , $\overline{INT}_0$ – $\overline{INT}_5$	$0.85 V_{CC}$	—	$V_{CC} + 0.3$	V			
		$SI_1, SI_2$	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V			
		OSC <sub>1</sub>		$V_{CC} - 0.5$	—	$V_{CC} + 0.3$	V	$V_{CC} = 3.5\text{ V to }6.0\text{ V}$	HD404710, HD404719
								$V_{CC} = 3.5\text{ V to }5.5\text{ V}$	HD4074710, HD4074719
		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V				
Input low voltage	$V_{IL}$	RESET, $\overline{SCK}_1$ , $\overline{SCK}_2$ , $\overline{INT}_0$ – $\overline{INT}_5$	-0.3	—	$0.2 V_{CC}$	V			
		$SI_1, SI_2$	-0.3	—	$0.3 V_{CC}$	V			
		OSC <sub>1</sub>		-0.3	—	0.5	V	$V_{CC} = 3.5\text{ V to }6.0\text{ V}$	HD404710, HD404719
								$V_{CC} = 3.5\text{ V to }5.5\text{ V}$	HD4074710, HD4074719
		-0.3	—	0.3	V				
Output high voltage	$V_{OH}$	$\overline{SCK}_1, \overline{SCK}_2$ , SO <sub>1</sub> , SO <sub>2</sub> , TOC, TOD, TOE <sub>1</sub> , TOE <sub>2</sub> , TOG, BUZZ'	$V_{CC} - 1.0$	—	—	V	$-I_{OH} = 1.0\text{ mA}$ , $V_{CC} = 3.5\text{ V to }6.0\text{ V}$	HD404710, HD404719	
			$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.5\text{ mA}$ , $V_{CC} = 3.5\text{ V to }6.0\text{ V}$	HD404710, HD404719	
		$V_{CC} - 1.0$	—	—	V	$-I_{OH} = 1.0\text{ mA}$ , $V_{CC} = 3.5\text{ V to }5.5\text{ V}$	HD4074710, HD4074719		
								$V_{CC} - 0.5$	—
		$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.3\text{ mA}$			
Output low voltage	$V_{OL}$	$\overline{SCK}_1, \overline{SCK}_2$ , SO <sub>1</sub> , SO <sub>2</sub> , TOC, TOD, TOE <sub>1</sub> , TOE <sub>2</sub> , TOG, BUZZ'	—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$ , $V_{CC} = 3.5\text{ V to }6.0\text{ V}$	HD404710, HD404719	
			—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$ , $V_{CC} = 3.5\text{ V to }5.5\text{ V}$	HD4074710, HD4074719	
		—	—	0.4	V	$I_{OL} = 0.4\text{ mA}$			



## DC Characteristics (cont)

**HD404710, HD404719:**  $V_{CC} = 3.0\text{ V to }6.0\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ ;  
**HD4074710, HD4074719:**  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  
 $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
I/O leakage current	$ I_{IL} $	RESET, SCK <sub>1</sub> , SCK <sub>2</sub> , SI <sub>1</sub> , SO <sub>1</sub> , SI <sub>2</sub> , SO <sub>2</sub> , TOC, TOD, TOE <sub>1</sub> , TOE <sub>2</sub> , TOG, BUZZ, OSC <sub>1</sub>	—	—	1	μA	$V_{in} = 0\text{ V to }V_{CC}$	2
Current dissipation in active mode	$I_{CC}$	$V_{CC}$	—	—	11.0	mA	$V_{CC} = 5.0\text{ V}$ , $f_{osc} = 4\text{ MHz}$ , digital input mode	HD404710, 3, 6 HD4074710
			—	—	8.0	mA		HD404719, 3, 6 HD4074719
			—	—	6.0	mA	$V_{CC} = 3.0\text{ V}$ , $f_{osc} = 2\text{ MHz}$ , digital input mode	HD404710, 3, 6 HD4074710
			—	—	4.5	mA		HD404719, 3, 6 HD4074719
	$I_{CMP}$	$V_{CC}$	—	—	15.0	mA	$V_{CC} = 5.0\text{ V}$ , $f_{osc} = 4\text{ MHz}$ , analog compare mode	HD404710, 4, 6 HD4074710
			—	—	12.0	mA		HD404719, 4, 6 HD4074719
			—	—	10.0	mA	$V_{CC} = 3.0\text{ V}$ , $f_{osc} = 2\text{ MHz}$ , analog compare mode	HD404710, 4, 6 HD4074710
			—	—	7.0	mA		HD404719, 4, 6 HD4074719
Current dissipation in standby mode	$I_{SBY}$	$V_{CC}$	—	—	3.0	mA	$V_{CC} = 5.0\text{ V}$ , $f_{osc} = 4\text{ MHz}$	5, 6
			—	—	1.5	mA	$V_{CC} = 3.0\text{ V}$ , $f_{osc} = 2\text{ MHz}$	5, 6
Current dissipation in subactive mode	$I_{SUB}$	$V_{CC}$	—	—	100	μA	$V_{in}(\overline{\text{TEST}}) = V_{CC} - 0.3\text{ V to }V_{CC}$ ,	HD404710 7, 8
			—	—	200	μA	$V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$ ,	HD4074710 7
			—	—	70	μA	$V_{CC} = 3\text{ V}$ , 32.768-kHz crystal oscillator	HD404719 7, 8
			—	—	150	μA		HD4074719 7
Current dissipation in watch mode	$I_{WTC}$	$V_{CC}$	—	—	20	μA	$V_{in}(\overline{\text{TEST}}) = V_{CC} - 0.3\text{ V to }V_{CC}$ ,	HD404710 7, 8, 9
			—	—	20	μA	$V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$ ,	HD4074710 7
			—	—	15	μA	$V_{CC} = 3\text{ V}$ , 32.768-kHz crystal oscillator	HD404719 7, 8, 9
			—	—	15	μA		HD4074719 7

## HD404710 Series

### DC Characteristics (cont)

HD404710, HD404719:  $V_{CC} = 3.0 \text{ V to } 6.0 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ ; HD4074710, HD4074719:  $V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in stop mode	I <sub>STOP</sub>	V <sub>CC</sub>	—	—	10	μA	V <sub>in</sub> (TEST) = V <sub>CC</sub> - 0.3 V to V <sub>CC</sub> , V <sub>in</sub> (RESET) = 0 V to 0.3 V, no 32.768-kHz crystal oscillator	HD404710, 7 HD404719
			—	—	15	μA	HD4074710, 7 HD4074719	
Watch mode retaining voltage	V <sub>WTC</sub>	V <sub>CC</sub>	3.5	—	6.0	V	V <sub>CC</sub> = 3.5 V to 6.0 V	HD404710, 8, 9 HD404719
			3.0	—	6.0	V		
			3.5	—	5.5	V	V <sub>CC</sub> = 3.5 V to 5.5 V	HD4074710, HD4074719
			3.0	—	5.5	V		
Stop mode retaining voltage	V <sub>STOP</sub>	V <sub>CC</sub>	2	—	—	V	No 32.768-kHz crystal oscillator	
Input high voltage	V <sub>IHA</sub>	R6 <sub>O</sub> /COMP	V <sub>Cref</sub> + 0.1	—	—	V	Analog compare mode	
Input low voltage	V <sub>ILA</sub>	R6 <sub>O</sub> /COMP	—	—	V <sub>Cref</sub> - 0.1	V	Analog compare mode	
Range of comparator input reference voltage	V <sub>Cref</sub>	R6 <sub>I</sub> /V <sub>ref</sub>	0	—	V <sub>CC</sub> - 1.2	V		
Allowable error of internal reference voltage	V <sub>OFS</sub>		-100	—	100	mV	V <sub>OFS</sub> = reference voltage - V <sub>Cref</sub>	1

## A/D Converter

**HD404710, HD404719:**  $V_{CC} = 3.0\text{ V to }6.0\text{ V}$ ,  $AGND = GND$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ ;  
**HD4074710, HD4074719:**  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $AGND = GND$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ ,  
 unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Analog supply voltage	$AV_{CC}$	$AV_{CC}$	$V_{CC} - 0.3$	$V_{CC}$	$V_{CC} + 0.3$	V		
Analog input voltage	$AV_{in}$	$AN_0$ - $AN_7$	AGND	—	$AV_{CC}$	V		HD404710, 10 HD404719
			AGND	—	$AV_{CC}$	V		HD4074710 HD4074719,
Current between $AV_{CC}$ and AGND	$I_{AD}$	$AV_{CC}$	—	—	150	$\mu\text{A}$	$AV_{CC} = 5.0\text{ V}$ , $V_{in}(\text{TEST}) = V_{CC} - 0.3\text{ V to }V_{CC}$ , $V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$	
			—	—	10	$\mu\text{A}$	$V_{in}(\text{TEST}) = V_{CC} - 0.3\text{ V to }V_{CC}$ , $V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$ ,	HD404710, HD404719
			—	—	15	$\mu\text{A}$	stop mode, no 32.768-kHz crystal oscillator	HD4074710, HD4074719
Analog input capacitance	$CA_{in}$	$AN_0$ - $AN_7$	—	—	30	pF		
Resolution			—	—	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute error			—	—	$\pm 2.5$	LSB	$T_a = 25^\circ\text{C}$ , $AV_{CC} = 5\text{ V}$	

- Notes:
- The reference voltage is the expected internal  $V_{Cref}$  voltage selected by the compare control register (CCR).  
Example: When CCR = \$9, reference voltage is  $2/11 \times V_{CC}$ .
  - Excluding output buffer current.
  - $I_{CC}$  is the source current when no I/O current is flowing while the MCU is in reset state.  
Test conditions: MCU: Reset  
Pins: RESET, TEST at  $V_{CC}$ ,  $R5_1$ - $RD_3$  at  $V_{CC}$ ,  $D_0$ - $D_{15}$ ,  $R0$ - $R4$ ,  $R5_0$  at  $V_{disp}$
  - $I_{CMP}$  is the source current when no I/O current is flowing while the  $R6_0$ /COMP pin is in analog input mode.  
Test condition: Pins:  $R6_0$ /COMP,  $R6_1$ / $V_{ref}$  at GND.
  - $I_{SBY}$  is the source current when no I/O current is flowing while the MCU timer is in operation.  
Test conditions: MCU: I/O same as at reset, standby mode  
Pins: RESET at GND, TEST at  $V_{CC}$ ,  $R5_1$ - $RD_3$  at  $V_{CC}$ ,  $D_0$ - $D_{15}$ ,  $R0$ - $R4$ ,  $R5_0$  at  $V_{disp}$
  - Power dissipation, while the MCU is operating or in standby mode, is in proportion to  $f_{OSC}$ .  
The value of the dissipation current when  $f_{OSC} = \chi$  MHz is given by the following equation:  
Maximum value ( $f_{OSC} = \chi$  MHz) =  $\chi/4 \times$  maximum value ( $f_{OSC} = 4$  MHz)
  - Source current when no I/O current is flowing.  
Test condition: Pins:  $R5_1$ - $RD_3$  at  $V_{CC}$ ,  $D_0$ - $D_{15}$ ,  $R0$ - $R4$ ,  $R5_0$  at GND
  - Applies when 32-kHz CPU operation is selected as an optional function.
  - Applies when no 32-kHz CPU operation with clock time base is selected as an optional function.
  - Select without pull-up MOS option for pins RC and RD when using these pins as analog input pins.

## HD404710 Series

### Input/Output Characteristics for Standard Pins

**HD404710, HD404719:**  $V_{CC} = 3.0 \text{ V to } 6.0 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ ;  
**HD4074710, HD4074719:**  $V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  
 $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pin (s)	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	$V_{IH}$	R5 <sub>1</sub> -RD <sub>3</sub>	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V		
Input low voltage	$V_{IL}$	R5 <sub>1</sub> -RD <sub>3</sub>	-0.3	—	$0.3 V_{CC}$	V		
Output high voltage	$V_{OH}$	R6-RB	$V_{CC} - 1.0$	—	—	V	$-I_{OH} = 1.0 \text{ mA}$ , $V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719
			$V_{CC} - 1.0$	—	—	V	$-I_{OH} = 1.0 \text{ mA}$ , $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719
			$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.5 \text{ mA}$ , $V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719
			$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.5 \text{ mA}$ , $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719
			$V_{CC} - 0.5$	—	—	V	$-I_{OH} = 0.3 \text{ mA}$	
Output low voltage	$V_{OL}$	R6-RB	—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$ , $V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719
			—	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$ , $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719
			—	—	0.4	V	$I_{OL} = 0.4 \text{ mA}$	
Input/output leakage current	$ I_{IL} $	R6-RD, R5 <sub>1</sub> -R5 <sub>3</sub>	—	—	1	$\mu\text{A}$	$V_{in} = 0.0 \text{ V to } V_{CC}$	HD404710, 1 HD404719
		R6-RD, R5 <sub>1</sub> , R5 <sub>3</sub>	—	—	1	$\mu\text{A}$		HD4074710, 1 HD4074719
		R5 <sub>2</sub>	—	—	20	$\mu\text{A}$		
Pull-up MOS current	$-I_{PU}$	R5 <sub>1</sub> -RD <sub>3</sub>	30	80	160	$\mu\text{A}$	$V_{CC} = 5.0 \text{ V}$ , $V_{in} = 0.0 \text{ V}$	HD4074710, 2 HD4074719
			10	30	60	$\mu\text{A}$	$V_{CC} = 3.0 \text{ V}$ , $V_{in} = 0.0 \text{ V}$	

Notes: 1. Excluding output buffer current.

2. Applies to I/O pins selected as with pull-up MOS by mask option.

## Input/Output Characteristics for High-Voltage Pins

**HD404710, HD404719:**  $V_{CC} = 3.0\text{ V to }6.0\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ ; **HD4074710, HD4074719:**  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	$V_{IH}$	D <sub>0</sub> -D <sub>15</sub> , R <sub>0</sub> -R <sub>4</sub> , R <sub>5<sub>0</sub></sub>	0.7 $V_{CC}$	—	$V_{CC} + 0.3$	V		
Input low voltage	$V_{IL}$	D <sub>0</sub> -D <sub>15</sub> , R <sub>0</sub> -R <sub>4</sub> , R <sub>5<sub>0</sub></sub>	$V_{CC} - 40$	—	0.3 $V_{CC}$	V		
Output high voltage	$V_{OH}$	D <sub>0</sub> -D <sub>15</sub> , R <sub>0</sub> -R <sub>4</sub>	$V_{CC} - 3.0$	—	—	V	$-I_{OH} = 15\text{ mA}$ , $V_{CC} = 4.0\text{ V to }6.0\text{ V}$	HD404710, HD404719
			$V_{CC} - 3.0$	—	—	V	$-I_{OH} = 15\text{ mA}$ , $V_{CC} = 4.0\text{ V to }5.5\text{ V}$	HD4074710, HD4074719
			$V_{CC} - 2.0$	—	—	V	$-I_{OH} = 10\text{ mA}$ , $V_{CC} = 4.0\text{ V to }6.0\text{ V}$	HD404710, HD404719
			$V_{CC} - 2.0$	—	—	V	$-I_{OH} = 10\text{ mA}$ , $V_{CC} = 4.0\text{ V to }5.5\text{ V}$	HD4074710, HD4074719
			$V_{CC} - 1.0$	—	—	V	$-I_{OH} = 4\text{ mA}$	
Output low voltage	$V_{OL}$	D <sub>0</sub> -D <sub>15</sub> , R <sub>0</sub> -R <sub>4</sub>	—	—	$V_{CC} - 37$	V	$V_{disp} = V_{CC} - 40\text{ V}$	HD404710, 1 HD404719
			—	—	$V_{CC} - 37$	V	150 k $\Omega$ at $V_{CC} - 40\text{ V}$	2
			—	—	$V_{CC} - 37$	V	150 k $\Omega$ at $V_{CC} - 40\text{ V}$	HD4074710, HD4074719
Input/output leakage current	$ I_{IL} $	D <sub>0</sub> -D <sub>15</sub> , R <sub>0</sub> -R <sub>4</sub> , R <sub>5<sub>0</sub></sub>	—	—	20	$\mu\text{A}$	$V_{in} = V_{CC} - 40\text{ V to }V_{CC}$	3
Pull-down MOS current	$I_{PD}$	D <sub>0</sub> -D <sub>15</sub> , R <sub>0</sub> -R <sub>4</sub>	200	400	800	$\mu\text{A}$	$V_{disp} = V_{CC} - 35\text{ V}$ , $V_{in} = V_{CC}$	HD404710, 1 HD404719

- Notes:
1. Applies to I/O pins selected as with pull-down MOS by mask option.
  2. Applies to I/O pins selected as without pull-down MOS (PMOS open drain) by mask option.
  3. For HD404710 and HD404719, excluding pull-down MOS current and output buffer current.
  4. For HD4074710 and HD4074719, excluding output buffer current.

# HD404710 Series

## AC Characteristics

HD404710, HD404719:  $V_{CC} = 3.0 \text{ V to } 6.0 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ , HD4074710, HD4074719:  $V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes	
Oscillation frequency (1/4 division)	$f_{OSC}$	OSC <sub>1</sub> , OSC <sub>2</sub>	1.6	4	4.5	MHz	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	
			1.6	4	4.5	MHz	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	
			1.6	2	2.25	MHz			
Oscillation frequency (1/8 division)	$f_{CL}$	CL <sub>1</sub> , CL <sub>2</sub>	—	32.768	—	kHz			
Instruction cycle time	$t_{cyc}$		0.89	1	2.5	$\mu\text{s}$	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	
			0.89	1	2.5	$\mu\text{s}$	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	
			1.78	2	2.5	$\mu\text{s}$			
Instruction cycle time	$t_{subcyc}$		—	244.14	—	$\mu\text{s}$		6	
Oscillation stabilization time (crystal oscillator)	$t_{RC}$	OSC <sub>1</sub> , OSC <sub>2</sub>	—	—	40	ms	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	1
			—	—	40	ms	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	1
			—	—	60	ms			1
Oscillation stabilization time (ceramic oscillator)	$t_{RC}$	OSC <sub>1</sub> , OSC <sub>2</sub>	—	—	20	ms	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	1
			—	—	20	ms	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	1
			—	—	60	ms			1
Oscillation stabilization time	$t_{RC}$	CL <sub>1</sub> , CL <sub>2</sub>	—	—	2	s			2
External clock high width	$t_{CPH}$	OSC <sub>1</sub>	92	—	—	ns	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	3
			92	—	—	ns	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	3
			203	—	—	ns			3
External clock low width	$t_{CPL}$	OSC <sub>1</sub>	92	—	—	ns	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	3
			92	—	—	ns	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	3
			203	—	—	ns			3
External clock rise time	$t_{CPr}$	OSC <sub>1</sub>	—	—	20	ns	$V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$	HD404710, HD404719	3
			—	—	20	ns	$V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$	HD4074710, HD4074719	3
			—	—	20	ns			3

## AC Characteristics (cont)

**HD404710, HD404719:**  $V_{CC} = 3.0\text{ V to }6.0\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ , **HD4074710, HD4074719:**  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$ ,  $GND = 0.0\text{ V}$ ,  $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
External clock fall time	$t_{CPf}$	OSC <sub>1</sub>	—	—	20	ns	$V_{CC} = 3.5\text{ V to }6.0\text{ V}$	HD404710, HD404719
			—	—	20	ns	$V_{CC} = 3.5\text{ V to }5.5\text{ V}$	HD4074710, HD4074719
			—	—	20	ns		3
INT <sub>0</sub> high width	$t_{IH}$	INT <sub>0</sub>	2	—	—	$t_{cyc}$ $t_{subcyc}$	4, 6	
INT <sub>0</sub> low width	$t_{IL}$	INT <sub>0</sub>	2	—	—	$t_{cyc}$ $t_{subcyc}$	4, 6	
INT high width	$t_{IH}$	INT <sub>1</sub> –INT <sub>5</sub>	2	—	—	$t_{cyc}$	4	
INT low width	$t_{IL}$	INT <sub>1</sub> –INT <sub>5</sub>	2	—	—	$t_{cyc}$	4	
RESET high width	$t_{RSTH}$	RESET	2	—	—	$t_{cyc}$	5	
Input capacitance	$C_{in}$	All pins	—	—	30	pF	$f = 1\text{ MHz}$ , $V_{in} = 0\text{ V}$	HD404710, HD404719
		Other than R5 <sub>2</sub>	—	—	30	pF		HD4074710, HD4074719
		R5 <sub>2</sub>	—	—	180	pF		HD4074719
Analog comparator stabilization time	$t_{CSTB}$	R6 <sub>0</sub> /COMP	—	—	2	$t_{cyc}$		7

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize after  $V_{CC}$  reaches 3.0 V (3.5 V if  $V_{CC} = 3.5\text{ V to }6.0\text{ V}$  [applies to HD404710/HD404719],  $V_{CC} = 3.5\text{ V to }5.5\text{ V}$  [applies to HD4074710/HD4074719]) at power-on or after RESET input goes high after stop mode in cancelled (figure 68).

At power-on and when stop mode is cancelled, RESET must remain high for at least  $t_{RC}$  to ensure the oscillation stabilization time.

If using an oscillator, contact the oscillator manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.

2. The oscillation stabilization time is the period required for the oscillator to stabilize after  $V_{CC}$  reaches 3.0 V at power-on (figure 69). If using a crystal oscillator, contact the manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
3. Refer to figure 70.
4. Refer to figure 71.
5. Refer to figure 72. The MCU will malfunction if noise interferes with the falling edge of the RESET signal when releasing from reset state. The reset circuit must be sufficiently evaluated in the application system.
6. The  $t_{subcyc}$  unit applies when the MCU is in watch or subactive mode.  
 $t_{subcyc} = 244.14\ \mu\text{s}$  (32.768 kHz crystal)
7. The analog comparator stabilization time is the period required for the analog comparator to stabilize and to read correct data after pin P6<sub>0</sub> switches to analog input mode.

## HD404710 Series

### Serial Interface Timing Characteristics

HD404710, HD404719:  $V_{CC} = 3.0 \text{ V to } 6.0 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ , HD4074710, HD4074719:  $V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $GND = 0.0 \text{ V}$ ,  $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$ , unless otherwise specified

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output transmit clock cycle time	$t_{S_{cyc}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	1	—	—	$t_{cyc}$	Load shown in figure 74.	1
Output transmit clock high width	$t_{S_{CKH}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	0.4	—	—	$t_{S_{cyc}}$	Load shown in figure 74.	1
Output transmit clock low width	$t_{S_{CKL}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	0.4	—	—	$t_{S_{cyc}}$	Load shown in figure 74.	1
Output transmit clock rise time	$t_{S_{CKr}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	—	—	80	ns	Load shown in figure 74.	1
Output transmit clock fall time	$t_{S_{CKf}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	—	—	80	ns	Load shown in figure 74.	1
Input transmit clock cycle time	$t_{S_{cyc}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	2	—	—	$t_{cyc}$		1
Input transmit clock high width	$t_{S_{CKH}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	0.4	—	—	$t_{S_{cyc}}$		1
Input transmit clock low width	$t_{S_{CKL}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	0.4	—	—	$t_{S_{cyc}}$		1
Input transmit clock rise time	$t_{S_{CKr}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	—	—	80	ns		1
Input transmit clock fall time	$t_{S_{CKf}}$	$\overline{SCK_1}$ , $\overline{SCK_2}$	—	—	80	ns		1
Serial output data delay time	$t_{D_{SO}}$	$SO_1$ , $SO_2$	—	—	600	ns	Load shown in figure 74.	1
Serial input data setup time	$t_{S_{SI}}$	$SI_1$ , $SI_2$	200	—	—	ns		1
Serial input data hold time	$t_{H_{SI}}$	$SI_1$ , $SI_2$	400	—	—	ns		1

Note: 1. Refer to figure 73.



Serial Interface Timing Characteristics (cont)

HD404710, HD404719:  $V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$   
 HD4074710, HD4074719:  $V_{CC} = 3.5 \text{ V to } 5.5 \text{ V}$

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output transmit clock cycle time	$t_{\text{Syc}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	1	—	—	$t_{\text{cyc}}$	Load shown in figure 74.	1
Output transmit clock high width	$t_{\text{SCKH}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	$t_{\text{Syc}}$	Load shown in figure 74.	1
Output transmit clock low width	$t_{\text{SCKL}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	$t_{\text{Syc}}$	Load shown in figure 74.	1
Output transmit clock rise time	$t_{\text{SCKr}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	40	ns	Load shown in figure 74.	1
Output transmit clock fall time	$t_{\text{SCKf}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	40	ns	Load shown in figure 74.	1
Input transmit clock cycle time	$t_{\text{Syc}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	2	—	—	$t_{\text{cyc}}$		1
Input transmit clock high width	$t_{\text{SCKH}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	$t_{\text{Syc}}$		1
Input transmit clock low width	$t_{\text{SCKL}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	$t_{\text{Syc}}$		1
Input transmit clock rise time	$t_{\text{SCKr}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	40	ns		1
Input transmit clock fall time	$t_{\text{SCKf}}$	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	40	ns		1
Serial output data delay time	$t_{\text{DSO}}$	$\text{SO}_1, \text{SO}_2$	—	—	300	ns	Load shown in figure 74.	1
Serial input data setup time	$t_{\text{SSI}}$	$\text{SI}_1, \text{SI}_2$	100	—	—	ns		1
Serial input data hold time	$t_{\text{HSI}}$	$\text{SI}_1, \text{SI}_2$	200	—	—	ns		1

Note: 1. Refer to figure 73.

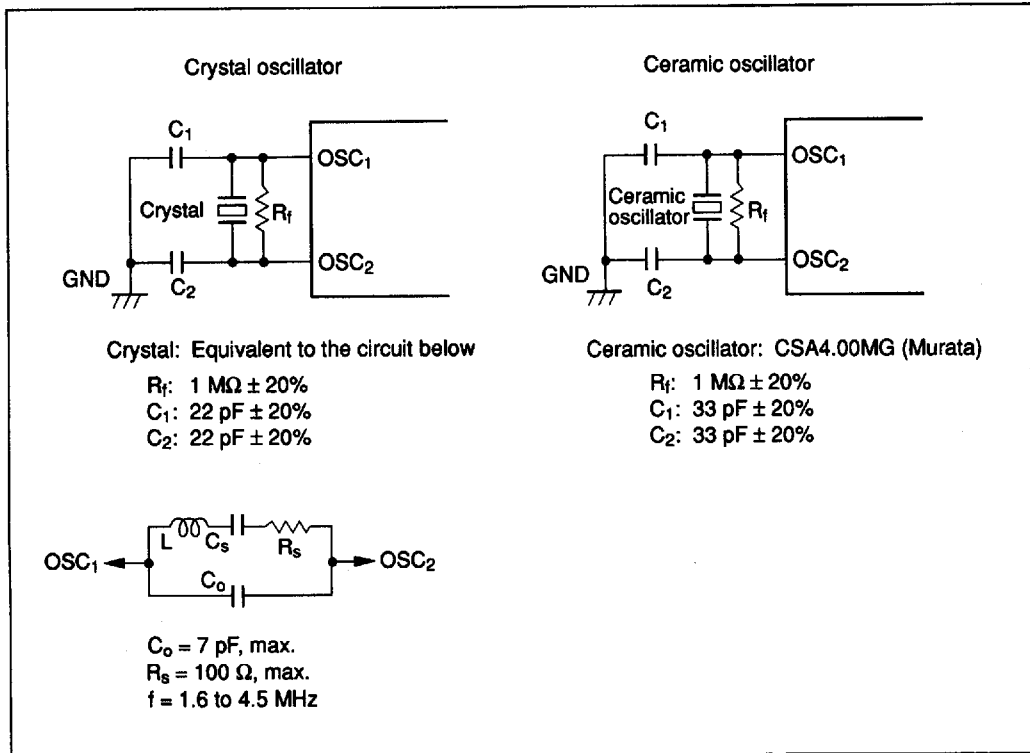


Figure 68 Oscillation Circuits (1)

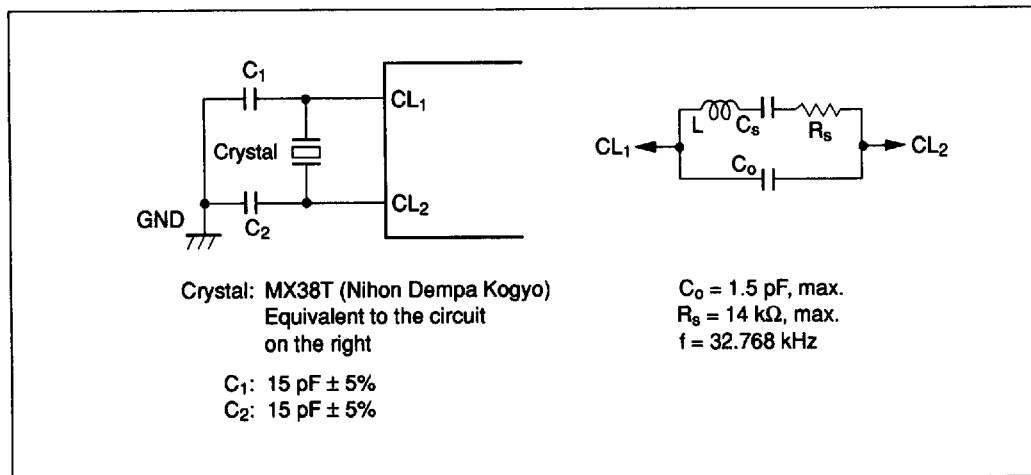


Figure 69 Oscillation Circuits (2)

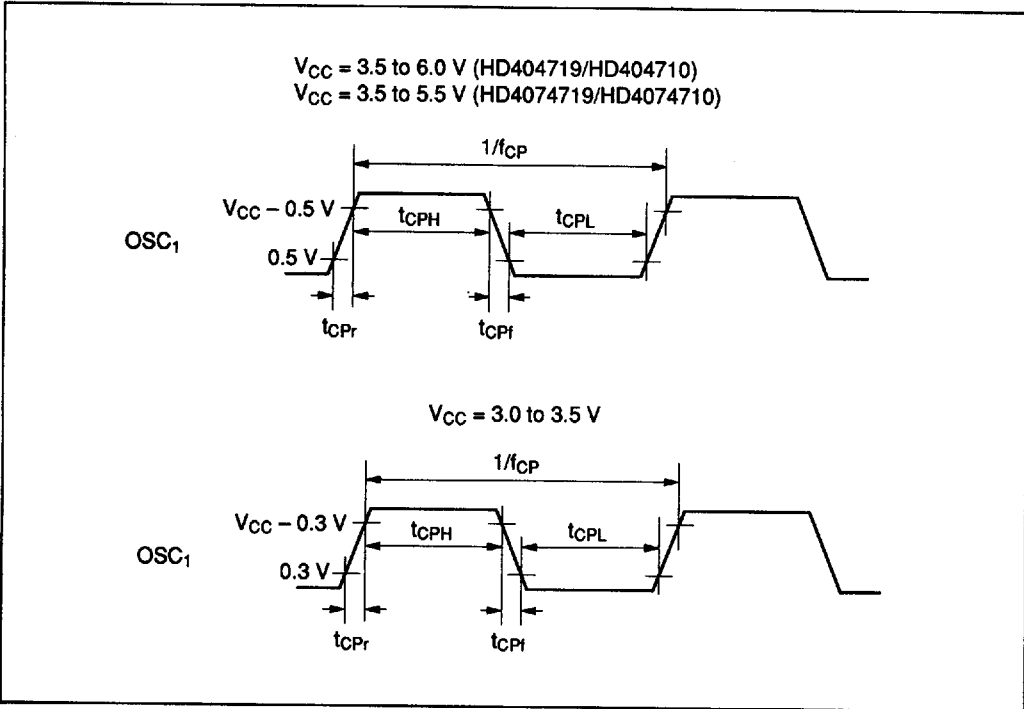


Figure 70 Oscillator Waveforms

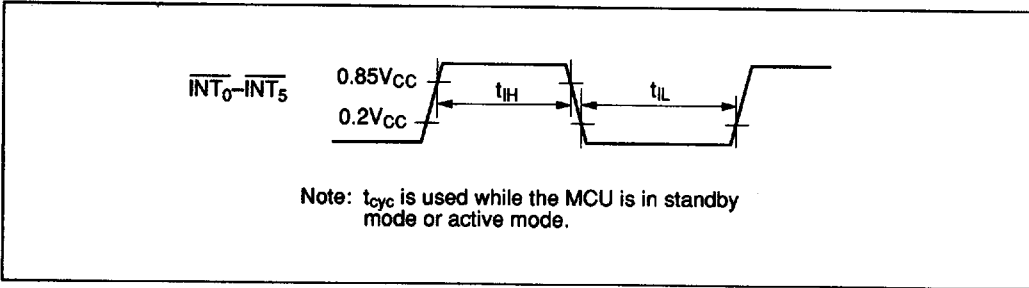


Figure 71 Interrupt Timing

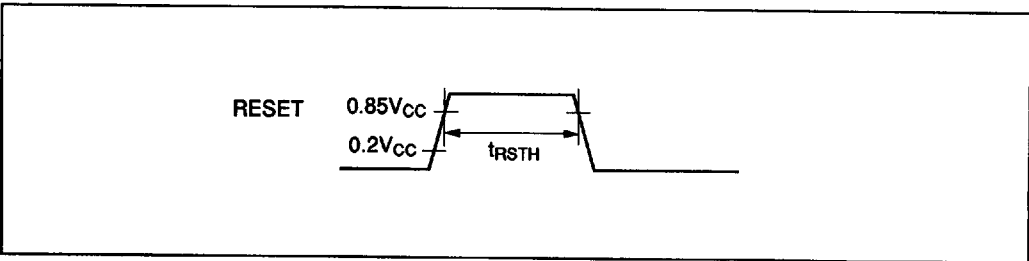
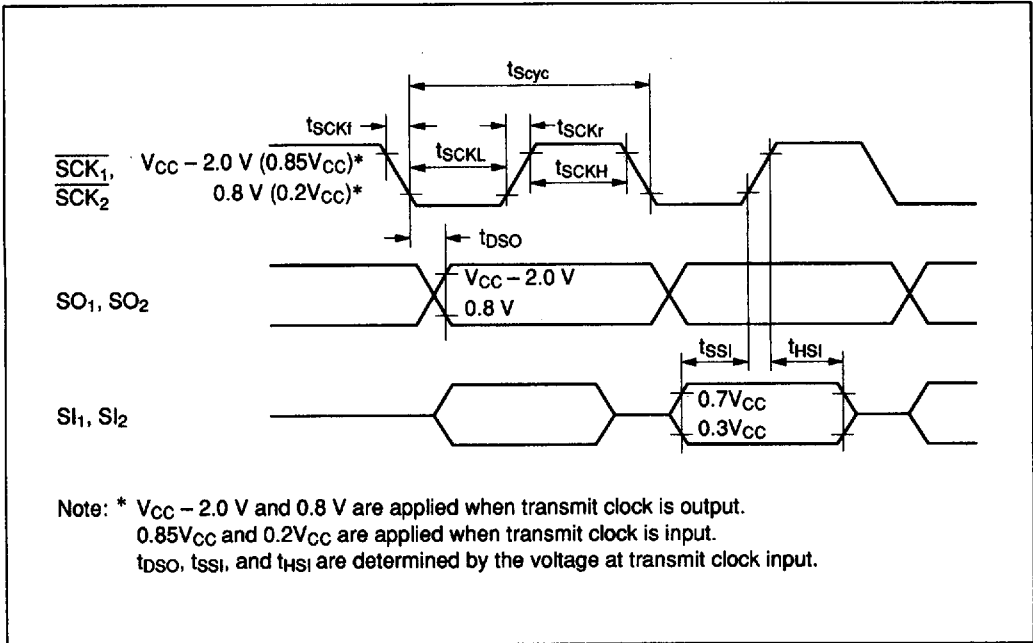
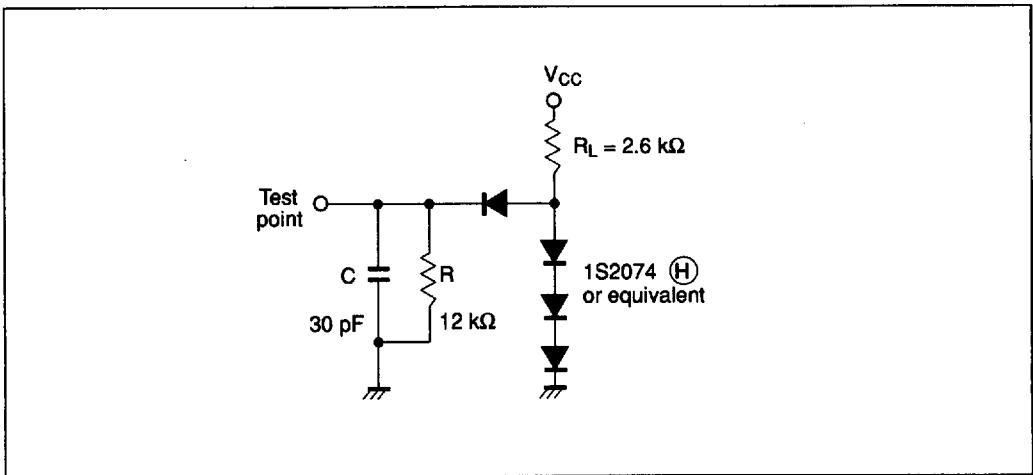


Figure 72 Reset Timing



**Figure 73 Serial Interface Timing**



**Figure 74 Load Circuit for Timing Measurement**

HD404719 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. Optional Functions

<input type="checkbox"/> With 32-kHz CPU operation, with time-base for clock
<input type="checkbox"/> Without 32-kHz CPU operation, with time-base for clock
<input type="checkbox"/> Without 32-kHz CPU operation, without time-base

Note: \* Options marked with an asterisk require a subsystem crystal oscillator (CL1, CL2).

2. I/O Options (shaded options are not available)

- B: With pull-up MOS                      C: Without pull-up MOS  
 D: Without pull-down MOS              E: With pull-down MOS

Pin name	I/O	I/O option			
		B	C	D	E
D0	I/O				
D1	I/O				
D2	I/O				
D3	I/O				
D4	I/O				
D5	I/O				
D6	I/O				
D7	I/O				
D8	I/O				
D9	I/O				
D10	I/O				
D11	I/O				
D12	I/O				
D13	I/O				
D14	I/O				
D15	I/O				
R0	I/O				
R00	I/O				
R01	I/O				
R02	I/O				
R03	I/O				
R1	I/O				
R10	I/O				
R11	I/O				
R12	I/O				
R13	I/O				
R2	I/O				
R20	I/O				
R21	I/O				
R22	I/O				
R23	I/O				
R3	I/O				
R30	I/O				
R31	I/O				
R32	I/O				
R33	I/O				
R4	I/O				
R40	I/O				
R41	I/O				
R42	I/O				
R43	I/O				

Pin name	I/O	I/O option			
		B	C	D	E
R5	R50	Checklist 3			
	R51				
	R52				
	R53				
R6	R60				
*1	R61				
	R62				
	R63				
R7	R70				
	R71				
	R72				
	R73				
R8	R80				
	R81				
	R82				
	R83				
R9	R90				
	R91				
	R92				
	R93				
RA	RA0				
	RA1				
	RA2				
	RA3				
RB	RB0				
	RB1				
RC	RC0				
*2	RC1				
	RC2				
	RC3				
RD	RD0				
*2	RD1				
	RD2				
	RD3				

Notes: 1. When a comparator is used, select pins R60/COMP and R61/Vref without pull-up MOS (I/O option C).  
 2. When pins RC and RD are used for analog input, select them without pull-up MOS (I/O option C).

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## HD404710 Series

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### 3. R50/Vdisp

- |   |
|---|
| <input type="checkbox"/> R50: Without pull-down MOS (D) |
| <input type="checkbox"/> Vdisp                          |

Note: If even one high-voltage pin is selected with I/O option E, pin R50/Vdisp must be selected to function as Vdisp.

### 4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

- |  |
|--|
| <input type="checkbox"/> EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...). |
| <input type="checkbox"/> EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.   |

### 5. OSC1 and OSC2 Oscillator

<input type="checkbox"/> Ceramic oscillator	f =	MHz
<input type="checkbox"/> Crystal oscillator	f =	MHz
<input type="checkbox"/> External clock	f =	MHz

### 6. Stop Mode

- |                                   |
|-----------------------------------|
| <input type="checkbox"/> Used     |
| <input type="checkbox"/> Not used |

### 7. Package

- |                                 |
|---------------------------------|
| <input type="checkbox"/> FP-80A |
| <input type="checkbox"/> FP-80B |

HD404710 Option List

Please check off the appropriate applications and enter the necessary information.

1. Optional Functions

- \*  With 32-kHz CPU operation, with time-base for clock
- \*  Without 32-kHz CPU operation, with time-base for clock
- Without 32-kHz CPU operation, without time-base

Note: \* Options marked with an asterisk require a subsystem crystal oscillator (CL1, CL2).

2. I/O Options (shaded options are not available)

- B: With pull-up MOS
- C: Without pull-up MOS
- D: Without pull-down MOS
- E: With pull-down MOS

Order date		
Customer name		
Department		
Name		
ROM code	16-k program ROM	
	8-k pattern ROM	
LSI number (Hitachi's entry)		

Pin name	I/O	I/O option			
		B	C	D	E
D0	I/O				
D1	I/O				
D2	I/O				
D3	I/O				
D4	I/O				
D5	I/O				
D6	I/O				
D7	I/O				
D8	I/O				
D9	I/O				
D10	I/O				
D11	I/O				
D12	I/O				
D13	I/O				
D14	I/O				
D15	I/O				
R0	R00				
	R01				
	R02				
	R03				
R1	R10				
	R11				
	R12				
	R13				
R2	R20				
	R21				
	R22				
	R23				
R3	R30				
	R31				
	R32				
	R33				
R4	R40				
	R41				
	R42				
	R43				

Pin name	I/O	I/O option			
		B	C	D	E
R5	R50				
	R51				
	R52				
	R53				
*1	R60				
	R61				
	R62				
	R63				
R7	R70				
	R71				
	R72				
	R73				
	R73				
R8	R80				
	R81				
	R82				
	R83				
	R83				
R9	R90				
	R91				
	R92				
	R93				
	R93				
RA	RA0				
	RA1				
	RA2				
	RA3				
RB	RB0				
	RB1				
*2	RC0				
	RC1				
	RC2				
	RC3				
RD	RD0				
	RD1				
	RD2				
	RD3				

Notes: 1. When a comparator is used, select pins R60/COMP and R61/Vref without pull-up MOS (I/O option C).  
 2. When pins RC and RD are used for analog input, select them without pull-up MOS (I/O option C).

## HD404710 Series

### 3. R50/Vdisp

R50: Without pull-down MOS (D)

Vdisp

Note: If even one high-voltage pin is selected with I/O option E, pin R50/Vdisp must be selected to function as Vdisp.

### 4. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).

EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

### 5. OSC1 and OSC2 Oscillator

Ceramic oscillator      f =      MHz

Crystal oscillator      f =      MHz

External clock      f =      MHz

### 6. Stop Mode

Used

Not used

### 7. Package

FP-80B