National Semiconductor

DM7546/DM8546 TRI-STATE® 8-Bit Universal I/O Shift Registers

General Description

These circuits are TRI-STATE, 8-bit, edge-triggered, universal shift registers which are capable of operating in any of the following modes: shift left, shift right, parallel load, or inhibit. Since the clock is edge-triggered, the control lines which determine the mode of operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

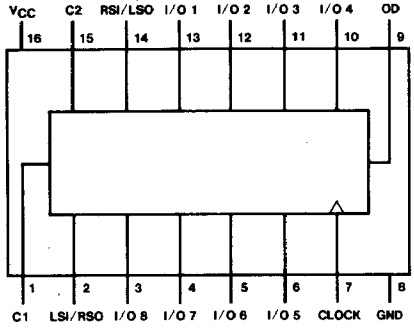
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Features

- Positive-edge triggered clock
- "Do nothing" state without gating the clock
- Both parallel and serial data lines are TRI-STATE
- High impedance state does not impede shift mode with parallel outputs

Connection Diagram

Dual-In-Line Package



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Recommended Operating Conditions

Symbol	Parameter		DM7546			DM8546			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		15	0		15	MHz
t_W	Clock Pulse Width		18	12		18	12		ns
$t_{SETUP\ (HIGH)}$	Serial Data	$C_L = 50$ pF, $R_L = 400\Omega$	38	25		38	25		ns
$t_{SETUP\ (HIGH)}$	Parallel Data		33	22		33	22		ns
$t_{SETUP\ (LOW)}$	Serial Data		21	14		21	14		ns
$t_{SETUP\ (LOW)}$	Parallel Data		18	12		18	12		ns
$t_{HOLD\ (HIGH)}$	Serial Data		0	−11		0	−11		ns
$t_{HOLD\ (HIGH)}$	Parallel Data		0	−11		0	−11		ns
$t_{HOLD\ (LOW)}$	Serial Data		0	−22		0	−22		ns
$t_{HOLD\ (LOW)}$	Parallel Data		0	−21		0	−21		ns
SETUP AND HOLD TIMES BETWEEN CHANGES IN MODE CONTROL AND CLOCKING									
t_{SETUP}	Parallel Load to Right Shift	$C_L = 50$ pF, $R_L = 400\Omega$	32	21		32	21		ns
t_{SETUP}	Parallel Load to Left Shift		40	27		40	27		ns
t_{SETUP}	Right Shift to Parallel Load		60	40		60	40		ns
t_{SETUP}	Left Shift to Parallel Load		53	35		53	35		ns
t_{SETUP}	Right Shift to Left Shift		33	21		33	21		ns
t_{SETUP}	Left Shift to Right Shift		56	37		56	37		ns
t_{SETUP}	Inhibit to Right Shift		57	38		57	38		ns
t_{SETUP}	Inhibit to Left Shift		65	43		65	43		ns
t_{SETUP}	Right Shift to Inhibit		50	33		50	33		ns
t_{SETUP}	Left Shift to Inhibit		50	32		50	32		ns
t_{HOLD}	Parallel Load to Right Shift		9	6		9	6		ns
t_{HOLD}	Parallel Load to Left Shift		6	4		6	4		ns
t_{HOLD}	Right Shift to Parallel Load		0	−13		0	−13		ns
t_{HOLD}	Left Shift to Parallel Load		0	−46		0	−46		ns
t_{HOLD}	Right Shift to Left Shift		0	−10		0	−10		ns
t_{HOLD}	Left Shift to Right Shift		0	−23		0	−23		ns
t_{HOLD}	Inhibit to Right Shift		0	−18		0	−18		ns
t_{HOLD}	Inhibit to Left Shift		0	−16		0	−16		ns
t_{HOLD}	Right Shift to Inhibit		0	−12		0	−12		ns
t_{HOLD}	Left Shift to Inhibit		0	−29		0	−29		ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	C2			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	C2			−3.2	mA
			Other			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−30		−70	mA
			DM85	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max	DM75		80	115	mA
			DM85		80	125	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

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Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX} Maximum Clock Frequency					15	22		MHz
t_{PLH} Propagation Delay Time Low to High Level Output						16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output						27	40	ns
t_{PZH} Output Enable Time to High Level Output	Output Control to Q					22	33	ns
t_{PZH} Output Enable Time to High Level Output	Mode Control (C1/C2) to Q					13	20	ns
t_{PZL} Output Enable Time to Low Level Output	Output Control to Q					18	27	ns
t_{PZL} Output Enable Time to Low Level Output	Mode Control (C1/C2) to Q					15	23	ns
t_{PHZ} Output Disable Time from High Level Output	Output Control to Q		5	8				ns
t_{PHZ} Output Disable Time from High Level Output	Mode Control (C1/C2) to Q		9	14				ns
t_{PLZ} Output Disable Time from Low Level Output	Output Control to Q		16	24				ns
t_{PLZ} Output Disable Time from Low Level Output	Mode Control (C1/C2) to Q		17	26				ns

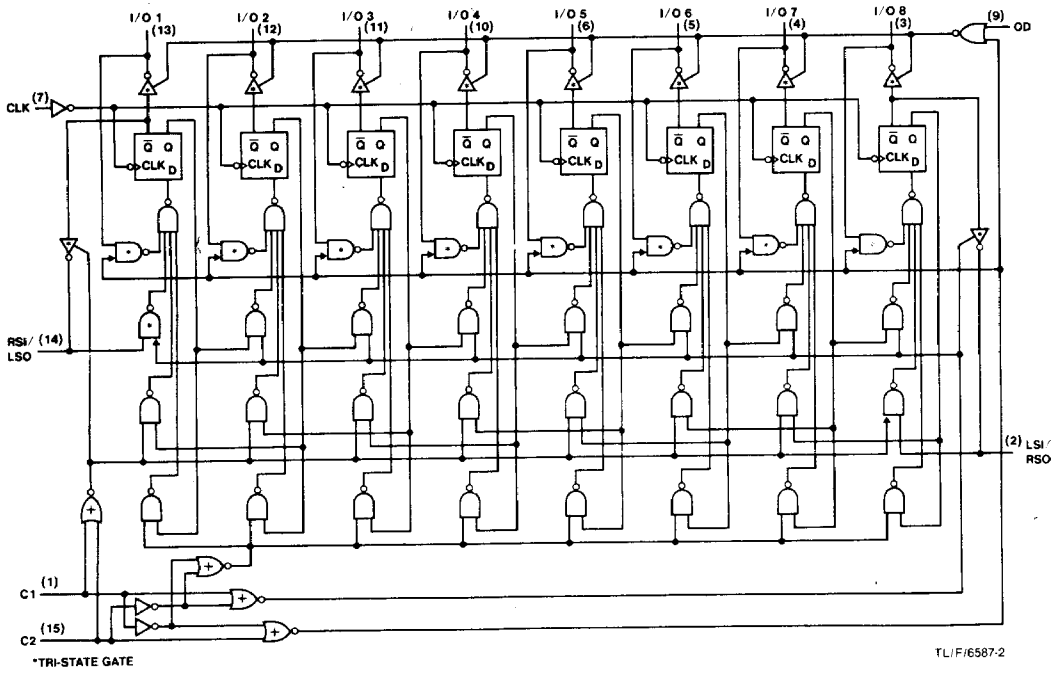
Function Table

OD	C1	C2	Mode of Operation	State of Parallel I/O	State of Serial I/O	
					RSI/LSO	LSI/RSO
L	H	H	Inhibit	Q_{OUT}	Hi-Z*	Hi-Z*
H	H	H	Inhibit	Hi-Z*	Hi-Z*	Hi-Z*
X	H	L	Parallel Load	Data In	Hi-Z*	Hi-Z*
L	L	H	Right Shift	Q_{OUT}	Data In	Q_{OUT} 8
H	L	H	Right Shift	Hi-Z*	Data In	Q_{OUT} 8
L	L	L	Left Shift	Q_{OUT}	Q_{OUT} 1	Data In
H	L	L	Left Shift	Hi-Z*	Q_{OUT} 1	Data In

OD = Output Disable (C1, C2 = Mode Controls)

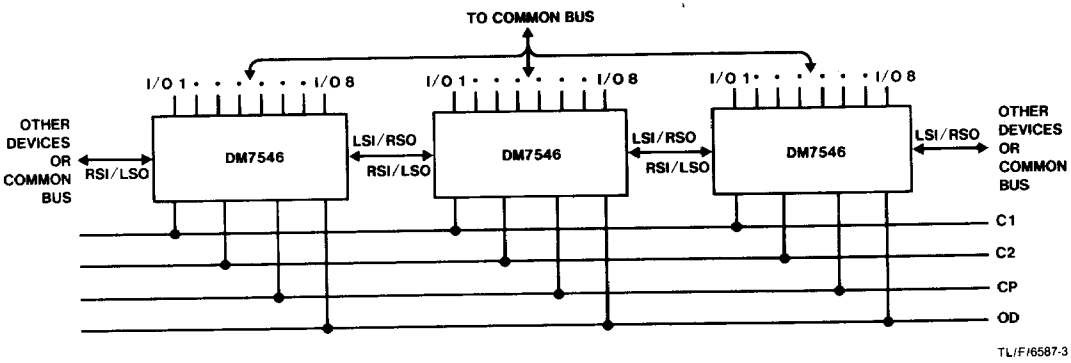
*Both Input and Output of the I/O pin are in the high impedance state.

Logic Diagram



Typical Applications

Cascading Devices



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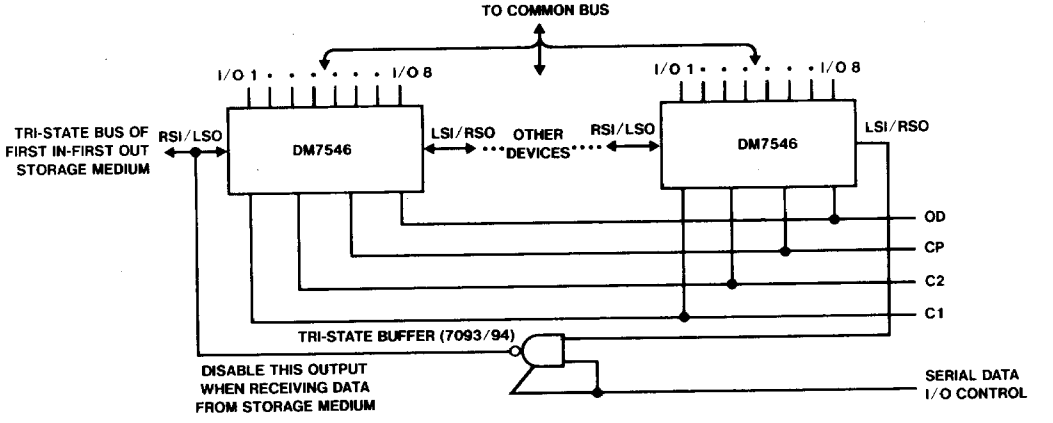
Serial Data Transfer to a First In-First Out Storage Medium



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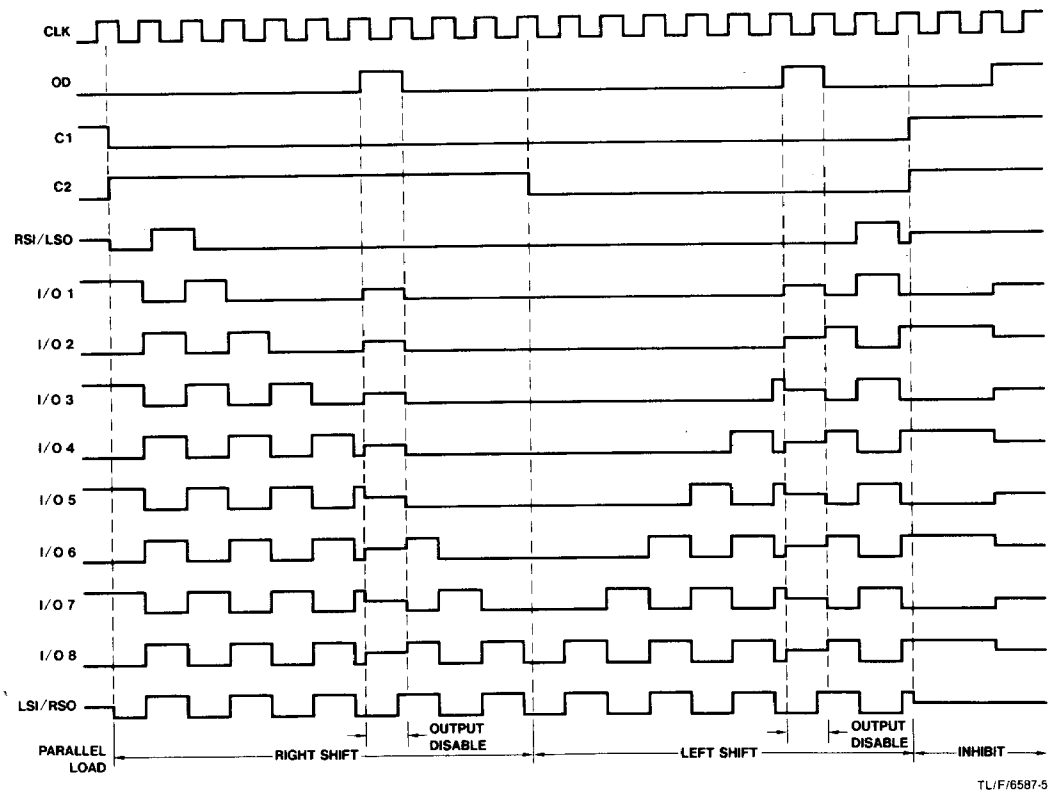
Typical Applications (Continued)

Typical Parallel Load, Right Shift, Left Shift and Inhibit Sequences



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