MOTOROLA

Military 54LS280

9-Bit Odd/Even Parity Generator/Checker

ELECTRICALLY TESTED PER:
MIL-M-38510/32901

The 54LS280 is a Universal 9-Bit Parity Generator/Checker. It features odd/even outputs to facilitate either odd or even parity. By cascading, the word length is easily expanded.

The 'LS280 is designed without the expander input implementation, but the corresponding function is provided by an input at pin 4 and the absence of any connection at pin 3. This design permits the 'LS280 to be substituted for the 'LS180 which results in improved performance. The 'LS280 has buffered inputs to lower the drive requirements to one LS unit load.

- Generates Either Odd or Even Parity for Nine Data Lines
- Typical Data-to-Output Delays of Only 33 ns
- Cascadable for n-Bits
- Can Be Used to Upgrade Systems Using MSI Parity Circuits
- Typical Power Dissipation = 80 mW

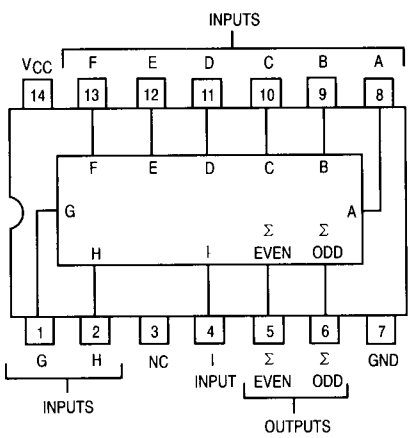
AVAILABLE AS:

1) JAN: JM38510/32901BXA
2) SMD: N/A
3) 883: 54LS280/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
G	1	1	2	V_{CC}
H	2	2	3	V_{CC}
NC	3	3	4	OPEN
I	4	4	6	GND
ΣE	5	5	8	V_{CC}
ΣO	6	6	9	OPEN
GND	7	7	10	GND
A	8	8	12	V_{CC}
B	9	9	13	V_{CC}
C	10	10	14	GND
D	11	11	16	V_{CC}
E	12	12	18	V_{CC}
F	13	13	19	GND
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

FUNCTION TABLE

Number of Inputs A thru I that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

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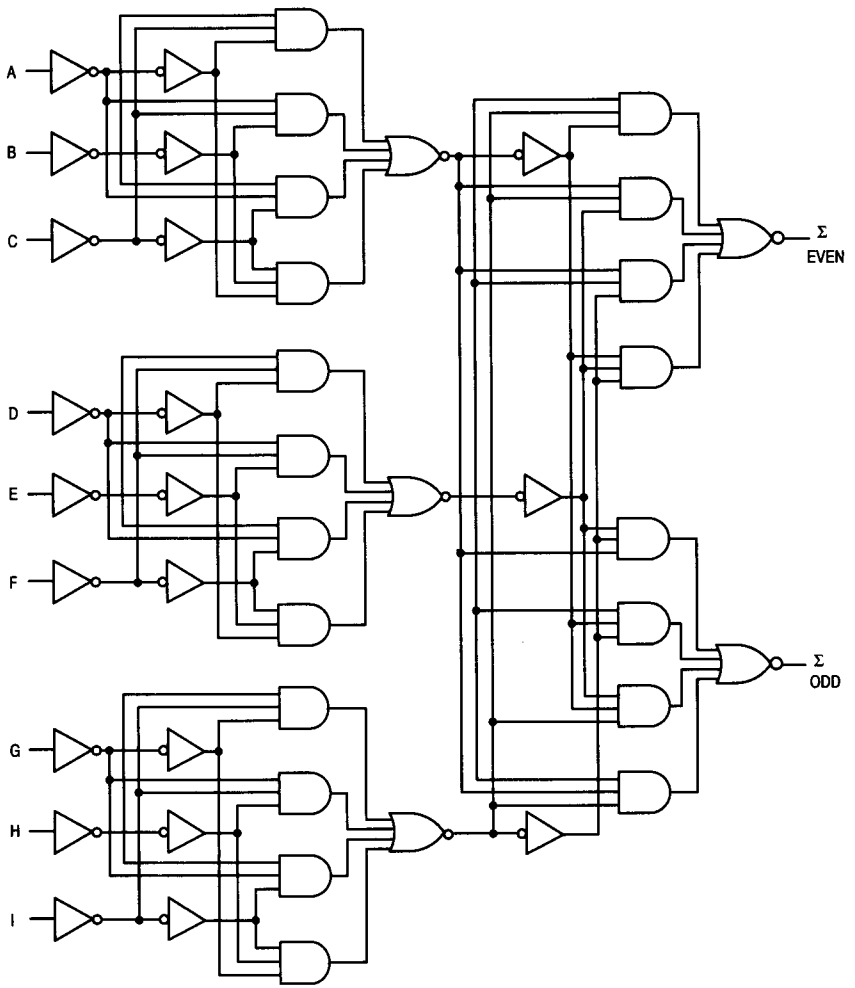
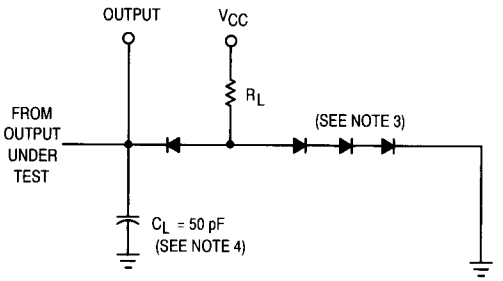
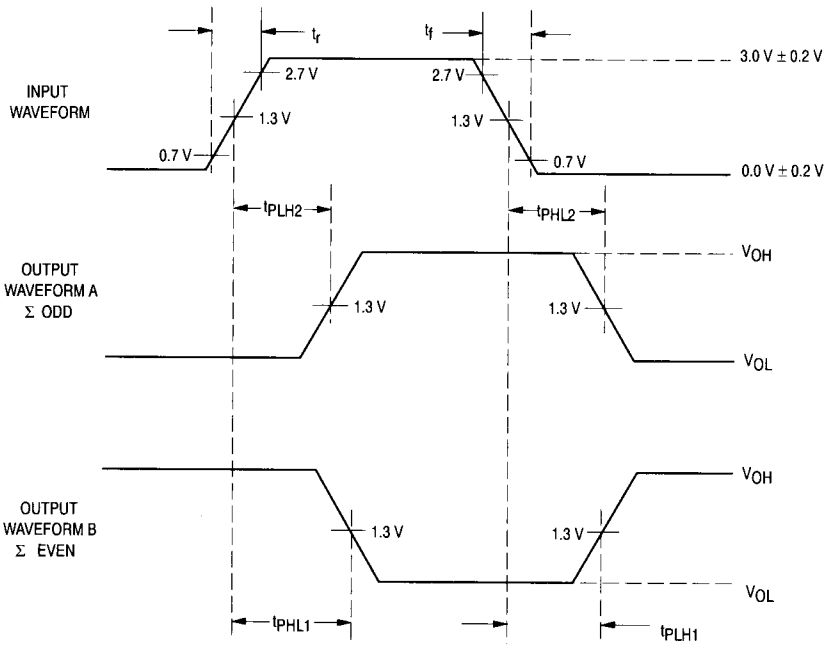
LOGIC DIAGRAM



TEST CIRCUIT AND WAVEFORMS



(LOAD FOR OUTPUT UNDER TEST)



NOTES:

1. The input pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz.
2. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance.
3. R_L = 2.0 kΩ ± 5.0%. All diodes are 1N3064 or 1N916.
4. Voltage measurements are to be made with respect to network ground terminal.
5. The limits specified for C_L = 15 pF are guaranteed but not tested.
6. Terminal conditions (pins not designated may be high ≥ 2.0 V, or low ≤ 0.7 V, or open).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IN} = 0.7 V all inputs, A = 0.7 V or 2.0 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V (all inputs), A = 2.0 V or 0.7 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, V_{IN} = GND, A = GND or 4.5 V, V_{OUT} = GND.
I_{IL}	Logical "0" Input Current	− 130	− 370	− 130	− 370	− 130	− 370	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{CC}	Power Supply Current Off		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output High-Low	2.0	50	2.0	65	2.0	65	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH1}	Propagation Delay /Data-Output Low-High	2.0	55	2.0	72	2.0	72	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL2}	Propagation Delay /Data-Output High-Low	2.0	40	2.0	72	2.0	72	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH2}	Propagation Delay /Data-Output Low-High	2.0	55	2.0	52	2.0	52	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ