BURR - BROWN®

PCM1760P/U
DF1760P/U

Multi-Bit Enhanced Noise Shaping 20-Bit ANALOG-TO-DIGITAL CONVERSION SYSTEM

FEATURES

- **DUAL 20-BIT MONOLITHIC MODULATOR (PCM1760) AND MONOLITHIC DECIMATING DIGITAL FILTER (DF1760)**
- **HIGH PERFORMANCE:**
  THD+N: –92dB typ, –90dB max
  Dynamic Range: 108dB typ
  SNR: 108dB min, 110dB typ
  Channel Separation: 98dB typ, 94dB min
- **64X OVERSAMPLING**
- **CO-PHASE CONVERSION**
- **RUNS ON 256fs OR 384fs SYSTEM CLOCK**
- **VERSATILE INTERFACE CAPABILITY:**
  16-, 20-Bit Output
  MSB First or LSB First Format
- **OPTIONAL FUNCTIONS:**
  Offset Error Calibration
  Overflow Detection
  Power Down Mode (DF1760)
- **RUNS ON ±5V SUPPLIES (PCM1760) AND 5V SUPPLY (DF1760)**
- **COMPACT 28-PIN PACKAGES:**
  28-Pin DIP and SOIC

DESCRIPTION

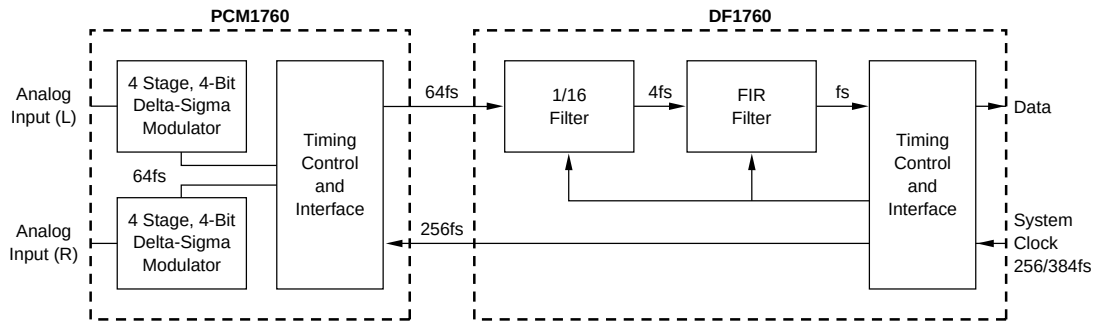
The PCM1760 and DF1760 combine for a low-cost, high-performance dual 20-bit, 48kHz sampling analog-to-digital conversion system which is specifically designed for dynamic applications.

The PCM1760/DF1760 pair form a 4-bit, 4th order, 64X oversampling analog-to-digital converter.

The PCM1760 is a delta-sigma modulator that uses a 4-bit quantizer within the modulation loop to achieve very high dynamic range.

The DF1760 is a high-performance decimating digital filter. The DF1760 accepts 4-bit 64fs data from the PCM1760 and decimates to 20-bit 1fs data.

The FIR filter of the DF1760 has pass-band ripple of less than ±0.001dB and greater than 100dB of the reject band attenuation.



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SBAS025

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$, $\pm V_{dd}$ = +5V, $+V_{DD}$ = +5V, f_S = 48kHz and ext. components = ±2% unless otherwise noted.

PARAMETER		CONDITIONS	PCM1760/DF1760 MIN	PCM1760/DF1760 TYP	PCM1760/DF1760 MAX	UNITS
RESOLUTION			20			Bits
ANALOG INPUT						
Input Range		$R_{IN}1$ = 2.2kΩ		±2.5		Vp-p
Input Impedance		$R_{IN}1$ = 2.2kΩ		$R_{IN}1$		Ω
SAMPLING FREQUENCY						
Cover Range of fs		Integrator Constants: Application(1)	30	48	50	kHz
ACCURACY						
Gain Error				±0.5	±1.0	dB
Gain Mismatch					±0.5	dB
Bipolar Zero Error		V_{IN} = 0 at 20s After Power-On			±0.4	% FSR(2)
Gain Drift		0°C to +70°C		±100		ppmfs/°C
Bipolar Zero Drift		0°C to +70°C		±20		ppmfs/°C
DYNAMIC CHARACTERISTICS(4)						
THD+N/(0dBFS)	P, U	f_{IN} = 1kHz		–92	–90	dB
	P-L, U-L			–90	–88	dB
THD+N/(–20dBFS)	P, U	f_{IN} = 1kHz		–76	–70	dB
	P-L, U-L			–76	–70	dB
THD+N/(–60dBFS)	P, U	f_{IN} = 1kHz		–44	–42	dB
	P-L, U-L			–44	–42	dB
Dynamic Range	P, U	f_{IN} = 1kHz, V_{IN} = –60dBFS, A Filter	104	108		dB
	P-L, U-L		104	108		dB
SNR	P, U	V_{IN} = 0, A Filter	108	110		dB
	P-L, U-L		106	110		dB
Frequency Response		f_{IN} = 20kHz		±0.1		dB
Channel Separation		f_{IN} = 1kHz, A Filter	94	98		dB
DIGITAL FILTER						
Over Sample Rate				64		fs
Ripple in Band		0 - 0.04535fs			±0.0001	dB
Stopband Attenuation –1		0.5465fs - 63.4535fs	–94			dB
Stopband Attenuation –2		0.5465fs - 3.4535fs	–100			dB
LOGIC INPUTS AND OUTPUTS						
Logic Family Input				TTL Level Compatible CMOS		
Frequency (System Clock 1)		256fs		12.288		MHz
Frequency (System Clock 2)		384fs		18.432		MHz
Duty Cycle (System Clock 1)		256fs	40	50	60	%
Duty Cycle (System Clock 2)		384fs	45	50	55	%
Data Clock Input			32	48	64	fs
Logic Family Output				CMOS		
Data Clock Output				64		fs
Data Coding				Two's Complement		
Data Bit Length			16	20		Bits
Data Format				Selectable		
Output Data Delay		fs = 48kHz		1.5		ms
POWER SUPPLY REQUIREMENTS						
Supply Voltage						
$\pm V_{CC}$		PCM1760	±4.75	±5.0	±5.25	V
$\pm V_{dd}$		PCM1760	±4.75	±5.0	±5.25	V
$+V_{DD}$		DF1760	4.75	5.0	5.25	V
Supply Current						
$+I_{CC}$		PCM1760		24	36	mA
$-I_{CC}$		PCM1760		–30	–45	mA
$+I_{dd}$		PCM1760		12	18	mA
$-I_{DD}$		PCM1760		–8	–12	mA
$+I_{DD}$ –1		DF1760, Normal Mode		40	55	mA
$+I_{DD}$ –2		DF1760, Power-Down Mode		4	6.6	mA
Power Consumption		PCM1760		370	500	mW
		DF1760, Normal Mode		200	275	mW
		DF1760, Power-Down Mode		20	33	mW
TEMPERATURE RANGE						
Operating		PCM1760/DF1760	0	+25	+70	°C
Storage		PCM1760/DF1760	–50		+125	°C

NOTES: (1) Integrator Constants are determined by the external components shown in the block diagram. (2) FSR means Full Scale Range, digital output code is from 90000H to 70000H, FSR = 5.0V. (3) Use 20-bit DAC, 20kHz LPF, 400Hz HPF, average response. (4) Average response using a 20-bit reconstruction DAC with 20kHz low-pass filter and 400Hz high-pass filter.

ABSOLUTE MAXIMUM RATINGS—PCM1760

Supply Voltage	±6V
Voltage Mismatch	0.1V
Analog Input	$\pm V_{CC}$
Digital Input	$+V_{DD}$ +0.3V
	GND –0.3V
Power Dissipation/P	580mW
Power Dissipation/U	550mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s)	235°C
Operating Temperature	0°C to +70°C
Storage Temperature	–50°C to +125°C

ABSOLUTE MAXIMUM RATINGS—DF1760

Supply Voltage	7.0V
Voltage Mismatch	0.1V
Digital Input	$+V_{DD}$ +0.5V
	V_{SS} –0.5V
Input Current	±20mA
Power Dissipation/P	460mW
Power Dissipation/U	440mW
Lead Temperature/P (soldering, 10s)	260°C
Lead Temperature/U (soldering, 10s, reflow)	235°C
Operating Temperature	0°C to +70°c
Storage Temperature	–50°C to +125°C

ORDERING INFORMATION

MODEL	PACKAGE	THD +N (fs)	SNR
PCM1760P	PDIP	–90dB	108dB
PCM1760U	SOIC	–90dB	108dB
PCM1760P-L	PDIP	–88dB	106dB
PCM1760U-L	SOIC	–88dB	106dB
DF1760P	PDIP	NA	NA
DF1760U	SOIC	NA	NA

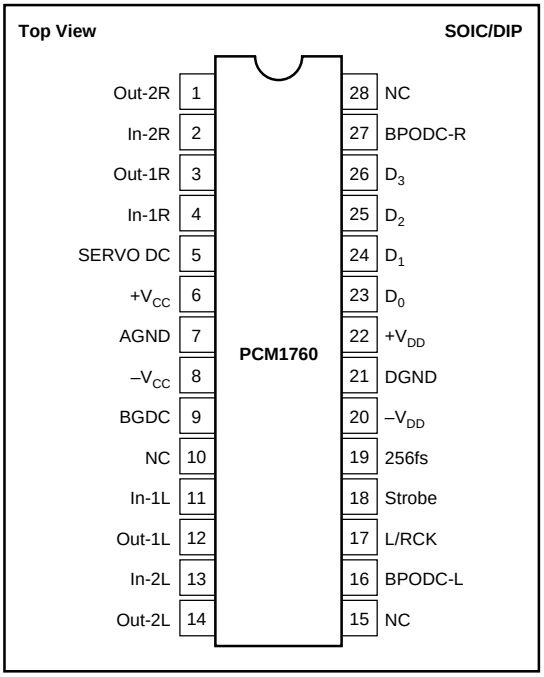
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
PCM1760P	28-Pin PDIP	800
PCM1760U	28-Pin SOIC	804
PCM1760P-L	28-Pin PDIP	800
PCM1760U-L	28-Pin SOIC	804
DF1760P	28-Pin PDIP	801
DF1760U	28-Pin SOIC	805

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN ASSIGNMENTS PCM1760

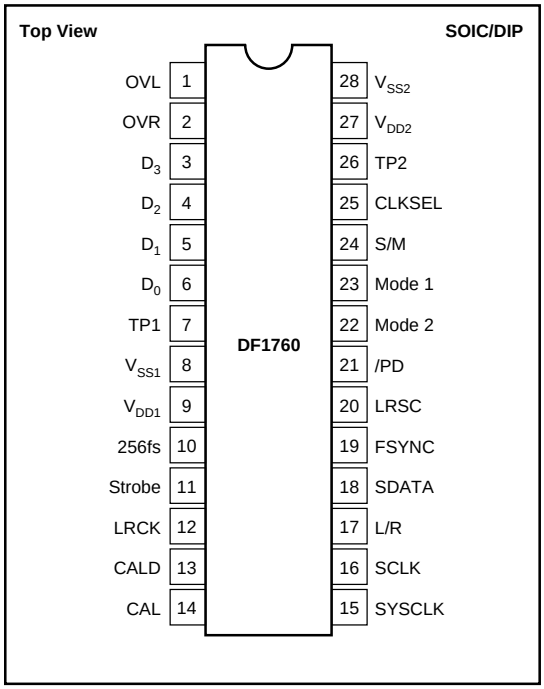
Top View **SOIC/DIP**



PIN	I/O[1]	NAME	DESCRIPTION
1	O	Out-2R	Right Channel Second Integrator Output
2	I	In-2R	Right Channel Second Integrator Input
3	O	Out-1R	Right Channel First Integrator Output
4	I	In-1R	Right Channel First Integrator Input
5	–	SERVO DC	Servo Amp Decoupling Capacitor
6	–	$+V_{CC}$	+5V Analog Supply Voltage
7	–	AGND	Analog Common
8	–	$–V_{CC}$	–5V Analog Supply Voltage
9	–	BGDC	Band Gap Reference Decoupling Capacitor
10	–	NC	No Connection
11	I	In-1L	Left Channel First Integrator Input
12	O	Out-1L	Left Channel First Integrator Output
13	I	In-2L	Left Channel Second Integrator Input
14	O	Out-2L	Left Channel Second Integrator Output
15	–	NC	No Connection
16	–	BPODC-L	Left Channel Bipolar Offset Decoupling Capacitor
17	O	L/RCK	LR Clock Output (64fs)
18	O	Strobe	Data Strobe Output (128fs)
19	I	256fs	256fs Clock Input
20	–	$–V_{DD}$	–5V Digital Supply Voltage
21	–	DGND	Digital Common
22	–	$+V_{DD}$	+5V Digital Supply Voltage
23	O	D_0	D_0 Data Output (LSB)
24	O	D_1	D_1 Data Output
25	O	D_2	D_2 Data Output
26	O	D_3	D_3 Data Output (MSB)
27	–	BPODC-R	Right Channel Bipolar Offset Decoupling Capacitor
28	–	NC	No Connection

NOTE: (1) O = Output terminal; I = Input terminal.

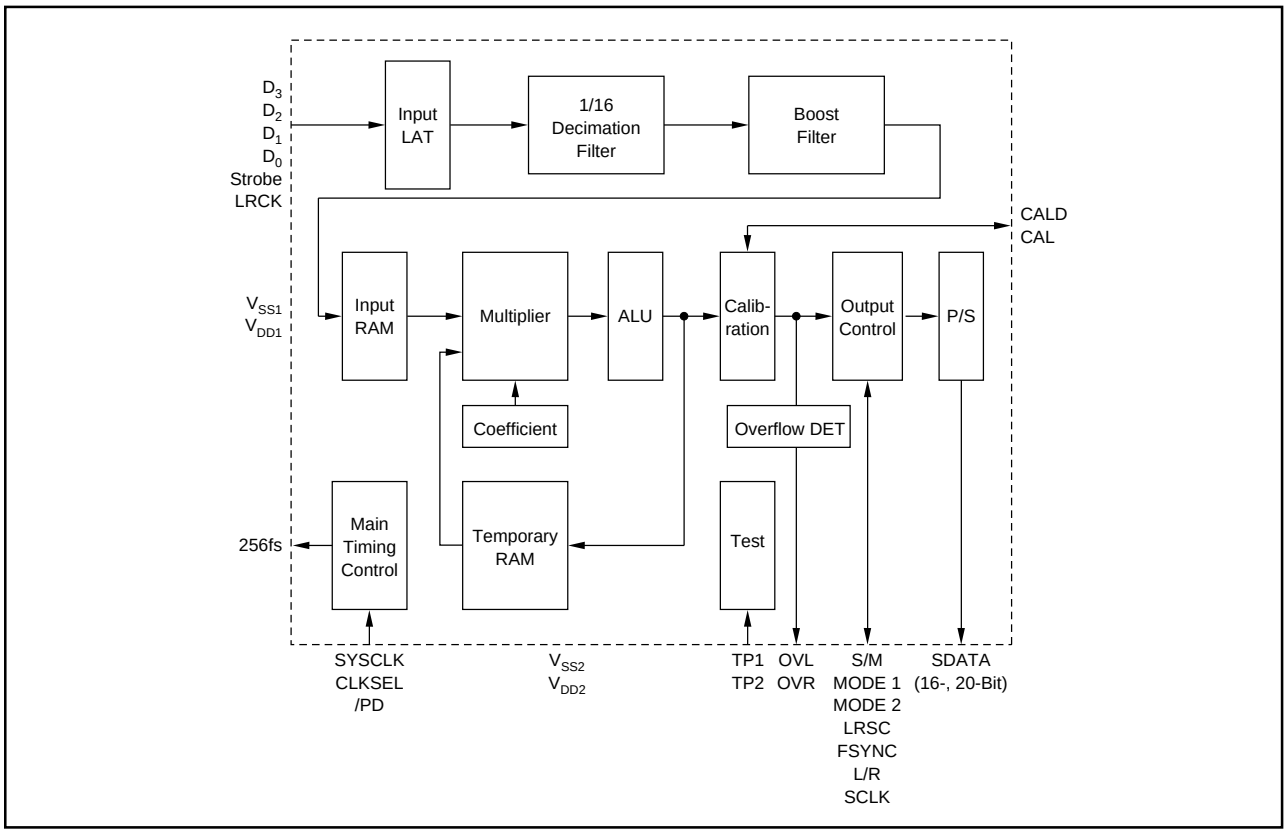
PIN ASSIGNMENTS DF1760



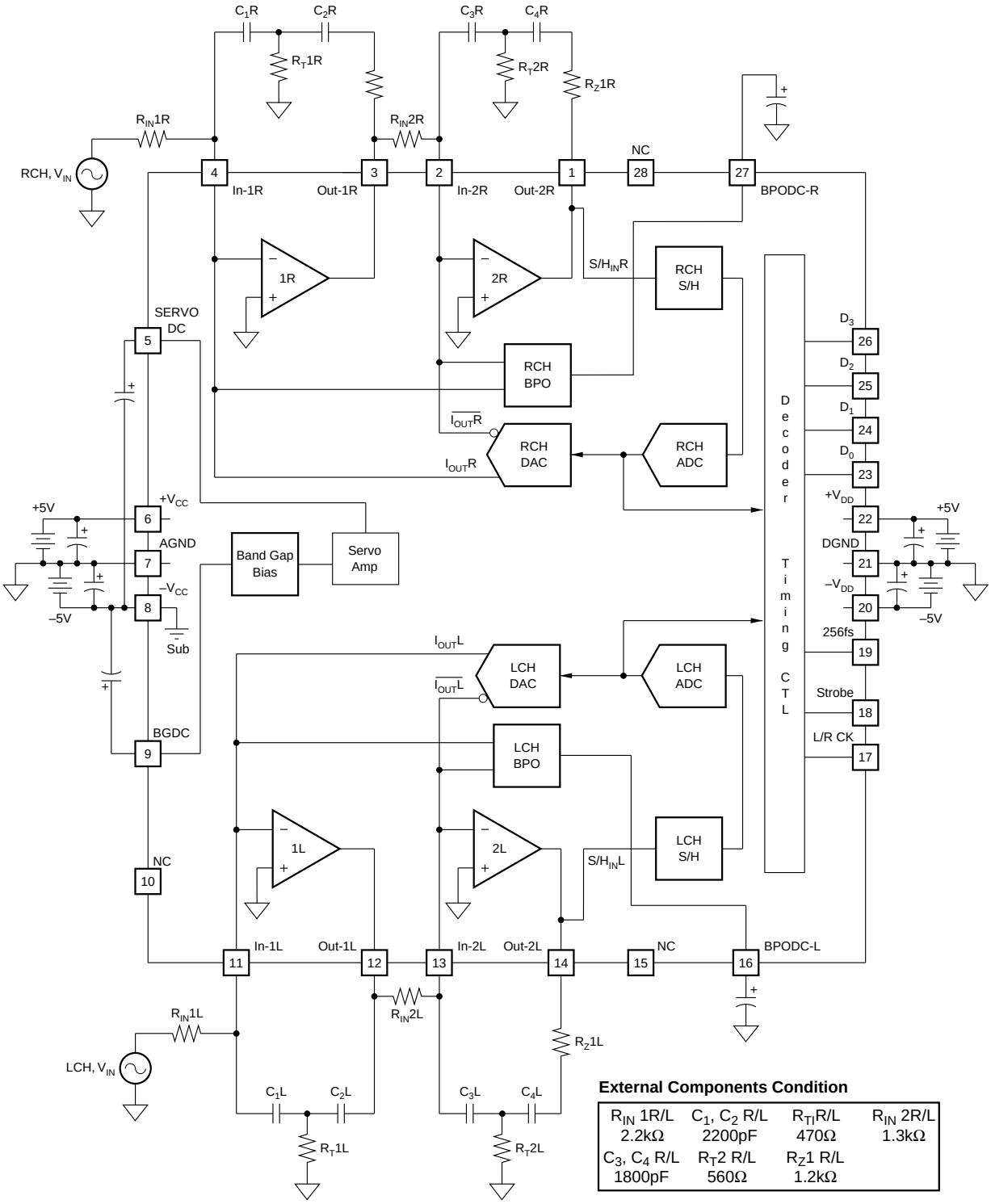
PIN	I/O(1)	NAME	DESCRIPTION
1	O	OVL	Left Channel Overflow Output (Active High)
2	O	OVR	Right Channel Overflow Output (Active High)
3	I	D_3	D3 Data Input (MSB)
4	I	D_2	D2 Data Input
5	I	D_1	D1 Data Input
6	I	D_0	D0 Data Input (LSB)
7	–	TP1	Test Pin (No Connection)
8	–	V_{SS1}	Common Channel 1
9	–	V_{DD1}	+5V Channel 1
10	O	256fs	256fs Clock Output
11	I	Strobe	Data Strobe Clock Input (128fs)
12	I	LRCK	LR Clock Input
13	I↑	CALD	Calibration Function Enable (Active Low)
14	O	CAL	Calibration Output (High During Calibration)
15	I	SYSCLK	System Clock Input (256fs or 384fs)
16	I↑/O	SCLK	Data Clock
17	I↑/O	L/R	LR Channel Phase Clock
18	O	SDATA	Serial Data Output (1fs)
19	I↑/O	FSYNC	Frame Clock (2fs)
20	I↑	LRSC	Phase Control of LR Channel Phase Clock
21	I↑	/PD	Power Down Mode Enable Input (Active Low)
22	I↑	Mode2	Output Format Selection Input 2
23	I↑	Mode1	Output Format Selection Input 1
24	I↑	S/M	Slave/Master Mode Selection Input (High Makes Slave Mode
25	I↑	CLKSEL	System Clock Selection Input (High Makes 256fs)
26	–	TP2	Test Pin (No Connection)
27	–	V_{DD2}	+5V Channel 2
28	–	V_{SS2}	Common Channel 2

NOTE: (1) O = Output terminal; I = Input terminal.

BLOCK DIAGRAM OF DF1760



BLOCK DIAGRAM OF PCM1760

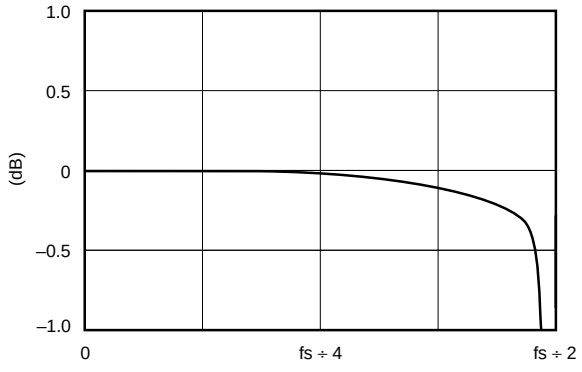


External Components Condition

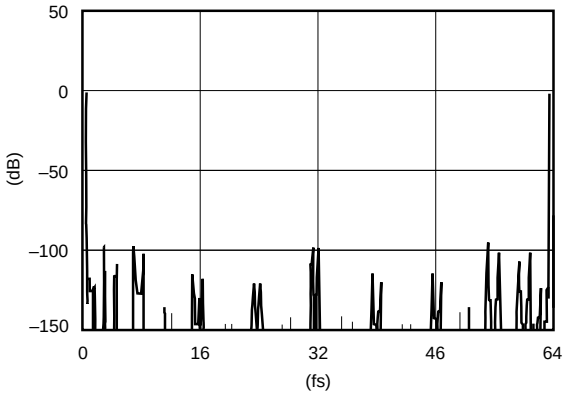
R_{IN} 1R/L 2.2kΩ	C_1, C_2 R/L 2200pF	R_{TI}R/L 470Ω	R_{IN} 2R/L 1.3kΩ
C_3, C_4 R/L 1800pF	R_T2 R/L 560Ω	R_Z1 R/L 1.2kΩ	

TYPICAL PERFORMANCE CURVES

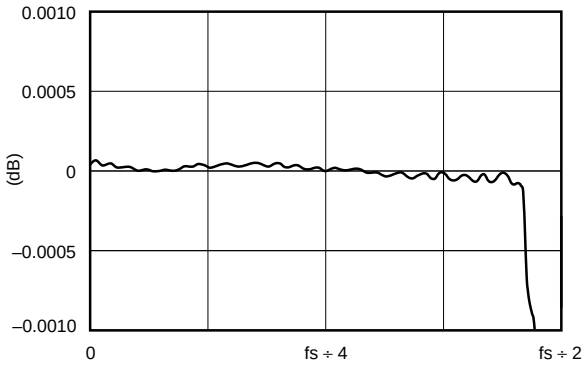
OVERALL PASS-BAND
CHARACTERISTICS OF THE DF1760



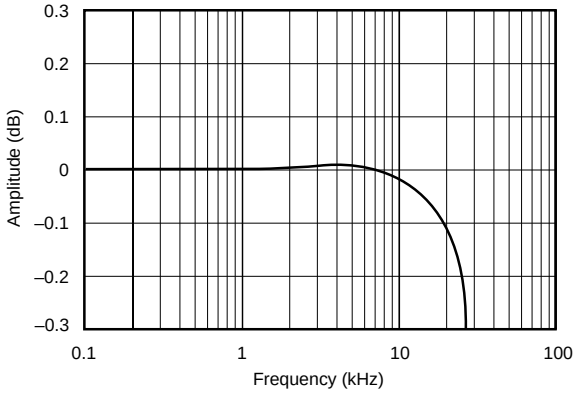
OVERALL CHARACTERISTICS OF THE DF1760



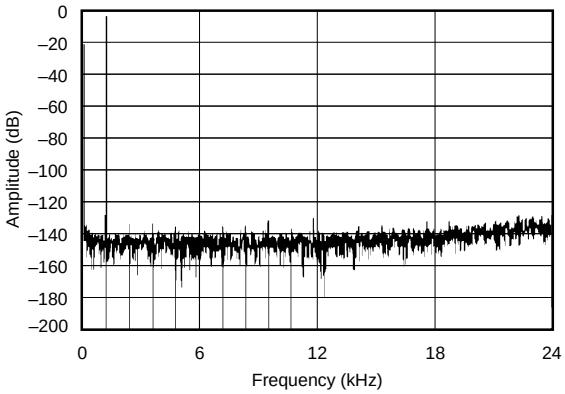
PASS-BAND CHARACTERISTICS
OF THE FIR PORTION OF THE DF1760



TOTAL PASS-BAND FREQUENCY RESPONSE,
COMBINATION OF PCM1760 AND DF1760

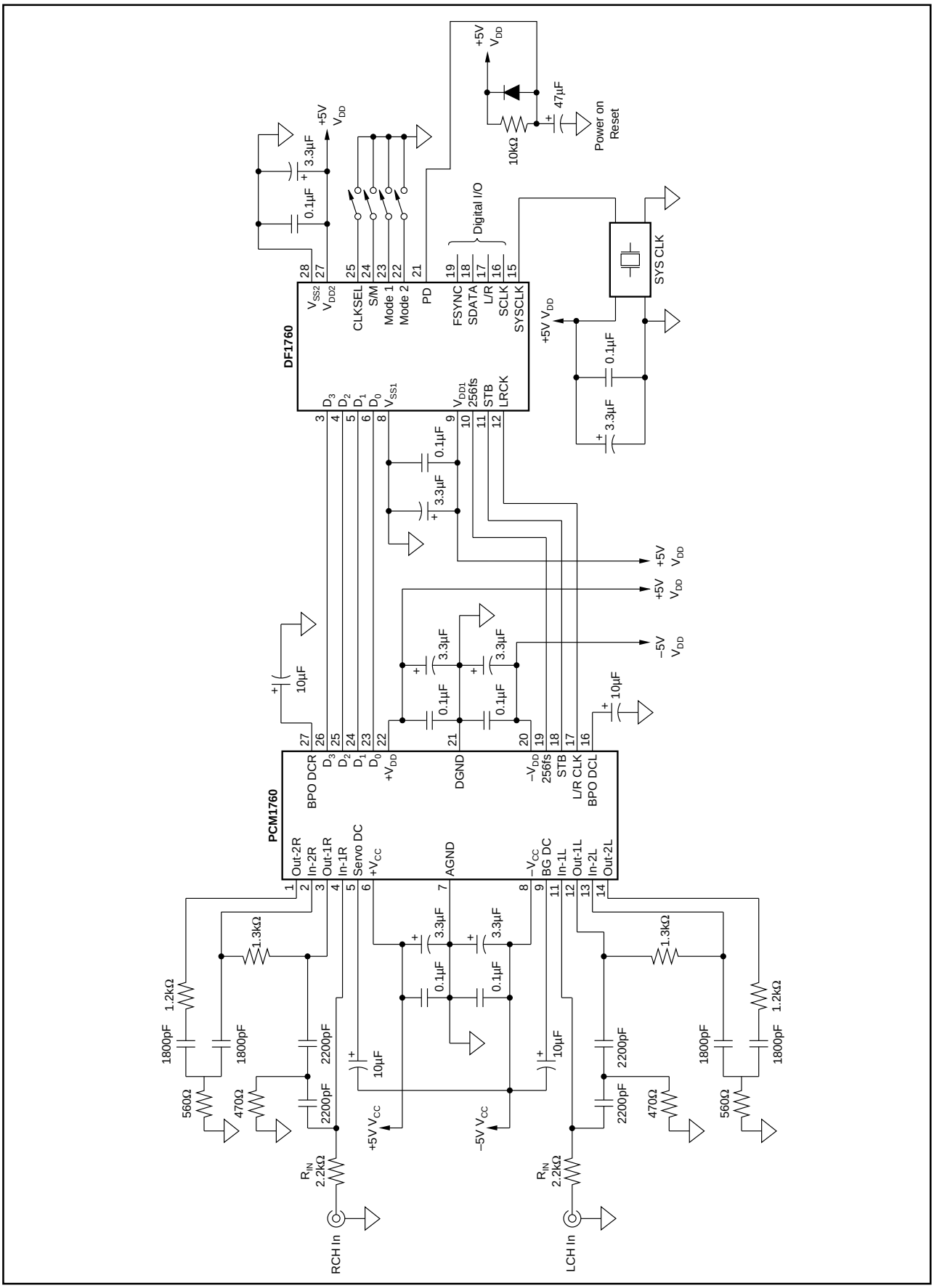


TYPICAL FFT ANALYSIS OF THE 1kHz fs INPUT SIGNAL



fs = 48.000000kHz F_{C1} = 1.171876kHz

BASIC CONNECTION DIAGRAM OF PCM1760 AND DF1760



FUNCTIONS OF THE DIGITAL FILTER

SYSTEM CLOCK

The DF1760 can accept a system clock of either 256fs or 384fs. If a 384fs system clock is used, the DF1760 divides by 2/3 to create the 256fs system clock required for the PCM1760. The system clock is applied to pin 15 (SYSCLK input). The actual clock selection is done by setting pin 25 (CLKSEL input) "high" for 256fs clock and "LOW" for 384fs clock.

The detailed timing requirements for the system clock are shown in Figure 3c.

CLKSEL	SYSCLK
H	256fs
L	384fs

MASTER/SLAVE MODE

The DF1760 can be used in both the master mode and slave mode. In the master mode, the DF1760 outputs L/R (left/right channel phase clock), SCLK (data clock) and FSYNC (frame clock 2fs) signals. In the slave mode, the DF1760 accepts L/R, SCLK and FSYNC signals. The mode selection is done by taking pin 24 (S/M INPUT) "HIGH" for slave mode and "LOW" for master mode.

S/M	MODE
H	Slave
L	Master

OUTPUT DATA FORMAT

The serial output data has four possible formats. The selection of the formats can be done by the Mode 1 and Mode 2 inputs.

MODE 1	MODE 2	FORMATS
H	H	MSB First, 16 Bits, Falling Edge
L	H	MSB First, 20 Bits, Falling Edge
H	L	MSB First, 20 Bits, Rising Edge
L	L	LSB First, 20 Bits, Falling Edge

LR CHANNEL PHASE CLOCK

The status of the LR channel phase clock can be set by the LRSC input.

LRSC	L/R CLOCK AND CHANNEL
H	H = LCH, L = RCH
L	L = LCH, H = RCH

OVERFLOW DETECTION

When a near-to-clipping input condition is detected, OVL output (Pin 1), or OVR output (Pin 2), becomes "HIGH" for a duration of 4096/fs (about 85ms) depending upon on the channel detected.

The OVL and OVR output return to "LOW" after 4096/fs duration automatically.

OFFSET CALIBRATION MODE

The offset error is calibrated by storing the digital data when the input is zero in registers and subtracting it from the future data with actual signal input.

CALD	CALIBRATION
H	Disable
L	Enable

To enable the calibration mode, set the CALD input (Pin 13) "LOW". The calibration mode is disabled by setting the CALD input (Pin 13) "HIGH". The calibration cycle is initiated by setting the /PD input (Pin 21) "LOW" for more than 2 system clock periods and then setting it "HIGH". During the calibration cycle, the CAL output (Pin 14) becomes "HIGH", all the serial data is forced to "LOW", and the L/R (Pin 17), SCLK (Pin 16) and FSYNC (Pin 19) pins become input terminals after the completion of the calibration cycle. The CAL output is "LOW".

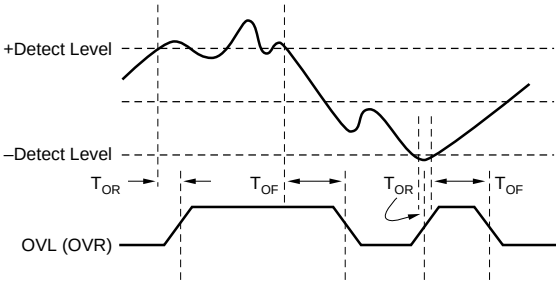
POWER DOWN MODE/RESET

The /PD input (Pin 21) has two functions. First, it should be set at "HIGH" after application or restoration of power (V_{SS} and/or V_{DD}) to accomplish the power-on/mode reset function. The detail timing requirements for this function are shown in Figure 3f. Second, the DF1760 is placed in the power down mode by setting the /PD input (Pin 21) "LOW". Set the /PD input (Pin 21) "HIGH" for normal operation mode.

/PD	OPERATION
H	Normal
L	Power Down

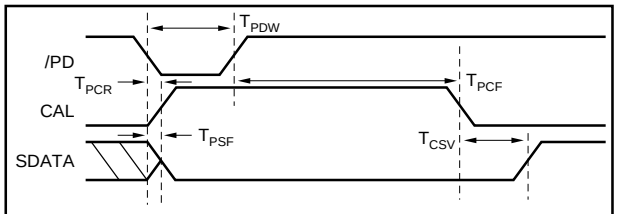
The power dissipation of the DF1760 in the power down mode is about 1/10 of the normal operation mode. During the power down mode, the L/R, SCLK, and FSYNC pins become input pins and all the serial data is forced "LOW". The 256fs output is enabled even in the power down mode.

The detailed timing of the power down mode operation and the offset calibration is shown in Figure 3b.



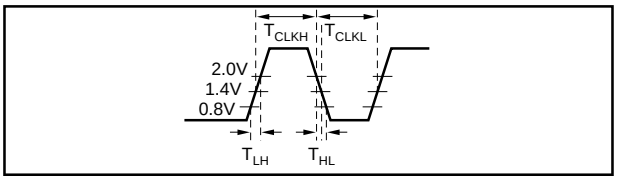
DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Delay from Overflow Detection to OVL (OVR) Output	T_{OR}	–	–	0	ns
OVL (OVR) Output Pulse Width	T_{OF}	–	4096	–	1/fs

FIGURE 3a. DF1760 Overflow Detection.



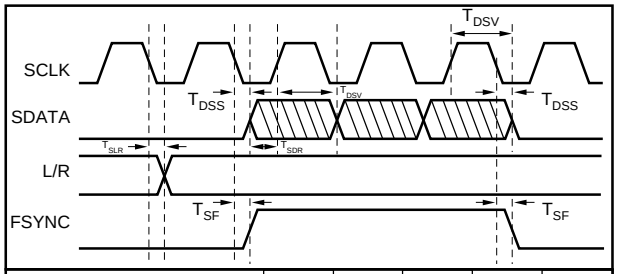
DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
Pulse Width of /PD Input	T_{PDW}	2	–	–	1/Fclk
Delay from /PD Input to CAL Output	T_{PCR}	–	–	6	1/Fclk
Calibration Cycle Duration	T_{PCF}	–	4096	–	1/fs
Delay from /PD Input to S_{DATA} L	T_{PSF}	–	–	6	1/Fclk
Delay from Completion of Calibration to SDATA Valid	T_{CSV}	–	1	–	1/fs

FIGURE 3b. DF1760 Power Down and Offset Calibration.



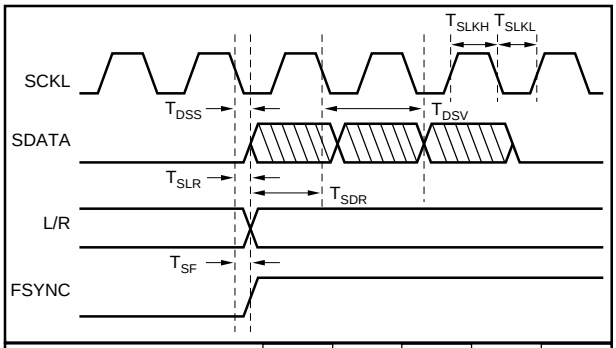
SYSTEM CLOCK: 256fs					
DESCRIPTION	**NAME**	**MIN**	**TYP**	**MAX**	**UNITS**
Low Level Duration	T_{CLKL}	31	–	–	ns
High Level Duration	T_{CLKH}	31	–	–	ns
SYSTEM CLOCK: 384fs					
DESCRIPTION	**NAME**	**MIN**	**TYP**	**MAX**	**UNITS**
Low Level Duration	T_{CLKL}	24	–	–	ns
High Level Duration	T_{CLKH}	24	–	–	ns
Rise Time	T_{LH}	–	–	6	ns
Fall Time	T_{HL}	–	–	6	ns

FIGURE 3c. System Clock Timing Requirements of DF1760.



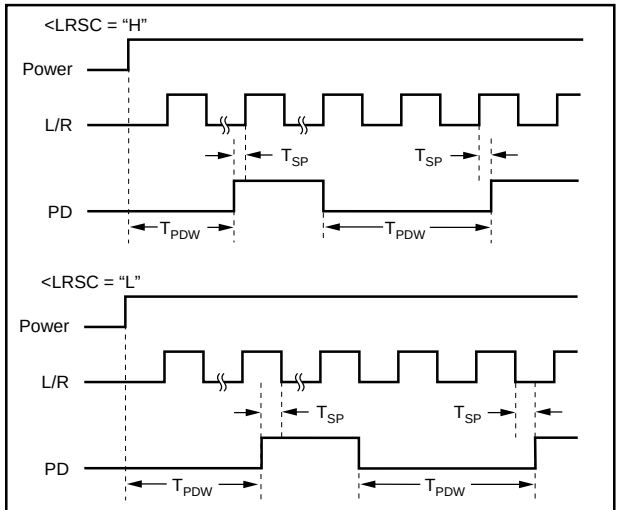
DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
SCLK Frequency	F_{SLK}	–	64fs	–	
SCLK Frequency Duty Cycle		–	50	–	%
FSYNC Frequency	F_{SYNC}	–	2fs	–	
FSYNC Frequency Duty Cycle		–	50	–	%
Delay from SCLK to L/R Edge	T_{SLR}	–20	–	50	ns
Delay from Falling Edge of SCLK to SDATA Valid	T_{DSS}	–	–	50	ns
Delay from SCLK to FSYNC Edge	T_{SF}	–20	–	50	ns
Delay from Rising Edge of SCLK to SDATA Valid	T_{SDR}	100	–	–	ns
Delay from SDATA Valid to Rising Edge of SCLK	T_{DSV}	100	–	–	ns

FIGURE 3d. Output Timing of Master Mode, DF1760.



DESCRIPTION	NAME	MIN	TYP	MAX	UNITS
SCLK Frequency	F_{SLK}	32fs	48fs	64fs	–
Low Duration of FSCLK	T_{SLKL}	100	–	–	ns
High Duration of FSCLK	T_{SLKH}	100	–	–	ns
Delay from SCLK to L/R Edge	T_{SLR}	–70	–	70	ns
Delay from Falling Edge of SCLK to SDATA Valid	T_{DSS}	–	–	50	ns
Delay from SCLK to FSYNC Edge	T_{SF}	–70	–	0	ns
Delay from Rising Edge of SCLK to SDATA Valid	T_{DSV}	100	–	–	ns
Delay from SDATA Valid to Rising Edge of SCLK	T_{SDR}	100	–	–	ns

FIGURE 3e. Timing of Slave Mode, DF1760.



DESCRIPTION	NAME	MIN	TYP	MAX	UNITS[1]	APPLIES TO MODE
Power on to PD ↑	T_{PDW}	2			1/fs	Master/Slave
PD ↑ to L/R ↑ (LRSC = "H")	T_{SP}	–1		+1	1/Fclk	Slave
PD ↑ to L/R ↓ (LRSC = "L")	T_{SP}	–1		+1	1/Fclk	Slave

NOTE: (1) fs: sampling rate. Fclk: system clock frequency.

FIGURE 3f. Power On and Mode Reset Timing.

THEORY OF OPERATION

MULTI-BIT ENHANCED NOISE SHAPING

A block diagram of a typical 1-bit delta-sigma modulator is shown in Figure 4.

In Figure 4, the quantizer consists of a single bit which has two possible states, either "0" or "1". The input signal is sampled at a much higher sample rate than the nyquist sampling frequency. The quantizer output data stream is digitally filtered for higher resolution nyquist data. The theoretical SNR is determined by the number of the order of the integrator and the oversampling rate.

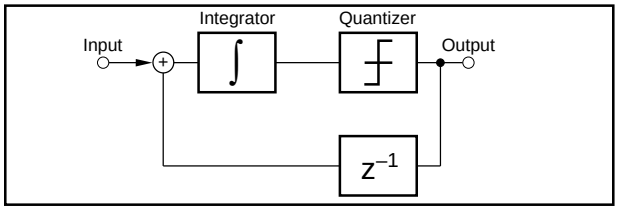


FIGURE 4. Single Stage 1-Bit Delta-Sigma.

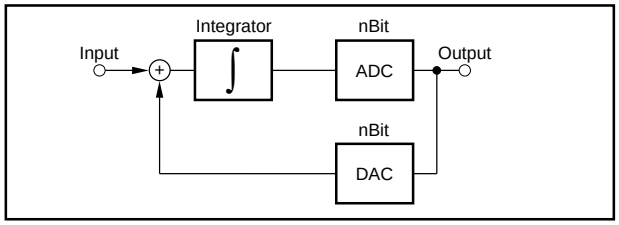


FIGURE 5. Single Stage Multi-bit Delta-Sigma.

There is a practical limit to increasing the numbers of order of the integrator due to an inherent oscillation in the modulator. There is also a limit to increasing the sample rate due to the increase in jitter sensitivity associated with high clock frequencies.

The PCM1760 utilizes a four-bit quantizer instead of the conventional one-bit method. The quantizing noise of a four-bit quantizer is 1/16 of the one-bit version. Using the four-bit quantizer allows for a lesser order number of the integrator and a lower oversampling rate to achieve similar performance to that of a more complex one-bit system.

A block diagram of the PCM1760 modulator is shown in Figure 6. The PCM1760 is a fourth-order integrator that samples at 64x oversampling, and samples left and right channel input signal simultaneously.

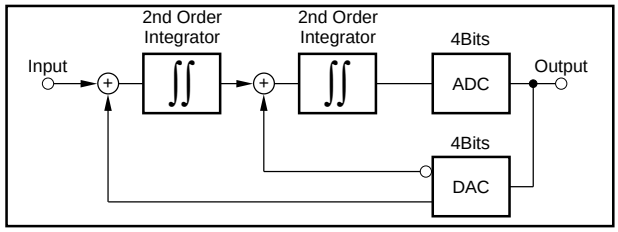


FIGURE 6. Multi-bit Enhanced Noise Shaping.

The DF1760 accepts the four-bit 64fs noise shaped data stream from the PCM1760 and decimates to 1/16 with an initial filter, and then decimates to 1fs 20-bit data using a 4x oversampling filter.

The PCM1760 and DF1760 combination achieves a dynamic range of 108dB and SNR of 110dB even with a single-ended input.

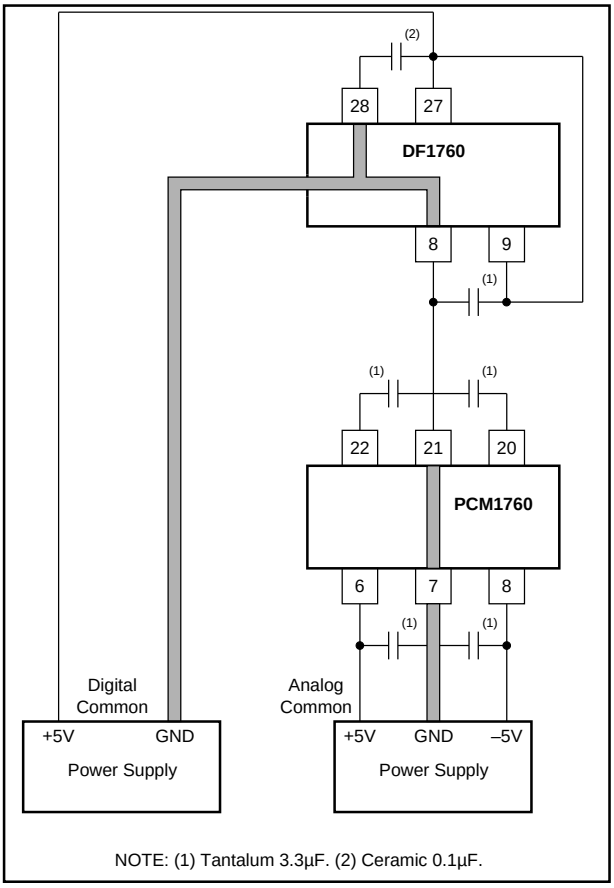


FIGURE 7. Recommended Power Supply Connection and Decoupling.

LAYOUT PRECAUTIONS

Analog common and digital common of the PCM1760 are not connected internally. These should be connected together with the common of the DF1760 as close to the unit as possible, preferably to a large ground plane under the PCM1760.

The use of a separate +5V supply is recommended for the PCM1760 and DF1760, and to connect the common at one point as described above. Low impedance analog and digital commons returns are essential for better performance.

The power supplies should be bypassed with tantalum capacitors as close as possible to the units. See Figure 7 for recommended common connections and power supplies bypassing.

OUTPUT TONE ELIMINATION

When the sampling frequency (fs) is between 40kHz and 50 kHz and the L/R relative offset voltage (ΔVs) is less than or equal to 0.05% of full scale range, the PCM1760 may output a tone similar to an idle tone. This tone is very low and its frequency depends on the input L/R relative offset voltage, ΔVs. This tone never occurs when the sampling frequency (fs) is 32kHz.

To avoid this tone, the offset voltage should be summed using an amplifier, buffer, active low pass filter, etc., to cause the input L/R relative offset voltage (ΔVs) to be greater than 0.05% of full scale range.

It is recommended that:

(A) Sum offset at both L/R channels
Lch: V_{IL} = –20mV ±10%
Rch: V_{IR} = +10mV ±10%

(B) Sum offset at L channel
Lch: V_{IL} = –30mV ±10%
Rch: V_{IR} = ±1mV (by a precircuit)

When FSR = 5V (±2.5V).

Figure 8 shows an application circuit for summing the offset at both L/R channels.

Alternately, Figure 9 shows an application circuit for use when fs = 48kHz which changes the external integrator circuit of the PCM1760.

MODULATOR COMPONENTS AND SAMPLING FREQUENCY

The PCM1760/DF1760 are capable to 30kHz to 50kHz fs sampling frequency by condition with external components value which are shown in Basic Connection Diagram.

The characteristics of the modulator's integrator can be set by external components. The values in the block diagram on page five are recommended for optimized performance. Low leakage, low voltage coefficient capacitors are recommended for integration capacitors.

The tolerance of external components should be better than ±2%.

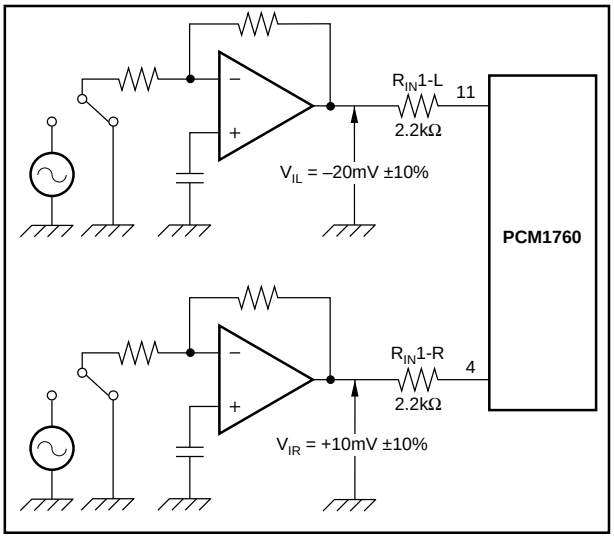


FIGURE 8. Application Example to Eliminate the Tone (offset voltage implementation for both channels).

OFFSET ERROR CALIBRATION

The offset voltage of the PCM1760 and the input stage of the system can be compensated by using the calibration mode of the DF1760. Offset calibration is shown in Figure 10. An optional analog switch is driven by a CAL output of the DF1760. The PD input of the DF1760 is used to initiate the calibration cycle.

ANALOG INPUT AND DIGITAL OUTPUT

Ideal output digital code range for 20-bit resolution is from 8000H (–Full Scale) to 7FFFFH (+Full Scale).

The DF1760, combined with 70000H (±FSR) of the PCM1760, produces a digital output code range at ±FSR input of 90000H (–FSR).

The relationship between analog input and digital output is shown in Table I.

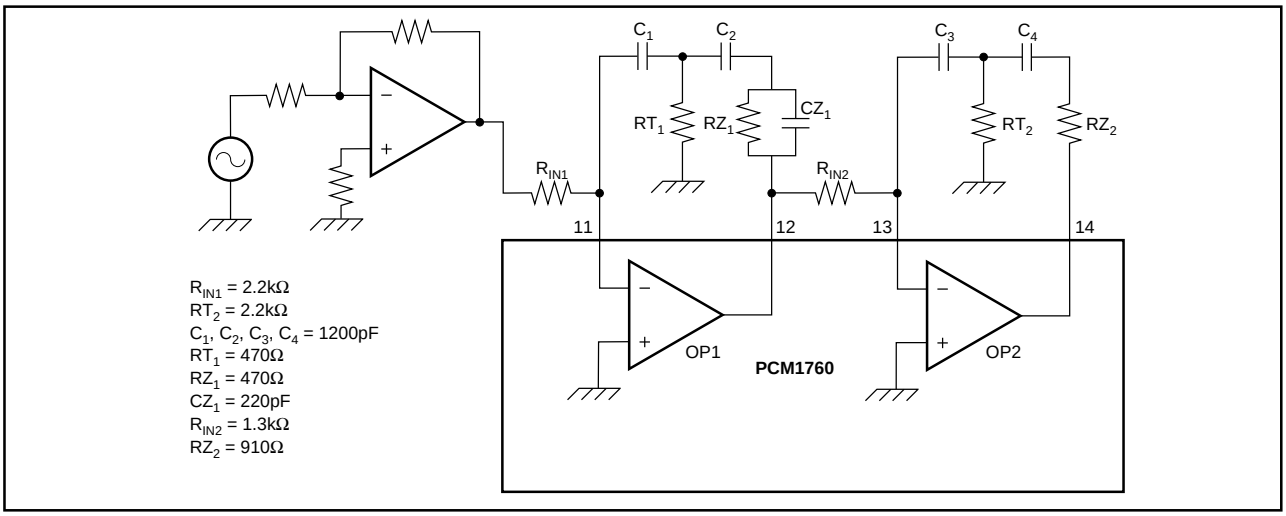


FIGURE 9. Application Example to Eliminate the Tone (alternative modulator's integrator circuit. Only for fs = 48kHz).

ANALOG INPUT	CONDITION	DIGITAL OUTPUT
+2.55V	+Max Input	72000H
+2.50V to +2.55V	Overflow	70000H to 72000H[2]
+2.50V	+FSR	70000H
0V	BPZ (Ideal)	00000H[1]
–2.50V	–FSR	90000H
–2.83V to –2.85V	Overflow	82FFFH to 82000H[2]
–2.85V	–Max Input	82000H

NOTES: (1) Incase of BPZ Error = 0. (2) Overflow detection level is over 70000H or under 82FFFH of digital output code.

TABLE I. Output Codes.

POWER SUPPLY SEQUENCING

The PCM1760 requires $\pm V_{CC}$ and $\pm V_{DD}$ power supplies. To avoid any possibility of latch-up, the $\pm V_{CC}$ and $\pm V_{DD}$ power should all be applied simultaneously or the $+V_{CC}$ and $+V_{DD}$ applied first followed by $-V_{CC}$ and $-V_{DD}$.

POWER-ON RESET AND MODE RESET

The timing requirements for POWER-ON RESET and MODE RESET are shown in Figure 3f. The DF1760 requires POWER-ON RESET when power is applied or restored. MODE RESET is required when any of the following has been changed: system clock, master/slave mode, output data format, L/R clock, calibration after POWER-ON in slave mode.

This reset should be done by holding the /PD input (pin 21) low for more than 2/fs. Suggested reset circuits are given in Figures 11, 12 and 13.

CLOCK INPUT

After power is applied to the DF1760, the system clock should be provided continuously. The DF1760 employs a dynamic logic architecture.

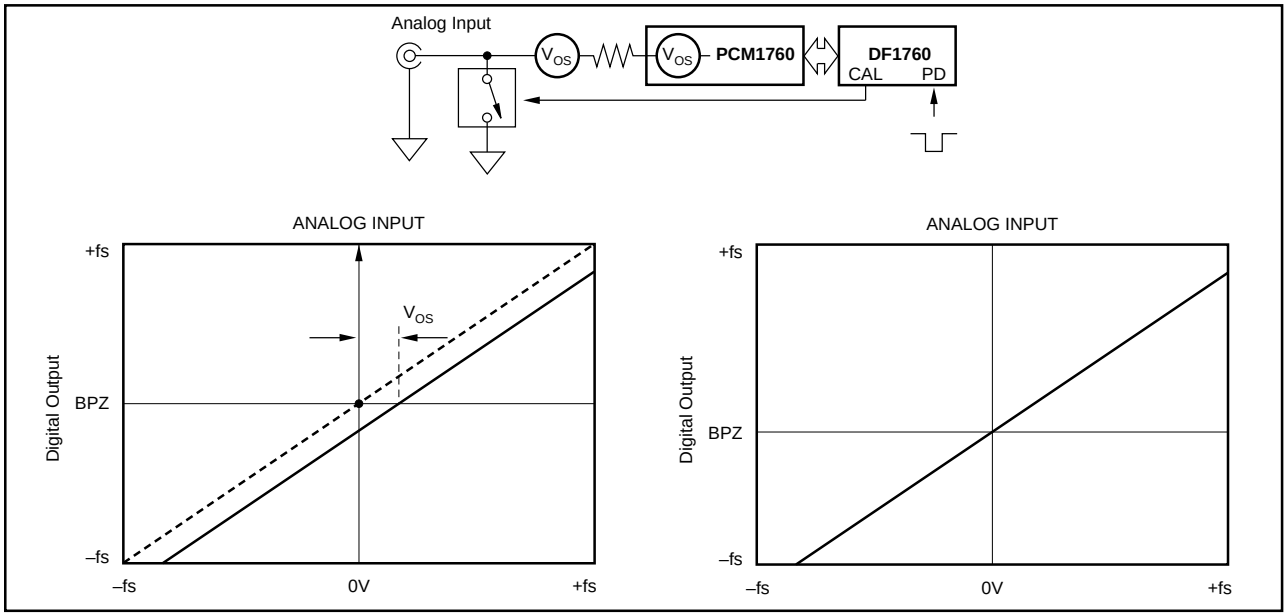


FIGURE 10. Illustration of Offset Calibration.

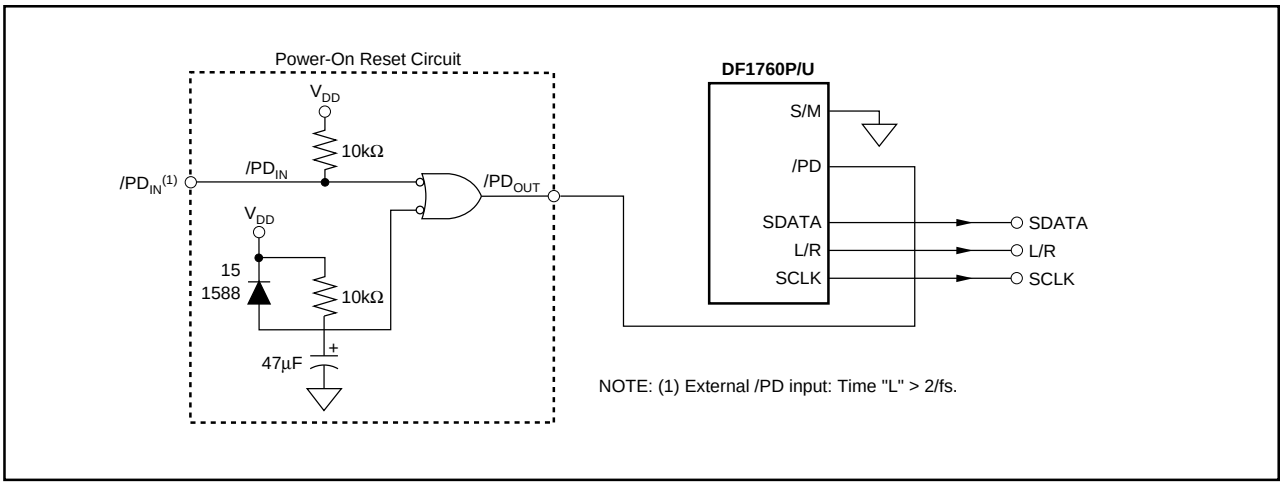


FIGURE 11. Master Mode Reset Circuit.

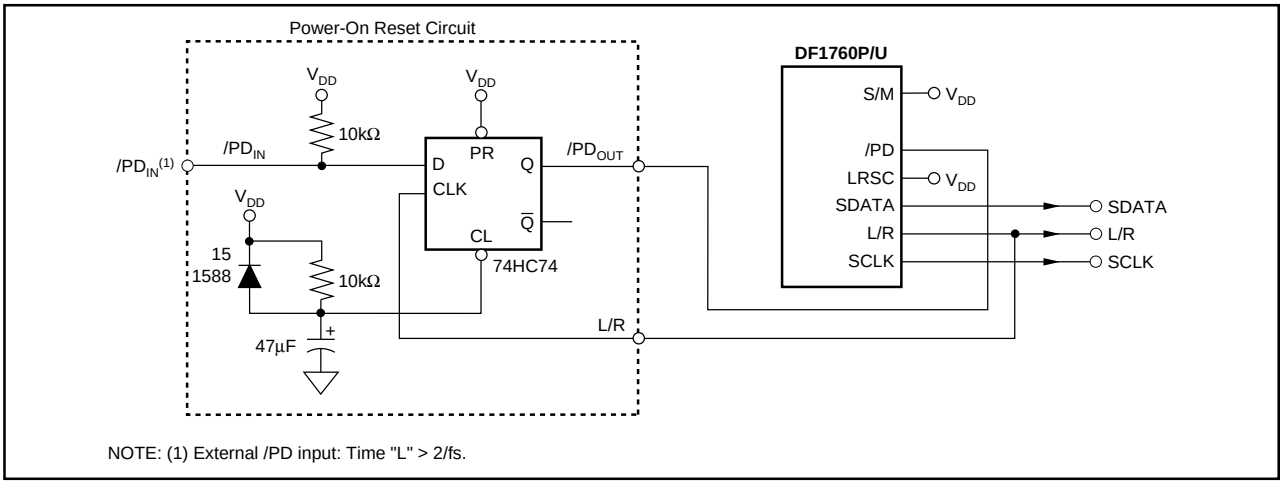


FIGURE 12. Slave Mode Reset Circuit, (LRSC = H).

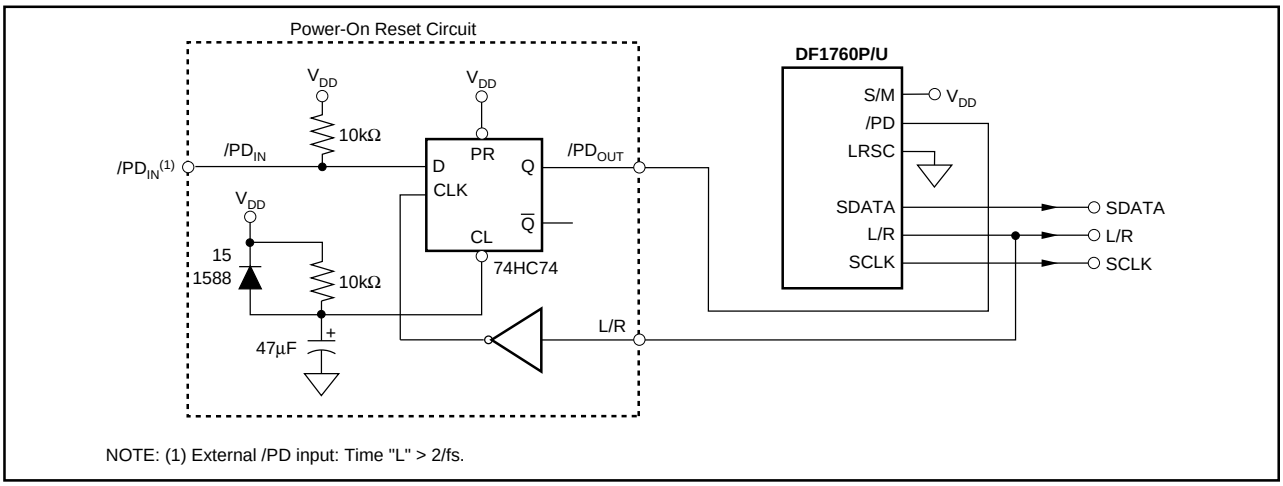


FIGURE 13. Slave Mode Reset Circuit, (LRSC = L).

TIMING CHARACTERISTICS

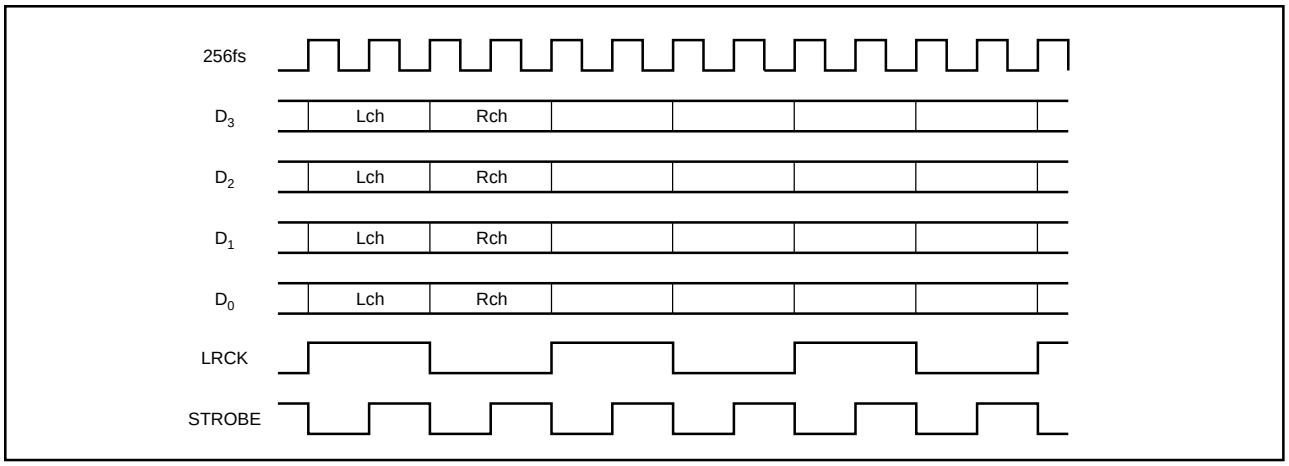


FIGURE 14. Input and Output Format of the DF1760 and PCM1760.

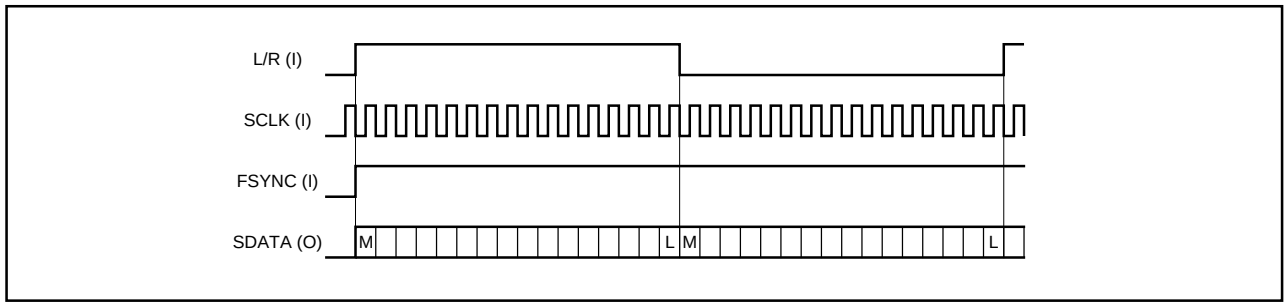


FIGURE 15a. Slave Mode and SCLK = 32fs. (Output format of the DF1760).

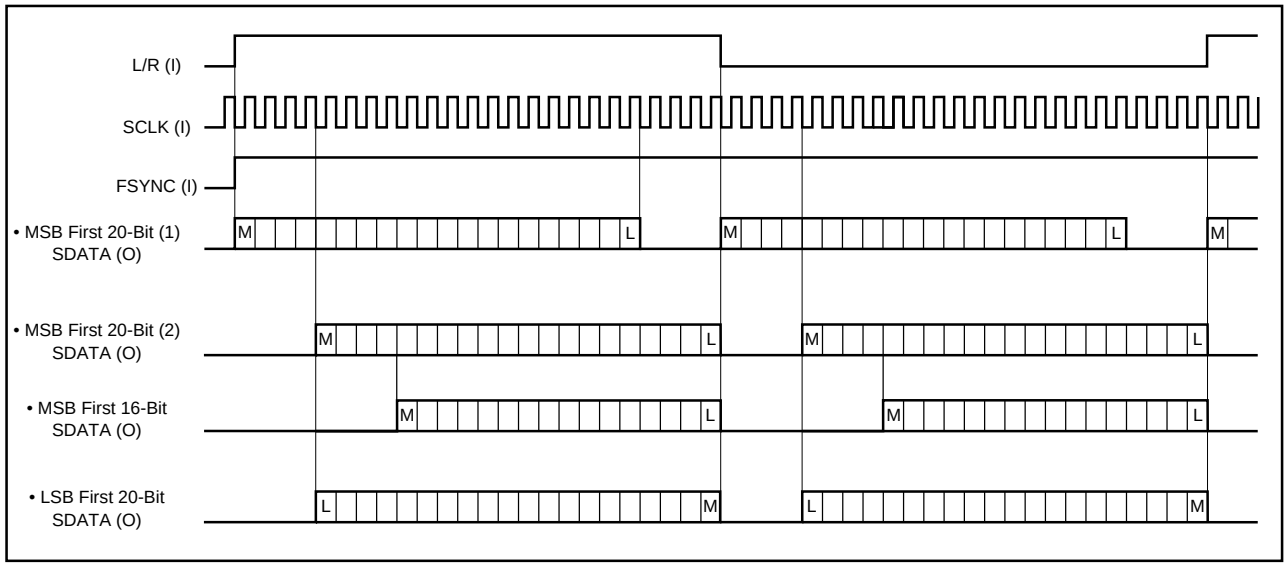


FIGURE 15b. Slave Mode and SCLK = 48fs.

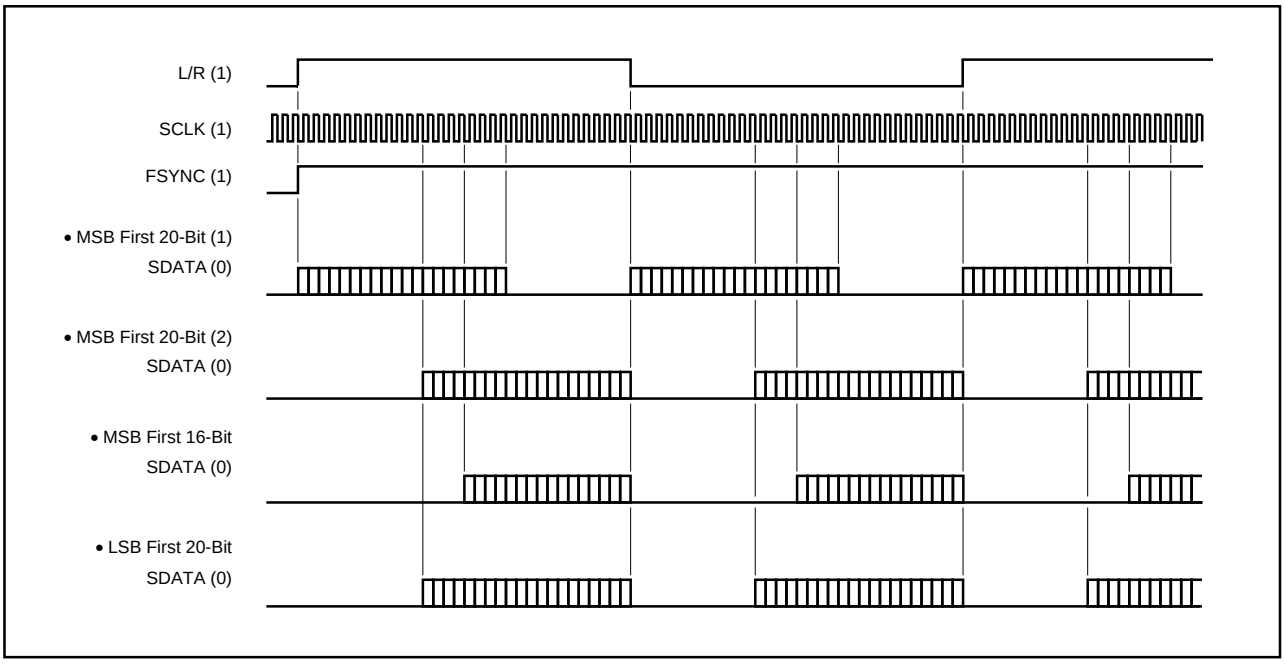


FIGURE 15c. Slave Mode and SCLK = 64fs.

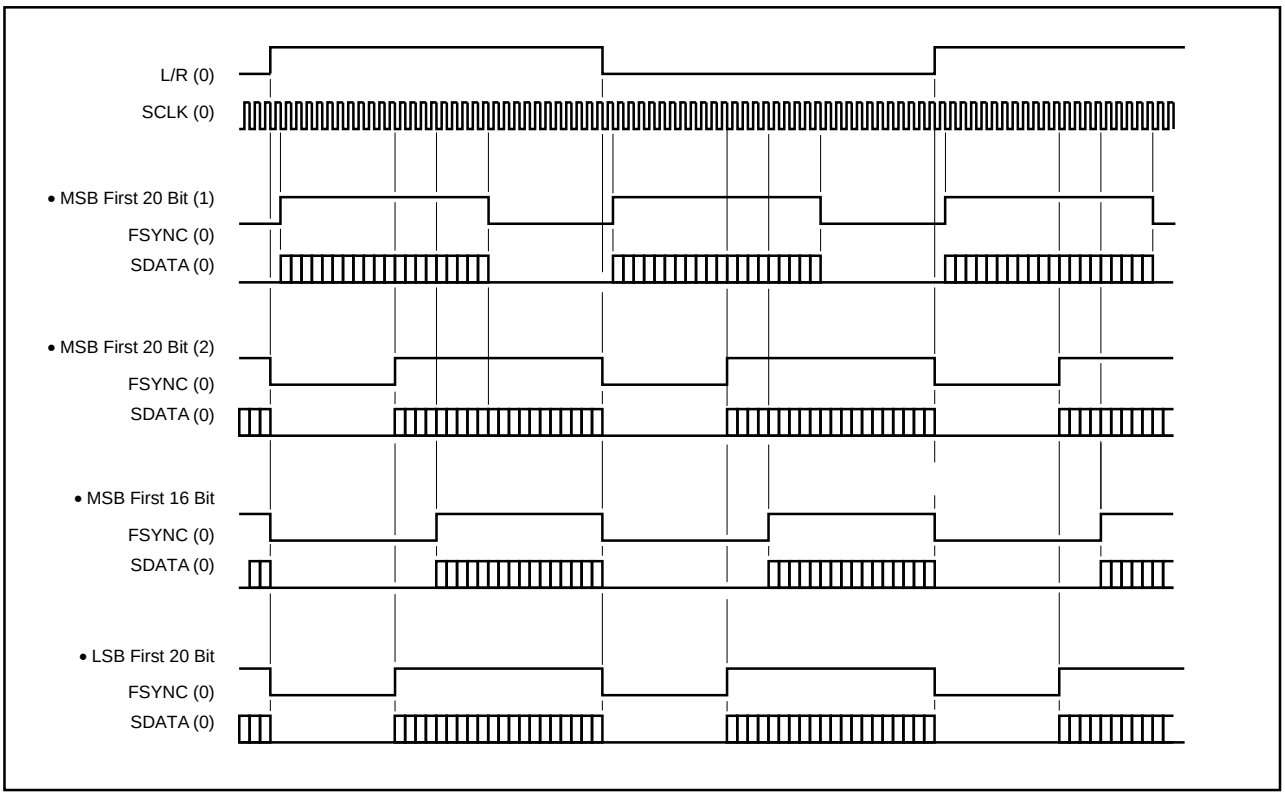


FIGURE 15d. Master Mode.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DF1760U	NRND	SO	NS	20		TBD	Call TI	Call TI			
PCM1760P	NRND	PDIP	NTD	28		TBD	Call TI	Call TI			
PCM1760P-L	NRND	PDIP	NTD	28		TBD	Call TI	Call TI			
PCM1760U	NRND	SOIC	DW	28		TBD	Call TI	Call TI			
PCM1760U-L	NRND	SOIC	DW	28		TBD	Call TI	Call TI			
PCM1760U-L/1K	NRND	SOIC	DW	28		TBD	Call TI	Call TI			
PCM1760U/1K	NRND	SOIC	DW	28		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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