30 V Input 3 A Buck DC/DC Converter

NO.EA-191-170607

OUTLINE

The R1242S is a CMOS-based 30 V input, 3 A, synchronous rectified step-down DC/DC converter with built-in High-side switch. The R1242S contains Nch High-side Tr. (Typ. 0.1 Ω) and can supply maximum 3 A output current. In order to reduce heat generation caused by energy loss, FET can be used as Low-side switch. Low-side switch turns off when ICs shut down. The R1242S consists of the followings: an oscillator, a PWM control circuit, a voltage reference unit, an error amplifier, a phase compensation circuit, a slope control circuit, a soft-start circuit, protection circuits, an internal regulator, a switch, and so on. Also, the R1242S consists of the following external components: an inductor, resistors, an external FET, and capacitors.

The R1242S operates with current mode topology, which does not require any sense resistor. As a result, the R1242S can achieve high speed and high efficiency. The oscillator frequencies for each version are set as follows; adjustable between 330 kHz to 1000 kHz for versions A and B, 330 kHz for versions C and D, 500 kHz for versions E and F, and 1000 kHz for versions G and H.

The R1242S is equipped with the protection functions, such as peak current limit function, latch function, fold back function, thermal-shutdown function, and undervoltage-lockout (UVLO) function. Peak current limit function restricts the maximum current into 4.5 A. Latch function (comes with versions A, C, E, and G) shuts off the output if current limit detection continues for a certain period of time. Fold back function (comes with versions B, D, F, and H) reduces the initial oscillator frequencies into 1/4 when output is short-circuited.

FEATURES

- Supply Current...Typ. 0.8 mA (V_{IN} = 30 V, Set V_{FB} = 1.0 V)
- Standby Current ....Typ. 0 μA (V_{IN} = 30 V, CE = L)
- Input Voltage Range ....5 V to 30 V
- Output Voltage Range ....0.8 V to 15 V, Adjustable using external resistors
- Feed Back Voltage Accuracy..0.8 V with 1.5% accuracy
- Output Current..3 A*
- Oscillator Frequency...330 kHz to 1 MHz (Ver. A/B), 330 kHz (Ver. C/D), 500 kHz, (Ver. E/F), 1000 kHz (Ver. G/H)
- Maximum Duty Cycle..Typ. 88%
- UVLO Detector Threshold ....Typ. 3.6 V
- Soft-start Time ....Typ. 0.5 ms
- Peak Current Limit...Typ. 4.5 A
- Thermal Shutdown ....Typ. 160°C
- Latch Type Protection...Delay Time: Typ. 5 ms (Ver. A/C/E/G)
- Fold-back Type Protection..Fold-back Frequency: Ver. B: fosc x 1/4, Ver. D: 83 kHz, Ver. F: 125 kHz, Ver. H: 250 kHz
- Package..HSOP-8E

* This is an approximate value. The output current depends on conditions and external parts.

APPLICATIONS

- Digital Home Appliances: Digital TVs, DVD Players
- Office Automation Equipment: Printers, Fax
- Hand-held Communication Equipment: Cameras, Video Recorders
- Battery-powered Equipment

SELECTION GUIDE

The oscillator frequency (Adjustable, Fixed: 330 kHz, 500 kHz, 1000 kHz) and the short-circuit protection type (Latch, Fold-back) are user-selectable options.

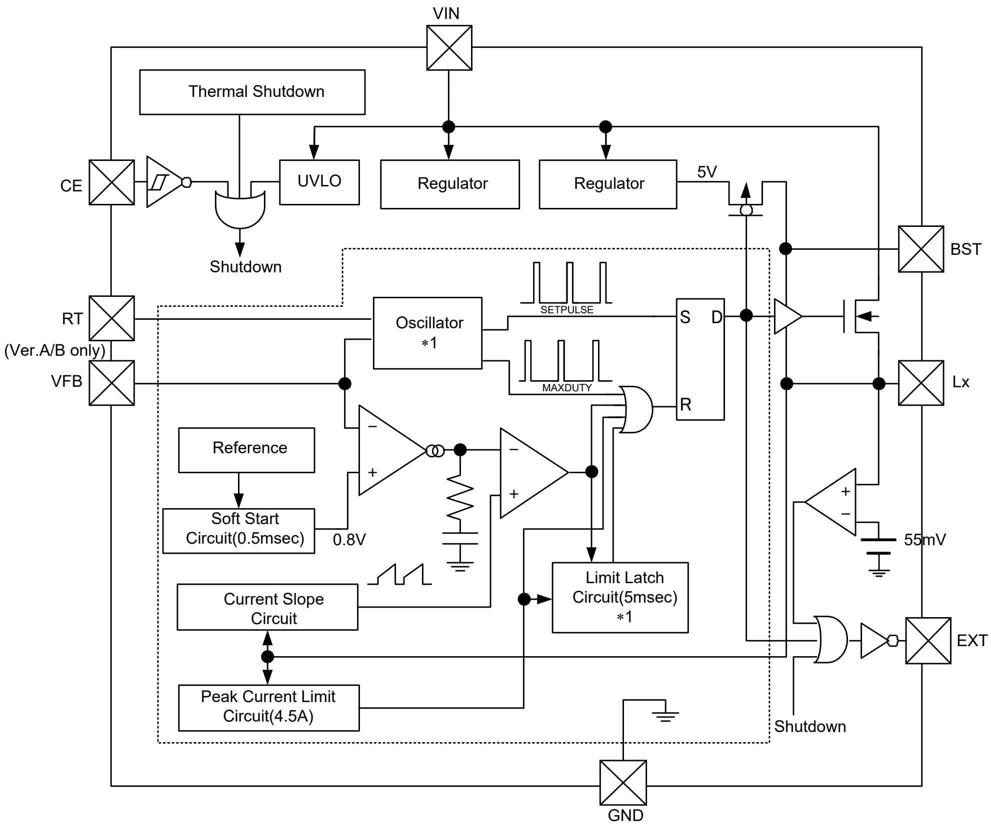
Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1242S001∗-E2-FE	HSOP-8E	1,000 pcs	Yes	Yes

∗ : Specify the oscillator frequency and the short-circuit protection type.

Code	Frequency	Latch Type	Fold-back Type
A	Adjustable	Yes	No
B	Adjustable	No	Yes
C	330 kHz	Yes	No
D	330 kHz	No	Yes
E	500 kHz	Yes	No
F	500 kHz	No	Yes
G	1000 kHz	Yes	No
H	1000 kHz	No	Yes

BLOCK DIAGRAM



R1242S Block Diagram

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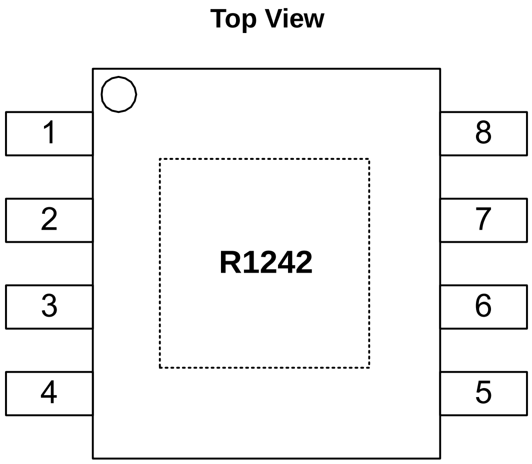
Version	Oscillator Frequency	Short Protection
A	Adjustable	Latch Type
B	Adjustable	Fold-back Type
C	330 kHz	Latch Type
D	330 kHz	Fold-back Type
E	500 kHz	Latch Type
F	500 kHz	Fold-back Type
G	1000 kHz	Latch Type
H	1000 kHz	Fold-back Type

PIN DESCRIPTIONS



HSOP-8E Pin Configuration

R1242S001A/B Pin Description

Pin No.	Symbol	Description
1	CE	Chip Enable Pin, Active with “H”
2	EXT	Gete Drive Pin
3	BST	Bootstrap Pin
4	VIN	Power Supply Pin
5	Lx	Lx Switching Pin
6	GND	Ground Pin
7	VFB	Feedback Pin
8	RT	Frequency Setting Pin

∗ Tab is GND level. (They are connected to the reverse side of this IC.) The tab must be connected to the GND.

R1242S001C/D/E/F/G/H Pin Description

Pin No.	Symbol	Description
1	CE	Chip Enable Pin, Active with “H”
2	EXT	Gate Drive Pin
3	BST	Bootstrap Pin
4	VIN	Power Supply Pin
5	Lx	Lx Switching Pin
6	GND	Ground Pin
7	VFB	Feedback Pin
8	TEST	TEST Pin, OPEN or connect to GND

∗ Tab is GND level. (They are connected to the reverse side of this IC.) The tab must be connected to the GND.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (GND = 0 V)

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	−0.3 V to 32 V	V
V_{BST}	Boost Pin Voltage	V_{LX} −0.3 V to V_{LX} +6 V	V
V_{LX}	Lx Pin Voltage	−0.3 V to V_{IN} +0.3	V
V_{CE}	CE Pin Input Voltage	−0.3 V to V_{IN} +0.3	V
V_{FB}	VFB Pin Voltage	−0.3 V to 6 V	V
V_{EXT}	EXT Pin Voltage	−0.3 V to 6 V	V
V_{RT}/ V_{TEST}	RT/ TEST Pin Voltage	−0.3 V to 6 V	V
P_D	Power Dissipation (Standard Land Pattern)*	2.9	W
Tj	Junction Temperature Range	−40 to 125	ºC
Tstg	Storage Temperature Range	−55 to 125	ºC

* Refer to *Power Dissipation* for detailed information.

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Operating Input Voltage	5 to 30	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

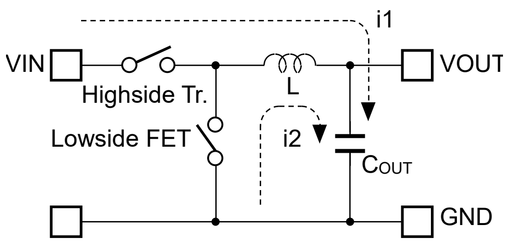
Electrical Characteristics (Unless otherwise noted, V_{IN} = 12 V, Ta = 25ºC)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I_{IN}	VIN Consumption Current	V_{IN} = 30 V, V_{FB} = 1.0 V	0.45	0.80	1.20	mA
V_{UVLO2}	UVLO Detect Voltage	Rising	V_{UVLO2} −0.5		V_{UVLO2} −0.3	V
V_{UVLO1}	UVLO Released Voltage	Falling	3.7	4.0	4.3	V
V_{FB}	VFB Voltage Tolerance		0.788	0.800	0.812	V
$\Delta V_{FB}/\Delta Ta$	VFB Voltage Temperature Coefficient	−40ºC ≤ Ta ≤ 85ºC		±100		ppm/ ºC
fosc	Oscillator Frequency (Ver. A/B)	RT = GND	900	1000	1100	kHz
		RT = floating	290	330	375	kHz
		RT = 120 kΩ	450	500	550	kHz
	Oscillator Frequency (Ver. C/D)		300	330	370	kHz
	Oscillator Frequency (Ver. E/F)		450	500	550	kHz
	Oscillator Frequency (Ver. G/H)		900	1000	1100	kHz
f_{FLB}	Fold back Frequency	V_{FB} < 0.56, RT = GND (Ver. B)		250		kHz
		V_{FB} < 0.56 (Ver. D)		83		kHz
		V_{FB} < 0.56 (Ver. F)		125		kHz
		V_{FB} < 0.56 (Ver. H)		250		kHz
Maxduty	Maximum Duty Cycle	RT = 120 kΩ (Ver. A/B) V_{IN} = 9 V (Ver. C/D)	82	88	95	%
tstart	Soft Start Time			0.5		ms
t_{DLY}	Delay Time for Latch Protection	(Ver. A/C/E/G)		5		ms
R_{LXH}	Lx High Side Switch ON Resistance			0.1		Ω
I_{LXHOFF}	Lx High Side Switch Leakage Current			0	20	μA
I_{LIMLXH}	Lx High Side Switch Limited Current			4.5		A
V_{CEH}	CE “H” Input Voltage		1.7			V
V_{CEL}	CE “L” Input Voltage				0.4	V
I_{FB}	VFB Input Current		−1.0		1.0	μA
I_{CEH}	CE “H” Input Current		−1.0		1.0	μA
I_{CEL}	CE “L” Input Current		−1.0		1.0	μA
T_{TSD}	Thermal Shutdown Detect Temperature	Hysteresis: 30ºC		160		ºC
Istandby	Standby Current	V_{IN} = 30 V, V_{CE} = 0 V		0	20	μA
R_{RISE}	EXT “H” Switch On Resistance	I_{EXT} = −100 mA	6		11	Ω
R_{FALL}	EXT “L” Switch On Resistance	I_{EXT} = 100 mA	0.5		1.5	Ω
V_{EXTLIM}	Detecting Voltage for Low Side Switch Current Limit		36	55	76	mV

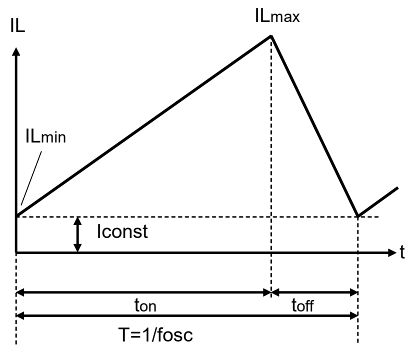
OPERATING DESCRIPTIONS

OPERATION OF STEP-DOWN DC/DC CONVERTER AND OUTPUT CURRENT

The step-down DC/DC converter charges energy in the inductor (L) when the Lx transistor turns on, and discharges the energy from the inductor when Lx transistor turns off and controls with less energy loss, so that a lower output voltage (V_{OUT}) than the input voltage (V_{IN}) can be obtained. The operation of the step-down DC/DC converter is explained in the following figures.



Basic Circuit



Inductor Current flowing through Inductor

Step1. The highside transistor turns on and the inductor current (i1) flows, L is charged with energy. At this moment, i1 increases from the minimum inductor current (ILmin), which is 0 A, and reaches the maximum inductor current (ILmax) in proportion to the on-time period (ton) of the highside transistor.

Step2. When the highside transistor turns off, L tries to maintain IL at ILmax, so L turns the lowside FET on and the inductor current (i2) flows into L.

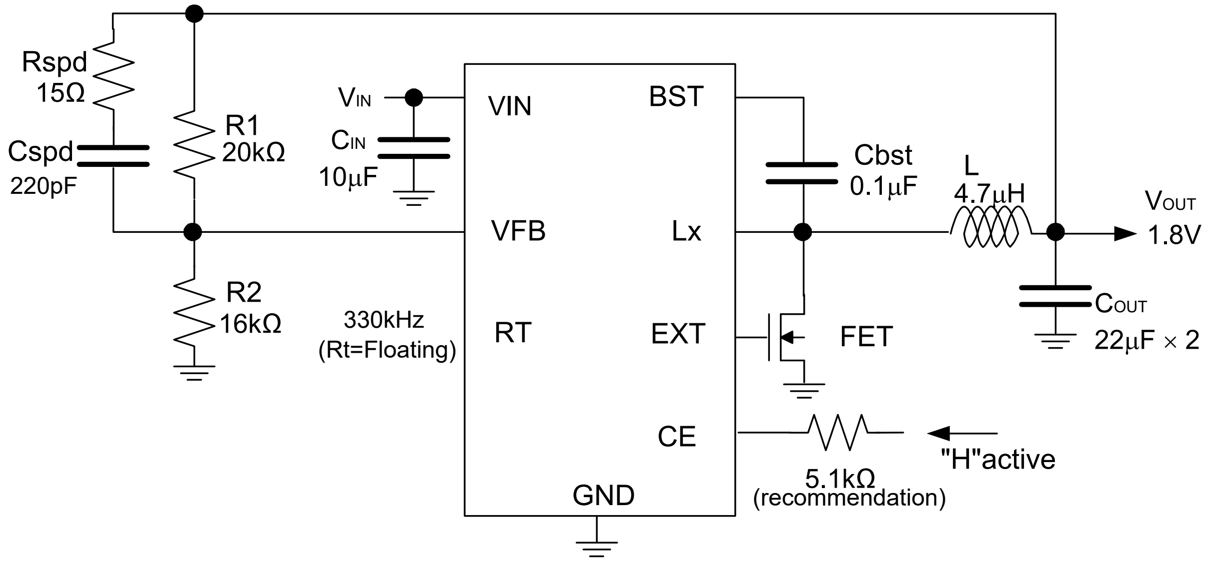
Step3. i2 decreases gradually and reaches ILmin in proportion to the off-time period (toff) of the highside transistor.

In the case of PWM mode, V_{OUT} is maintained by controlling ton. During PWM mode, the oscillator frequency (fosc) is being maintained constant.

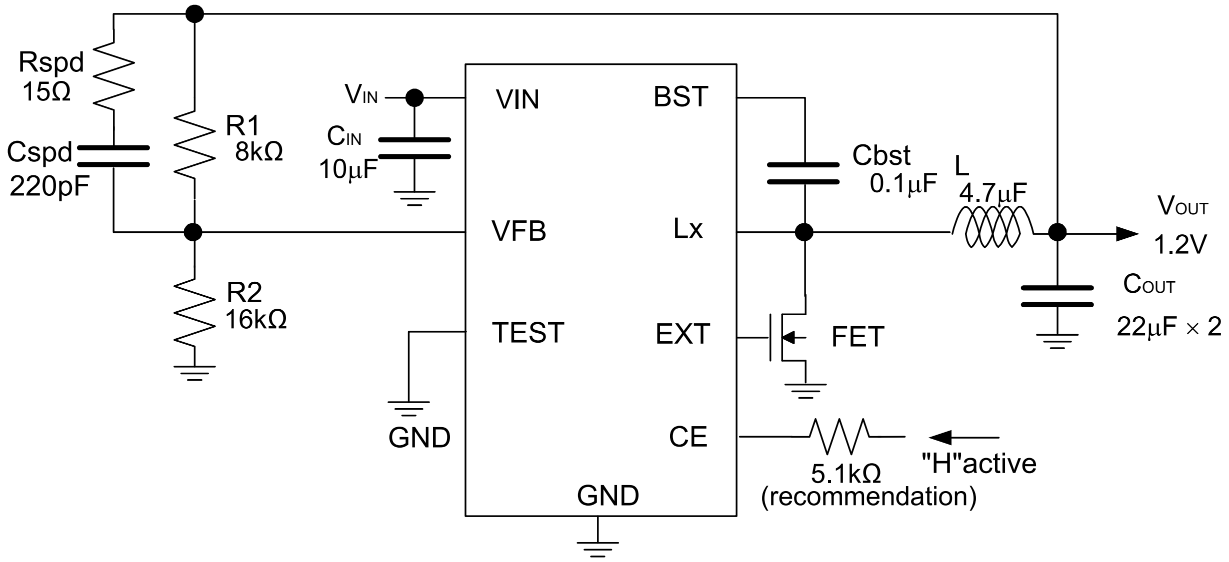
When the step-down DC/DC operation is constant, ILmin and ILmax during ton of highside transistor would be same as during toff of highside transistor.

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUIT



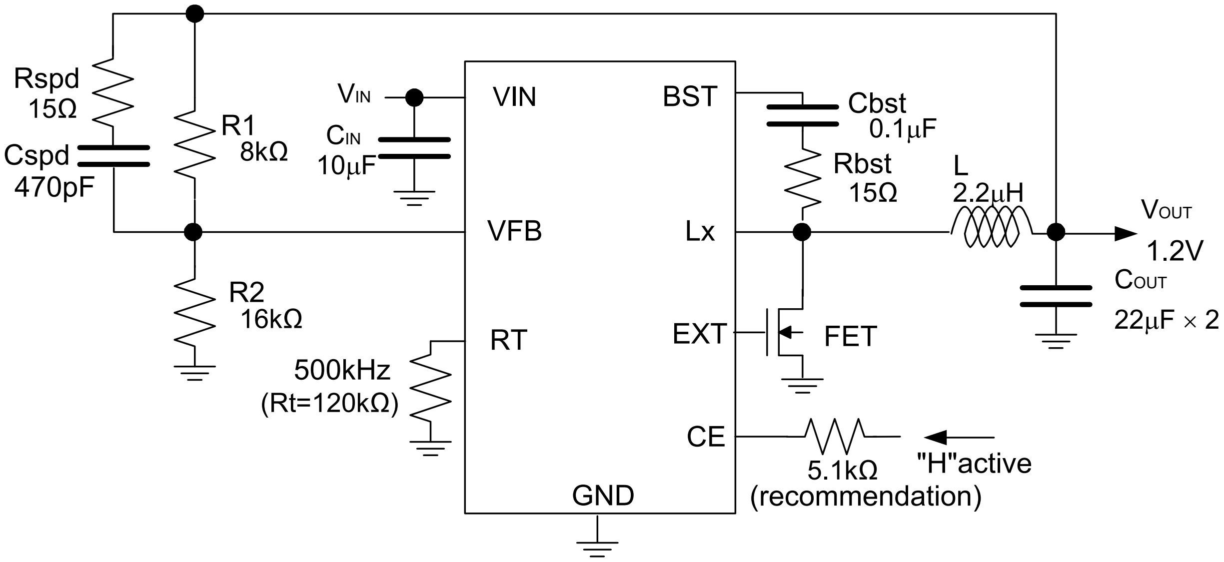
R1242S001A/B Typical Application Circuit, V_{OUT} = 1.8 V, 330 kHz



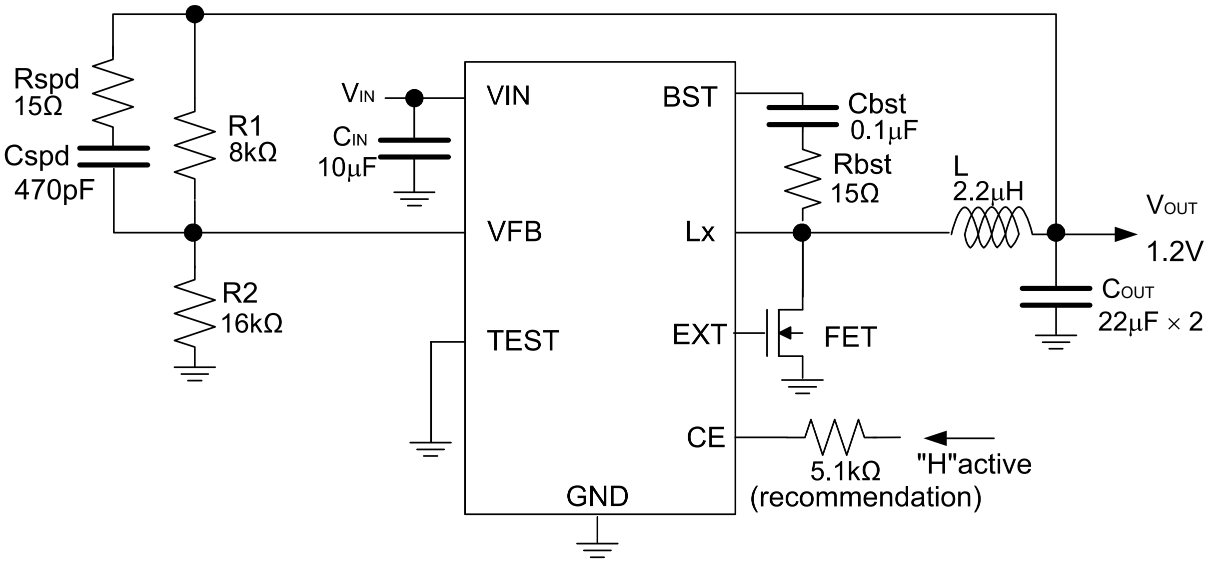
R1242S001C/D Typical Application Circuit, V_{OUT} = 1.2 V, 330 kHz

Recommendation Parts

C_{IN}	10 µF, KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{OUT}	22 µF, GRM31CR71A226M (Murata)
Cbst	0.1 µF, GRM21BB11H104KA01L (Murata)
L	4.7 µH, VLF10045T-4R7N6R1 (TDK)
FET	TPN11003NL (TOSHIBA)



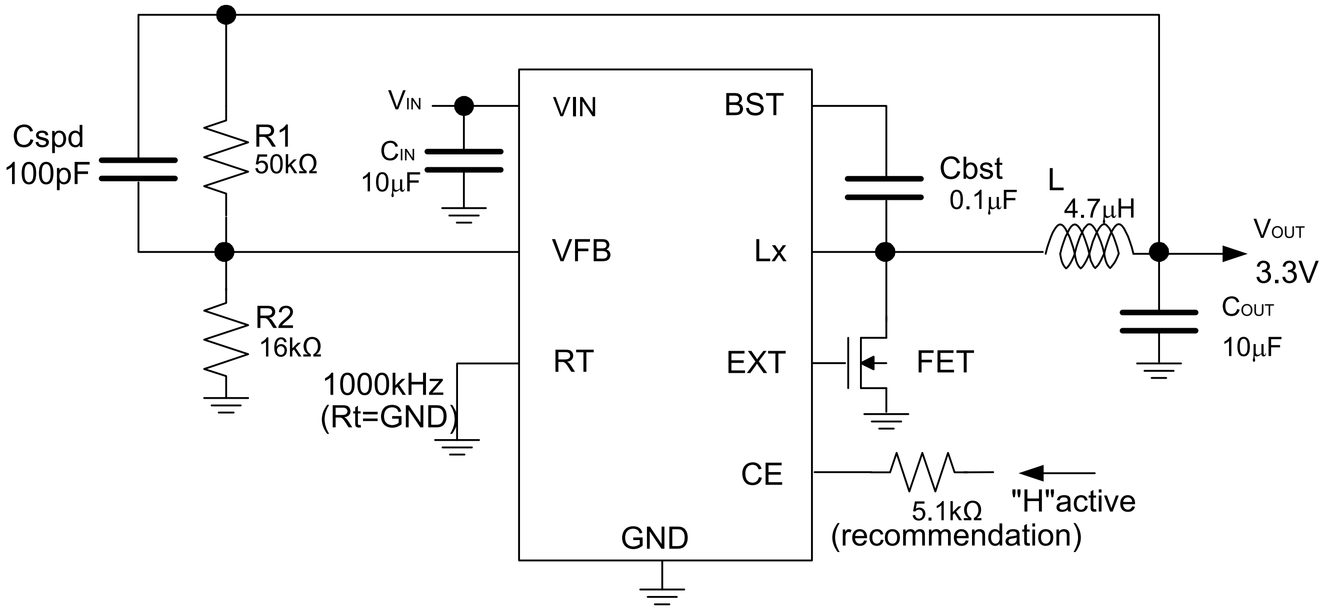
R1242S001A/B Typical Application Circuit, V_{OUT} = 1.2 V, 500 kHz



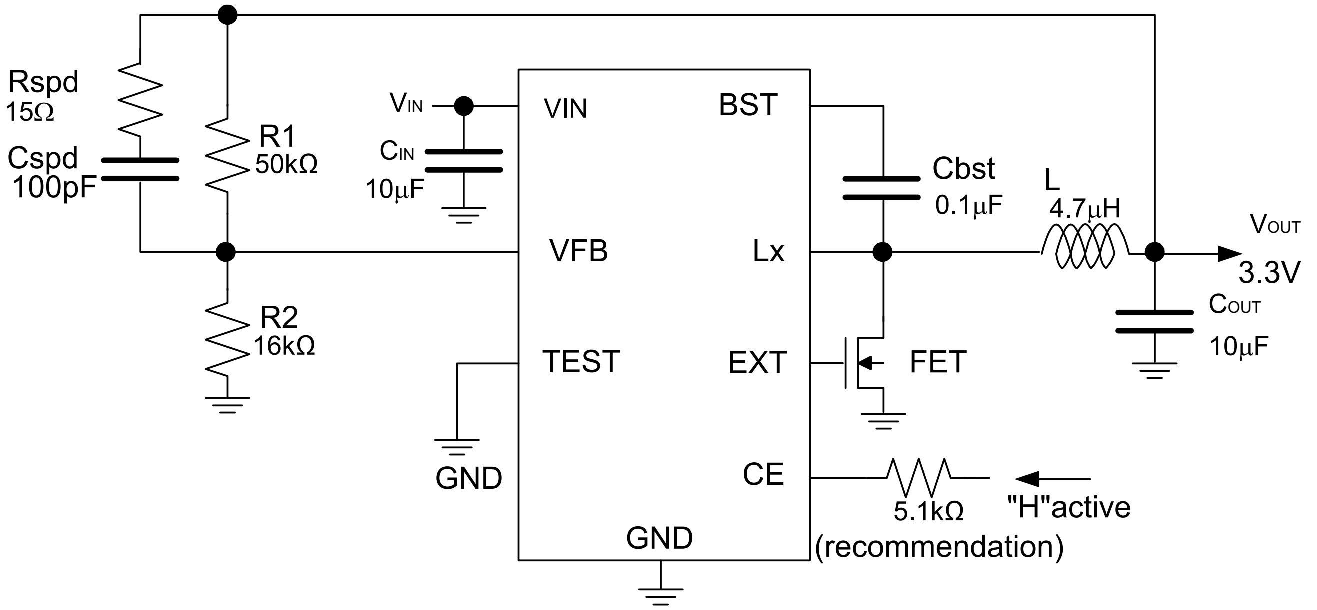
R1242S001E/F Typical Application Circuit, V_{OUT} = 1.2 V, 500 kHz

Recommendation Parts

C_{IN}	10 µF, KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{OUT}	22 µF, GRM31CR71A226M (Murata)
Cbst	0.1 µF, GRM21BB11H104KA01L (Murata)
L	2.2 µH, RLF7030T-2R2M5R4 (TDK)
FET	TPN11003NL (TOSHIBA)



R1242S001A/B Typical Application Circuit, V_{OUT} = 3.3 V, 1000 kHz



R1242S001G/H Typical Application Circuit, V_{OUT} = 3.3 V, 1000 kHz

Recommendation Parts

C_{IN}	10 µF, KTS500B106M55N0T00 (Nippon Chemi-Con)
C_{OUT}	10 µF, GRM31CR71E106K (Murata)
Cbst	0.1 µF, GRM21BB11H104KA01L (Murata)
L	4.7 µH, VLF10045T-4R7N6R1 (TDK)
FET	TPN11003NL (TOSHIBA)

RICOH

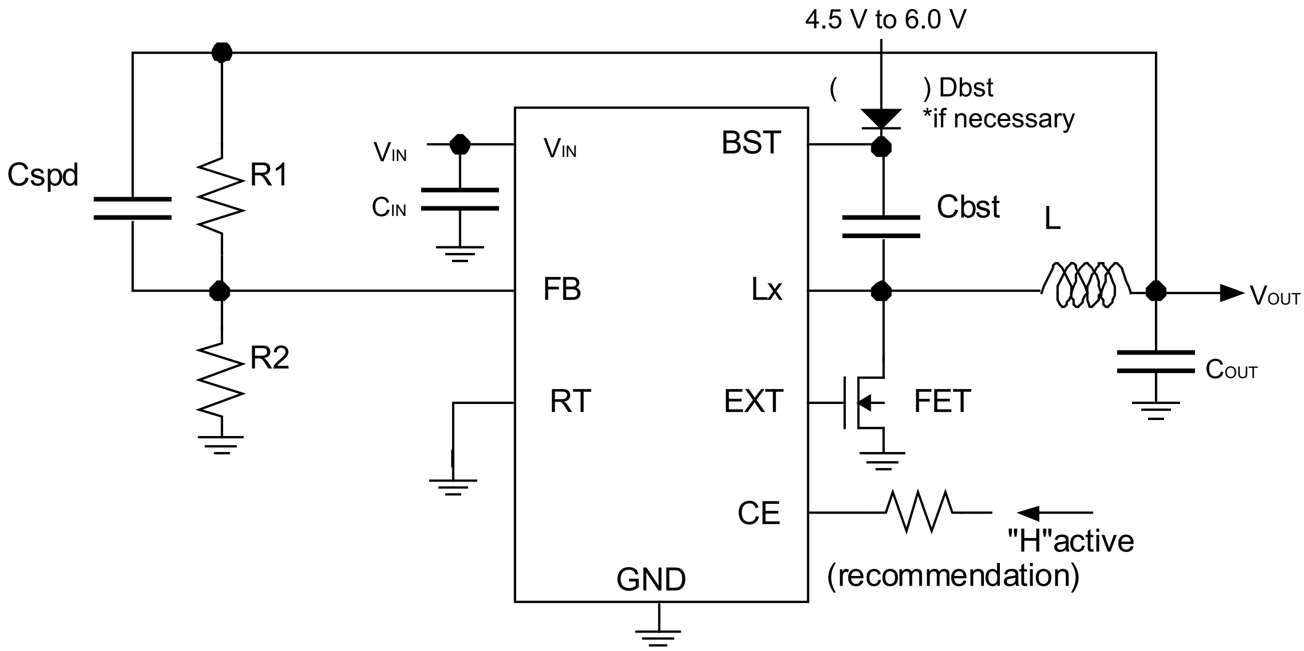
THE VOLTAGE BETWEEN THE BST PIN AND Lx PIN

In the application of the "Bootstrap" Start switching regulator, the R1242S, when the Lx pin voltage becomes equal or less than the BST voltage supply regulator, the BST voltage supply regulator charges the capacitor, Cbst. By this function, even if the Lx pin becomes "H", the high side switch composed of an Nch transistor can be turned on.

Under the condition of PWM operation, the BST voltage supply regulator of the R1242S, while the Lx pin voltage is "L", the voltage between BST pin and GND pin is controlled and maintained the level as of 5 V, then regardless of the voltage drop by the bootstrap switch, the BST voltage supply regulator can drive a high side switch and the low side external MOSFET.
However, if either the maximum duty cycle limit or the low side switch current limit is detected, sampling of the voltage between BST pin and Lx pin is halted, and the output of the BST voltage supply regulator becomes stacked at 5 V as same as a conventional "Bootstrap" Start switching regulator. Depending on the external FET gate capacitance, excessive voltage drop can be caused by bootstrap switching, and also switching failure can be caused by insufficient electrical charge on Cbst. As a result, the desired voltage may not be obtained. Higher frequency requires higher electrical charge. Special attention is required in case of using the device at 1000 kHz.

Events that may trigger such trouble are
(A) Detect of the current limit of low side switch at light load
(B) V_{OUT} > V_{IN} / 2 and starting the circuit without using CE pin individually or CE pin and VIN are tied and controlled at the same time.
(C) The voltage difference between the input and the output is small and usage at maximum duty cycle is expected.

The countermeasure to avoid the trouble caused by the events above is to use an external diode, Dbst shown in the figure below. The Dbst will charge C_{BST} and prevents the abnormal switching. The supply voltage to Dbst should be in the range from 4.5 V to 6.0 V and if the set output voltage of the R1242S is in the range from 4.5 V to 6.0 V, then the output voltage can be used directly as the supply voltage of Dbst. The voltage rating of the diode, Dbst must be V_{IN} or more, the forward current of Dbst must be 20 mA or more. Other specifications of the Dbst are not important.



Application Circuit Example

If the auxiliary power source for BST 4.5 V to 6.0 V does not have a bypass capacitor, set 0.1 μF or higher bypass capacitor between the auxiliary power source and GND.

OPERATING FREQUENCY (VERSION A/B)

In the application circuit of the R1242S001A/B, the 330 kHz operation is selected by leaving Rt open. Connecting a 200 kΩ to 0 Ω resistor between Rt (pin 8) and ground can be used to set the switching frequency to approximately 450 kHz to 1000 kHz. To calculate the Rt resistor, use the equation below:
*(Between 330 kHz and 450 kHz switching frequency can be also set by connecting the appropriate resistor according to the next equation.)

Rt = 120000 / (2 / (1000000 / f_{osc} - 1) - 1) [Ω]

The switching frequency vs. Rt value is shown in Figure 1 and Figure 2.

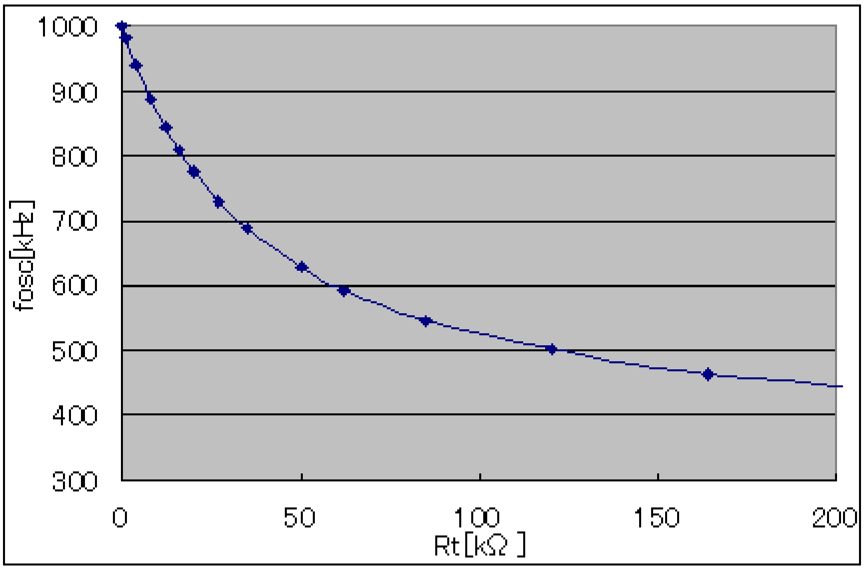


Figure 1. Linearscale

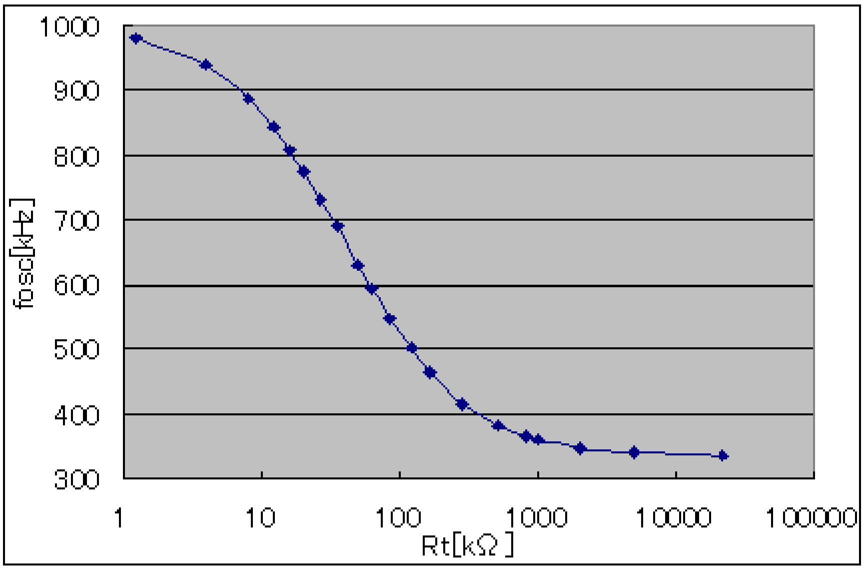


Figure 2. Logscale

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OUTPUT CURRENT AND SELECTION OF EXTERNAL COMPONENTS

The following equations explain the relationship between output current and peripheral components.

Ripple Current P-P value is described as I_{RP}, ON resistance of Highside Tr. is described as R_{ONH}, ON resistance of Lowside FET is described as R_{ONL}, and DC resistance of the inductor is described as R_L.

First, when Highside Tr. is “ON”, the following equation is satisfied.

$V_{IN} = V_{OUT} + (R_{ONH} + R_L) \times I_{OUT} + L \times I_{RP} / ton$ .... Equation 3

Second, when Highside Tr. is "OFF" (Lowside FET is "ON"), the following equation is satisfied.

$L \times I_{RP} / toff = R_{ONL} \times I_{OUT} + V_{OUT} + R_L \times I_{OUT}$ .... Equation 4

Put Equation 4 into Equation 3 to solve ON duty of Highside Tr. (D_{ON} = ton / (toff + ton)):

$D_{ON} = (V_{OUT} + (R_{ONL} + R_L) \times I_{OUT}) / (V_{IN} + (R_{ONL} - R_{ONH}) \times I_{OUT})$ .... Equation 5

Ripple Current is described as follows:

$I_{RP} = (V_{IN} - V_{OUT} - R_{ONH} \times I_{OUT} - R_L \times I_{OUT}) \times D_{ON} / fosc / L$ .... Equation 6

Peak current that flows through L, and L_X Tr. is described as follows:

$ILmax = I_{OUT} + I_{RP} / 2$ .... Equation 7

Notes: Please consider ILmax when setting conditions of input and output, as well as selecting the external components. The above calculation formulas are based on the ideal operation of the ICs in continuous mode.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed its voltage, current or power ratings. When designing a peripheral circuit, please be fully aware of the following points. (Refer to our PCB layout for detailed information).

- External components must be connected as close as possible to the ICs and their wiring must be short as possible. Especially, the capacitor must be connected with the shortest distance between V_{IN} and GND pins. If the impedances of the power supply line and the GND line are high, the operation can be unstable due to the switching current which fluctuates the electric potential of the inside the ICs. The impedances of power supply line and GND line must be as low as possible. When designing their wirings, it is necessary to give careful consideration to the large current flowing into the power supply, GND, Lx, VOUT and inductor. The wiring of output voltage setting resistance (R1) and the wiring of inductor must be separated from load wiring.
- The ceramic capacitors with low ESR (Equivalent Series Resistance) must be used for the ICs. The recommended value for the C_{IN} capacitor between VIN and GND is equal or more than 10 μF.
- The selections of inductor (L) and output capacitor (C_{OUT}) can be different according to the ICs' oscillation frequencies, output voltages and input voltages. Refer to "Recommended Value for Each Output Voltage" on the next page and select the most suitable values at the conditions of use. The internal phase compensation is built in the ICs; therefore, if the values selected are largely deviated from the recommended values, the operation may result in unstable.
- The over current protection circuit could be influenced by self-heating of the ICs and heat dissipation of the PCB environment.
- In order to prevent self-turning on, FET with smaller gate resistance and with smaller Cgd/ Cgs (capacities between gate drains and the capacities between gate sources) should be selected.
- The output voltage (V_{OUT}) can be calculated as $V_{OUT} = V_{FB} \times (R1 + R2) / R2$. The various voltage settings are possible by changing the values of R1 and R2. However, R2 value must be equal or less than 16 kΩ.
- Rspd prevents the deterioration in the regulation characteristics, which is caused by spike noise occurred in V_{OUT}. Spike noise is largely depending on the PCB layout. If the PCB board layout is optimized, there is no need of Rspd; however, if the spike noise is a concern, Rspd with 15 Ω or so should be used.
- After the completion of soft start, latch function (Ver. A, C, E, G) starts to work. The internal counter starts counting up when the over current protection circuit activates the limited current detection. When the internal counter counts up to 5ms, which is a typical delay time for latch protection, the latch function turns off the output. The turned off output can be reset when CE pin is changed to "L", and also V_{IN} pin voltage is became less than 3.6 V (Typ.), which is UVLO detecting voltage. If the output voltage increases more than the setting voltage (VFB pin voltage is 0.8 V (Typ.)) within the delay time for latch protection, the counter restores the default. If the power-supply voltage's start-up is slow and the output voltage is not reached to the setting voltage within the delay time for latch protection after the soft start, the careful attention is required.

- After the soft start, fold back function (Ver. B, D, F, H) starts to work. The fold back function limits the oscillation frequencies into 1/4 when (VFB pin voltage decreases to less than 0.56 V (Typ.)). If the power-supply voltage's start-up is slow and the output voltage is not reached to the 70% of the setting voltage even for a short period of time after the soft start, the careful attention is required.
- The ICs are not supporting Nonsynchronous rectification using a diode as a rectifier.
  The following table shows the recommended values for setting frequency and setting output voltage.

Recommended Values

330 kHz

V_{OUT} [V]	0.8	1.2	1.2	1.5	1.5	1.8	1.8	2.5	2.5	3.3	5	9	15
V_{IN} Range [V]	5~14	~12	9~30	5~10	10~30	5~15	12~30	5~15	12~30	5~30	7~30	15~30	20~30
L [μH]	2.2	10	4.7	10	4.7	15	4.7	15	10	15	15	15	15
C_{OUT} [μF]	100	22	44	22	44	22	44	22	22	22	22	22	22
Cspd [pF]	-	470	470	220	220	470	220	220	220	220	220	220	220->100
R1 [Ω]	-	8000	8000	14000	14000	20000	20000	34000	34000	50000	84000	164000	284000
R2 [Ω]	-	16000	16000	16000	16000	16000	16000	16000	16000	16000	16000	16000	16000

500 kHz

V_{OUT} [V]	0.8	1.0	1.2	1.5	1.5	1.8	1.8	2.5	3.3	5	9	12	15
V_{IN} Range [V]	~9	~10	5~15	5~18	7~19	5~23	9~21	5~29	5~30	7~30	15~30	18~30	20~30
L [μH]	2.2	2.2	2.2	4.7	2.2	4.7	2.2	10	10	10	10	15	15
C_{OUT} [μF]	100	44	44	44	44	44	44	22	22	22	22	22	22
Cspd [pF]	-	1000	470	220	220	220	220	220	220	220	220	220	220
R1 [Ω]	-	4000	8000	14000	14000	20000	20000	34000	50000	84000	164000	224000	284000
R2 [Ω]	-	16000	16000	16000	16000	16000	16000	16000	16000	16000	16000	16000	16000

1000 kHz

V_{OUT} [V]	0.8	1.2	1.5	1.8	2.5	3.3	5	5	9	15
V_{IN} Range [V]	5~7	5~10	5~15	5~15	5~19	5~30	7~12	12~30	15~30	20~30
L [μH]	1.5	2.2	2.2	4.7	4.7	4.7	4.7	4.7	4.7	10
C_{OUT} [μF]	100	22	22	22	22	10	10	10	10	10
Cspd [pF]	-	220	100	220	220	100	100	56	56	100
R1 [Ω]	-	8000	14000	20000	34000	50000	84000	84000	164000	284000
R2 [Ω]	-	16000	16000	16000	16000	16000	16000	16000	16000	16000

Recommended External Components

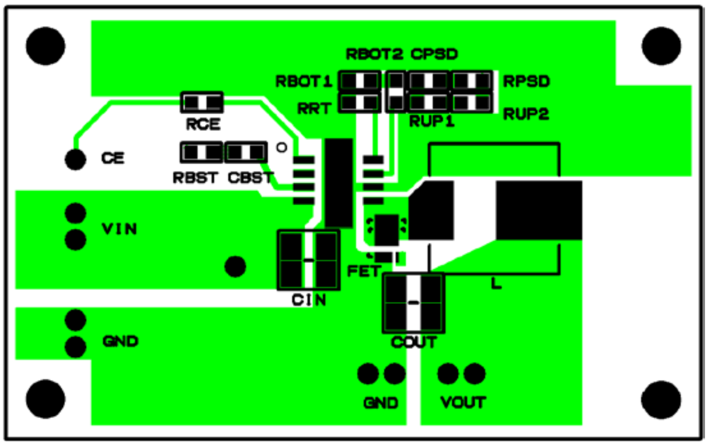
Symbol	Condition	Value	Parts Name	MFR
C_{IN}		10 μF/ 50 V	UMK325BJ106MM-P	TAIYO YUDEN
		10 μF/ 50 V	CGA6P3X7S1H106K	TDK
		10 μF/ 50 V	KTS500B106M55N0T00	Nippon Chemi-Con
		10 μF/ 10 V	GRM31CR71A106K	Murata
C_{OUT}	V_{OUT} > 10 V	10 μF/ 50 V	KTS500B106M55N0T00	Nippon Chemi-Con
	10 V > V_{OUT} > 1.8 V	10 μF/ 25 V	GRM31CR71E106K	Murata
	V_{OUT} < 1.8 V	22 μF/ 10 V	GRM31CR71A226M	Murata
			(at the diode rectifier, the specified condition only)	
C_{BST}		0.1 μF/ 50 V	GRM21BB11H104KA01L	Murata
L	1.5 μH ±30%/ 4.0 A	1.5 μH	SLF7055T-1R5N4R0-3PF	TDK
	2.2 μH ±20%/ 5.4 A	2.2 μH	RLF7030T-2R2M5R4	TDK
	4.7 μH ±30%/ 6.1 A	4.7 μH	VLF10045T-4R7N6R1	TDK
	10 μH ±20% 6.2 A	10 μH	VLF12060T-100M6R2	TDK
	15 μH ±20% 5.0 A	15 μH	VLF12060T-150M5R0	TDK
FET	30 V/11 A	12.6 mΩ	TPN11003NL	TOSHIBA
	30 V/20 A	10.2 mΩ	TPN8R903NL	TOSHIBA
	30 V/6 A	56 mΩ	SSM3K335R	TOSHIBA
R_{CE}	The diode is connected between CE pin and VIN pin as an ESD protection element.			
	If there is a possibility that the CE pin voltage becomes higher than the VIN pin voltage,			
	it is recommended to insert a 5 kΩ resistance or more in order to prevent the large current			
	flowing from CE pin into VIN pin.			

TECHNICAL NOTES ON PCB LAYOUT PATTERN

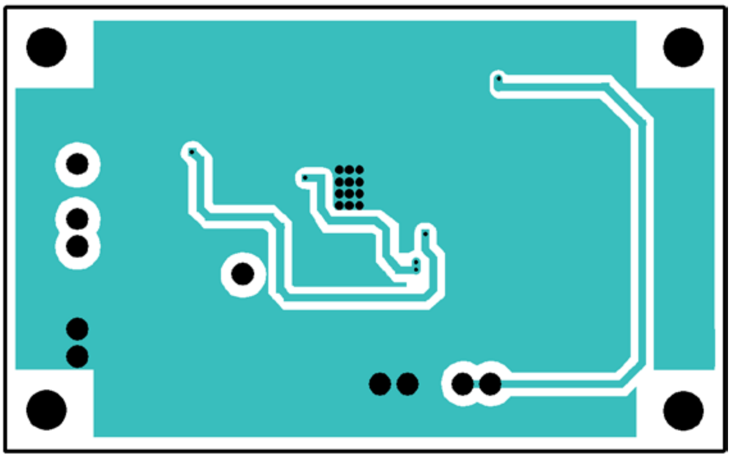
1. Make the power line (VIN and GND) broad to avoid the generation of the parasitic inductance. Place the bypass capacitor (C_{IN}) between VIN and GND as close as possible to each other.
2. Make the wire between Lx pin and the inductor as short as possible to avoid the generation of the parasitic inductance. (This Evaluation Board is designed for the testing. Therefore, the inductor is large, a diode is connectable, and the large space is secured for Lx part.)
3. The ripple current passes through the output capacitor; therefore, if the C_{OUT}'s GND is placed in the outside of the C_{IN}'s GND side and the IC's GND, the IC can be easily affected by the noise.
4. Mount R_{UP}, R_{BOT}, C_{SPD} and R_{SPD} on the place where the FB pin is close and the inductor and the BST pin are away.
5. Start the feedback from where the output capacitor (C_{OUT}) is close.

PCB LAYOUT

TOP VIEW



BOTTOM VIEW



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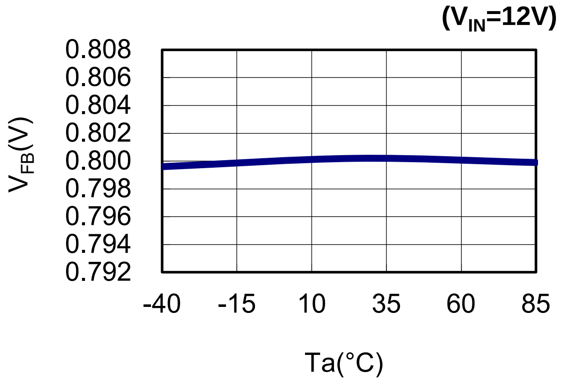
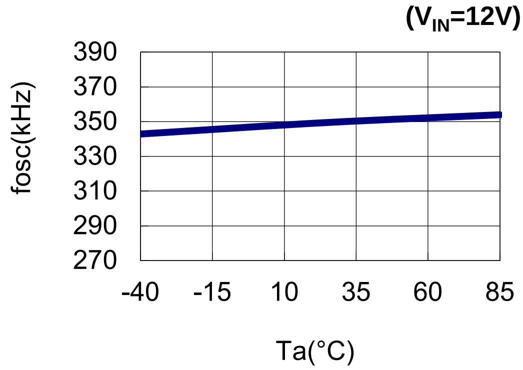
TYPICAL CHARACTERISTICS

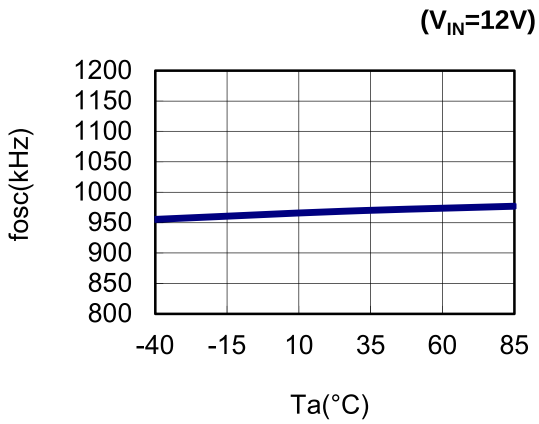
1)FB Voltage



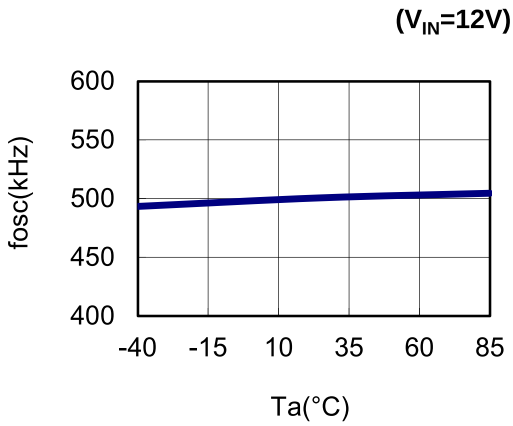
2)Oscillator Frequency(ver.A,B Rt=floating)



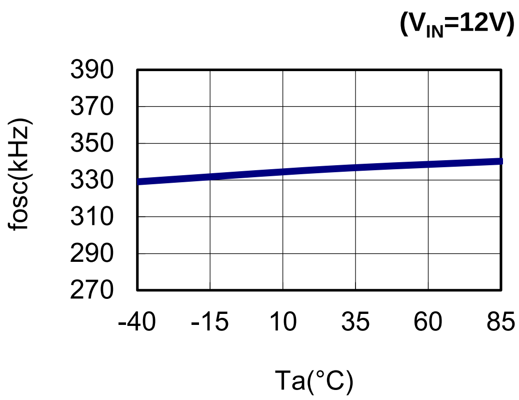
3)Oscillator Frequency(ver.A,B Rt=GND)



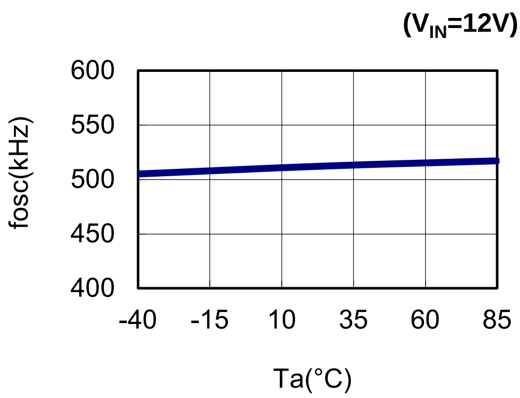
4)Oscillator Frequency(ver.A,B Rt=120kΩ)



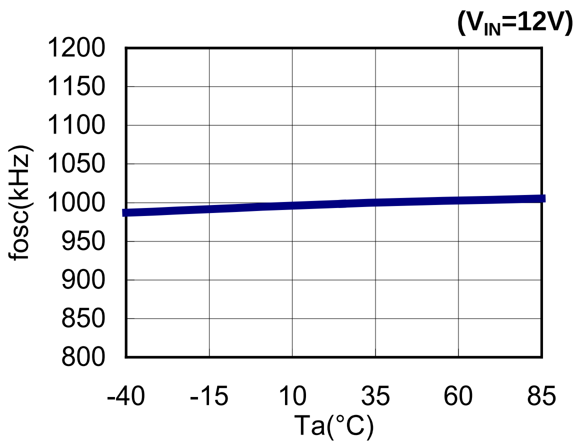
5)Oscillator Frequency(ver.C,D)



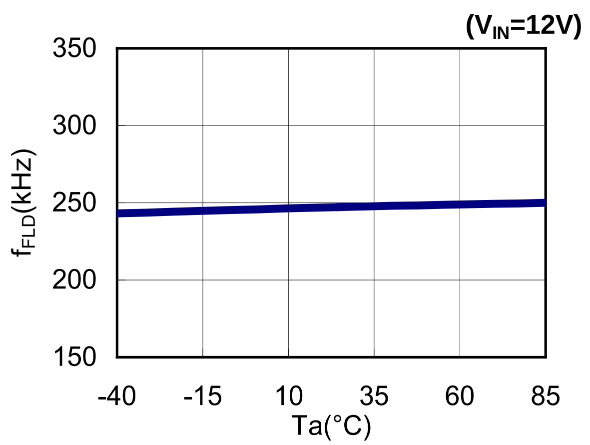
6) Oscillator Frequency(ver.E,F)



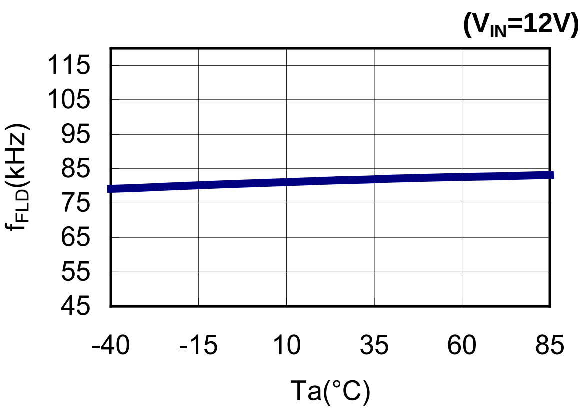
7) Oscillator Frequency(ver.G,H)



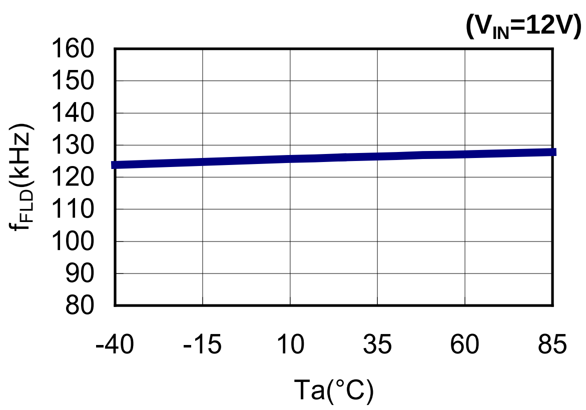
8) Fold-Back Frequency(ver.A,B Rt=GND)



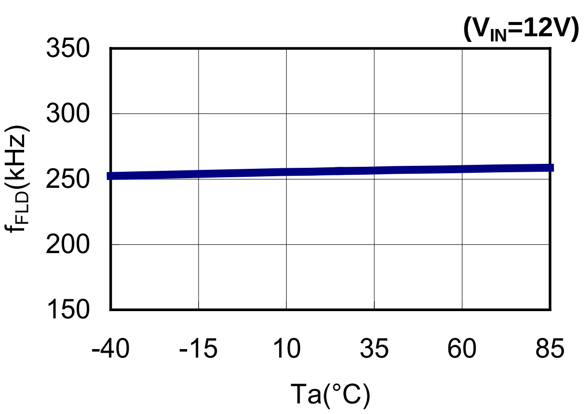
9) Fold-Back Frequency(ver.C,D)



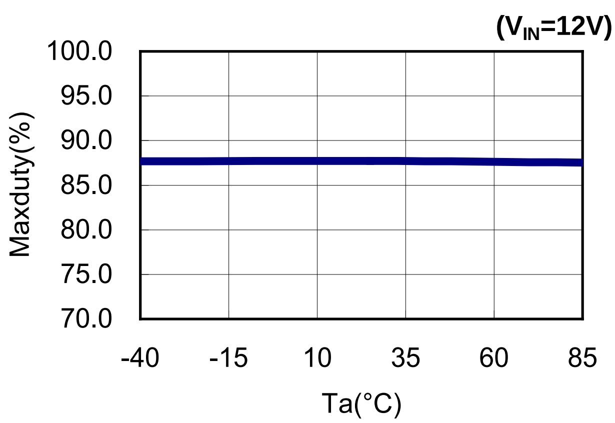
10) Fold-Back Frequency(ver.E,F)



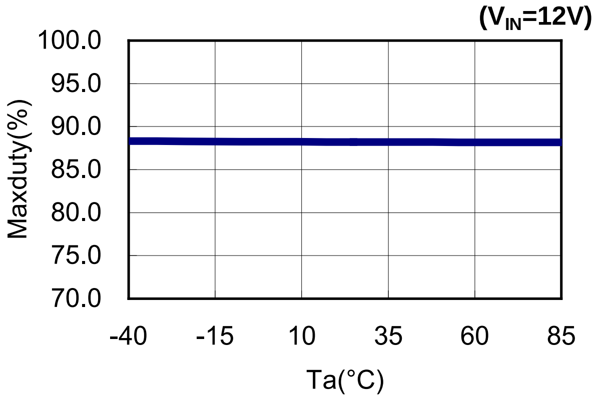
11) Fold-Back Frequency(ver.G,H)



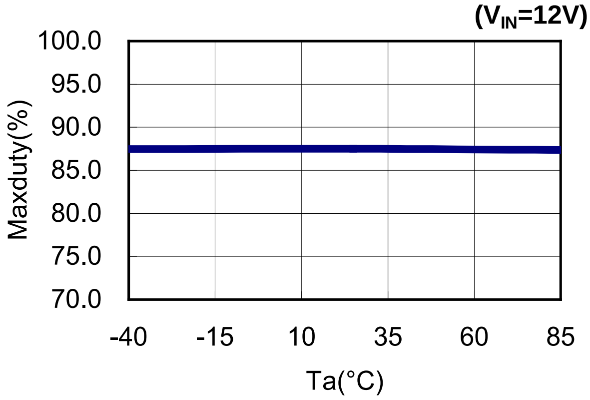
12) Maxduty(ver.A,B Rt=floating)



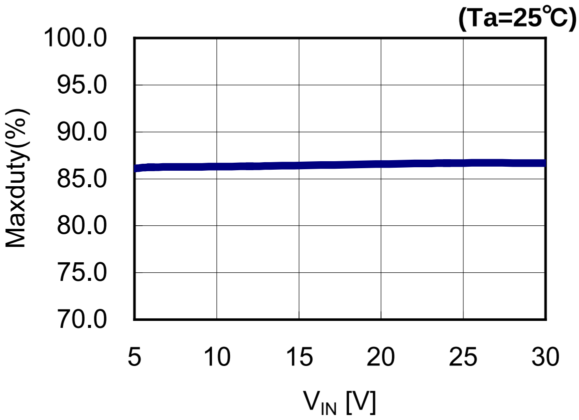
13) Maxduty(ver.C,D)



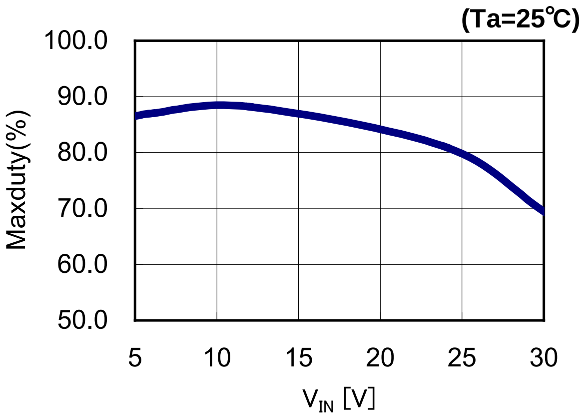
14) Maxduty(ver.G,H)



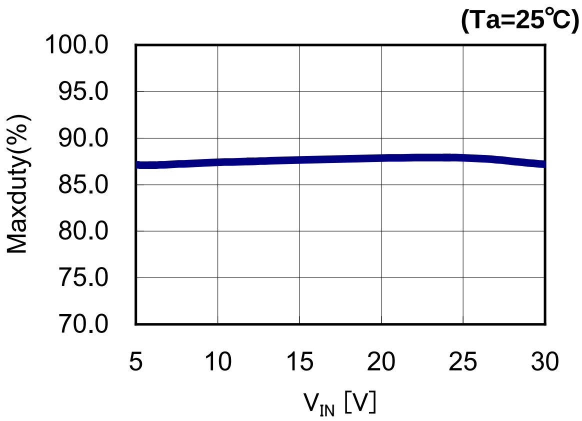
15) Maxduty(ver.A,B Rt=GND)



16) Maxduty(ver.C,D)



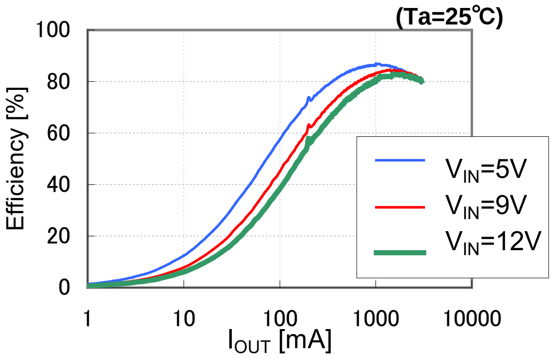
17) Maxduty(ver.G,H)



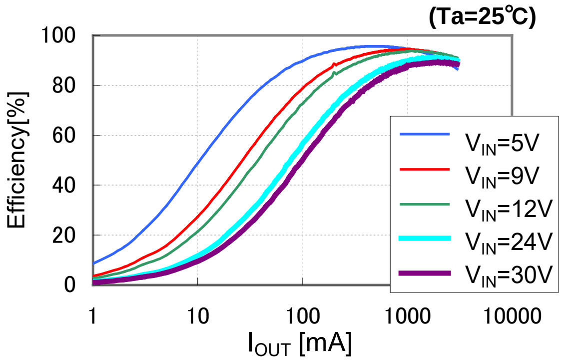
18)Efficiency vs Load Current

fosc=330kHz

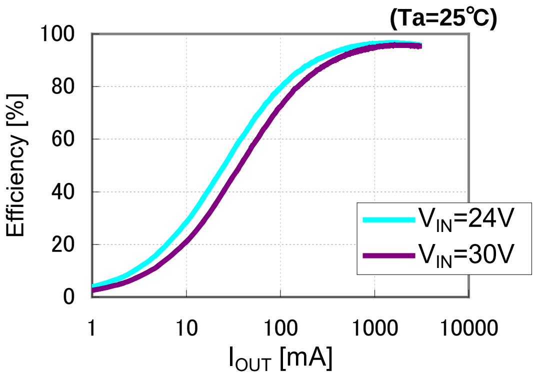
V_{OUT}:0.8V



V_{OUT}:3.3V

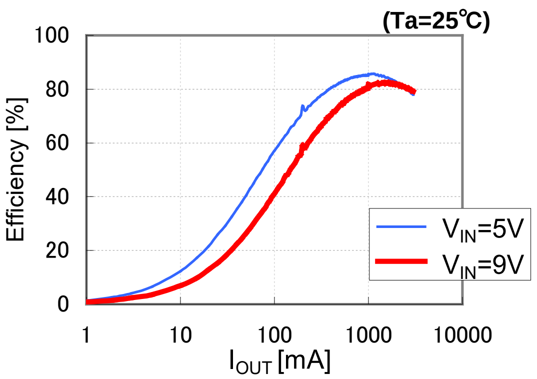


V_{OUT}:15V

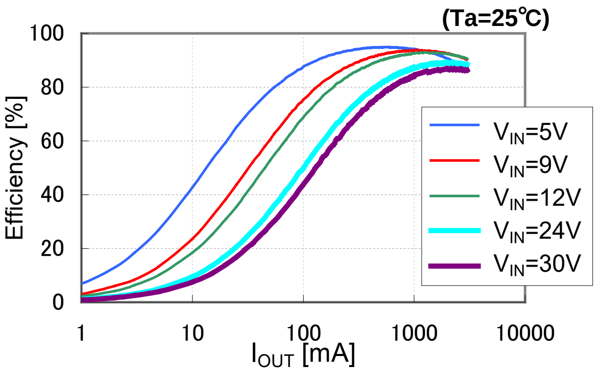


fosc=500kHz

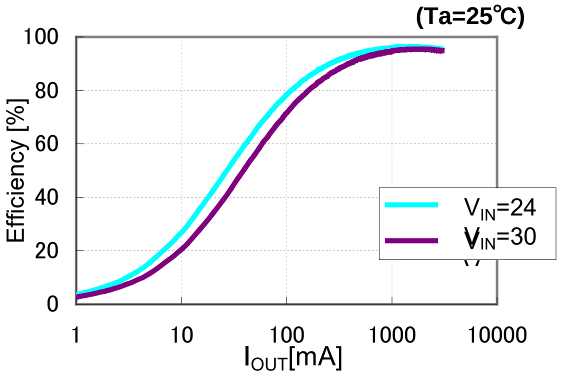
V_{OUT}:0.8V



V_{OUT}:3.3V

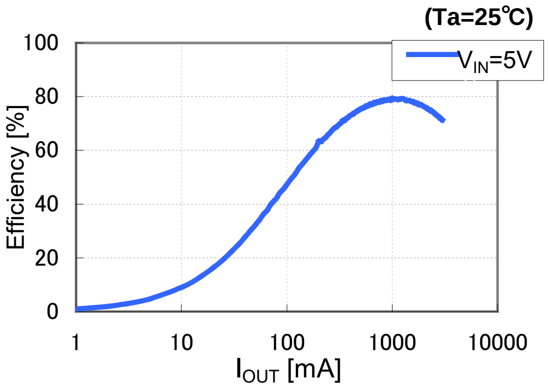


V_{OUT}:15V

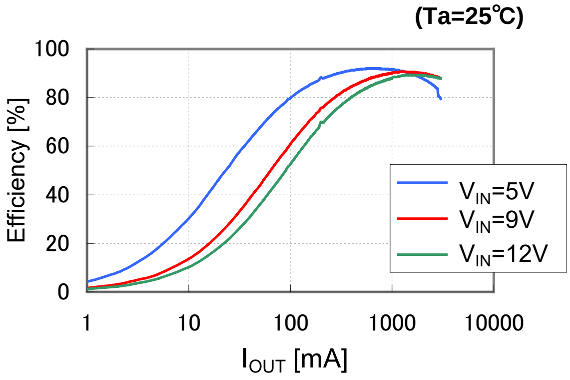


fosc=1000kHz

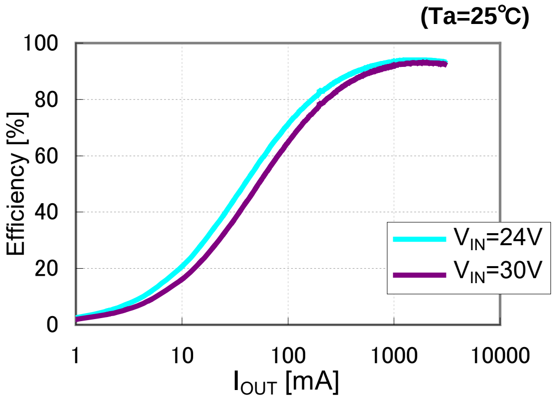
V_{OUT}:0.8V



V_{OUT}:3.3V



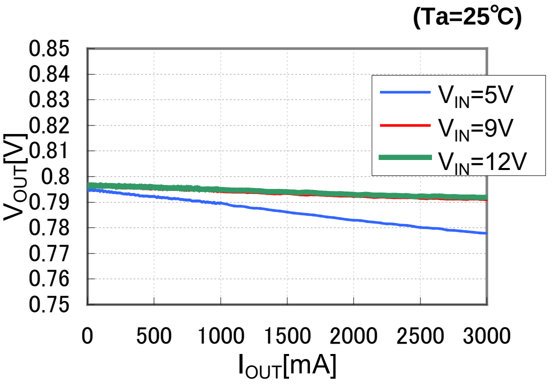
V_{OUT}:15V



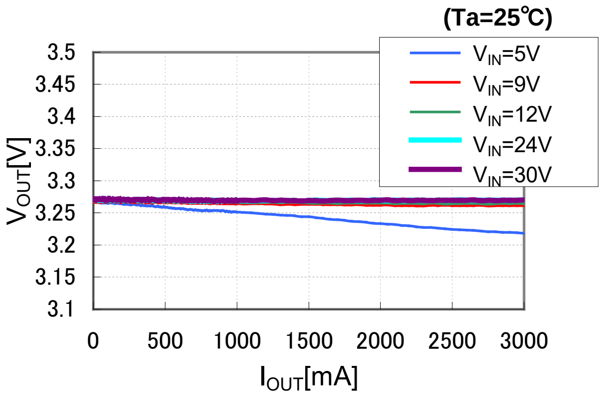
19)Load Regulation

fosc=330kHz

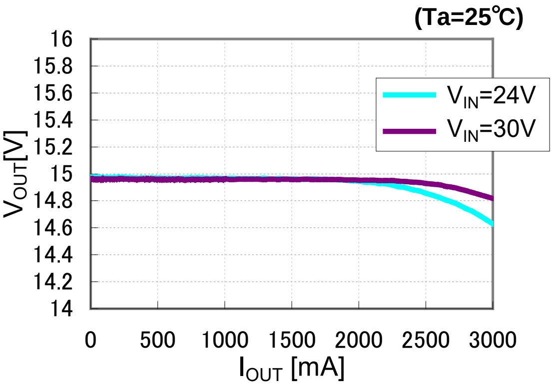
V_{OUT}:0.8V



V_{OUT}:3.3V

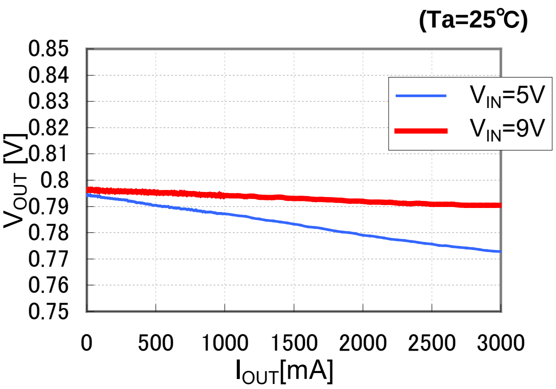


V_{OUT}:15V

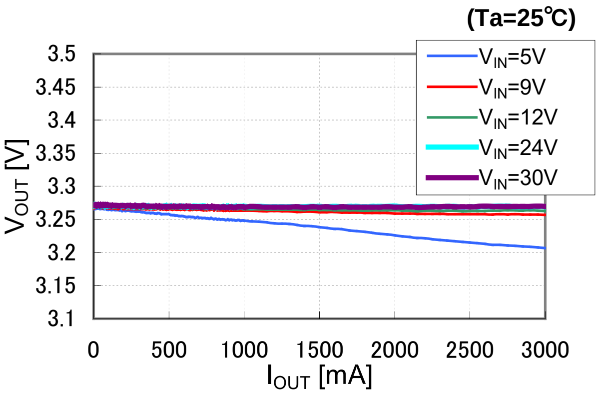


fosc=500kHz

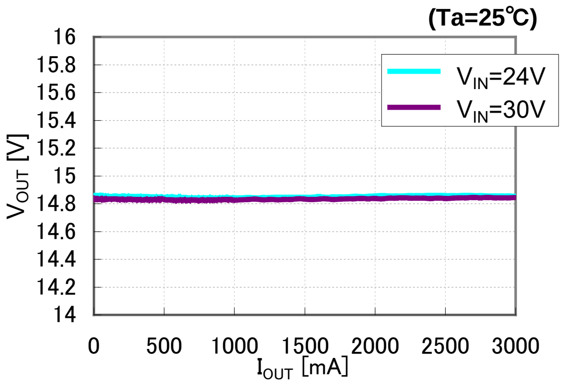
V_{OUT}:0.8V



V_{OUT}:3.3V

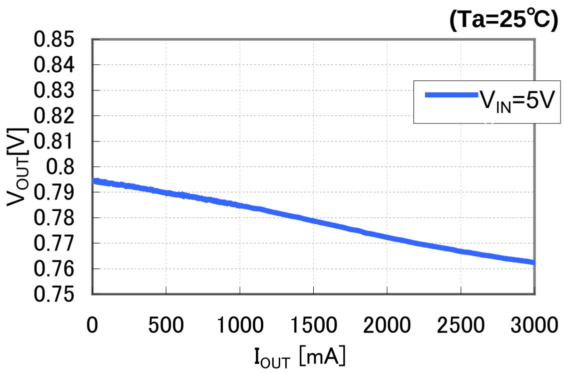


V_{OUT}:15V

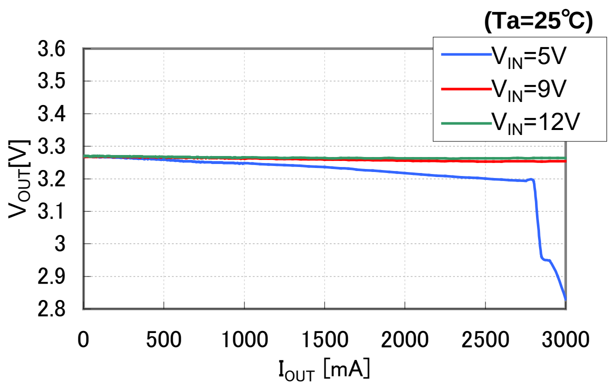


fosc=1000kHz

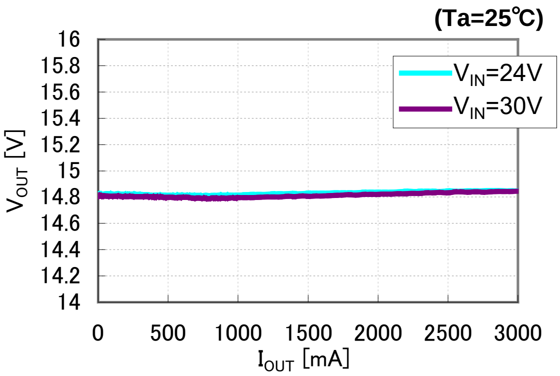
V_{OUT}:0.8V



V_{OUT}:3.3V



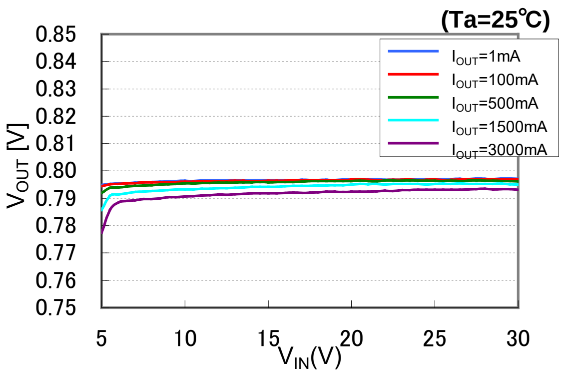
V_{OUT}:15V



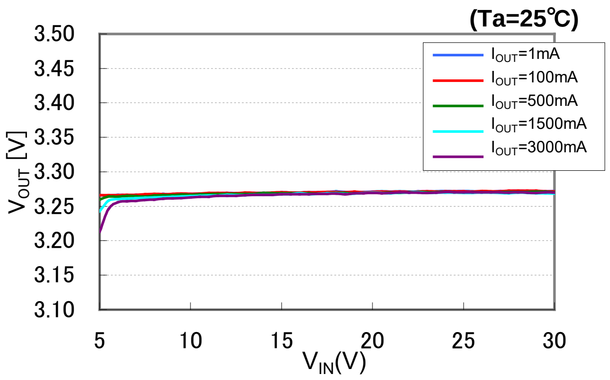
20)Line Regulation

fosc=330kHz

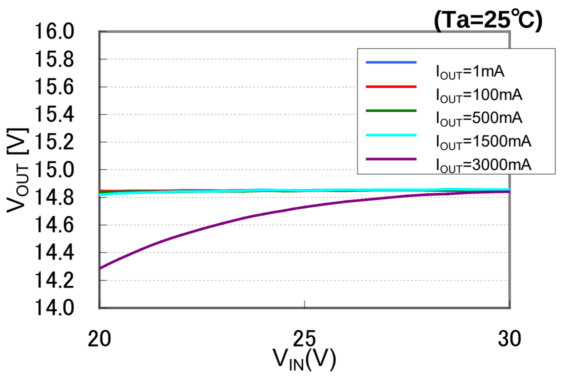
V_{OUT}:0.8V



V_{OUT}:3.3V

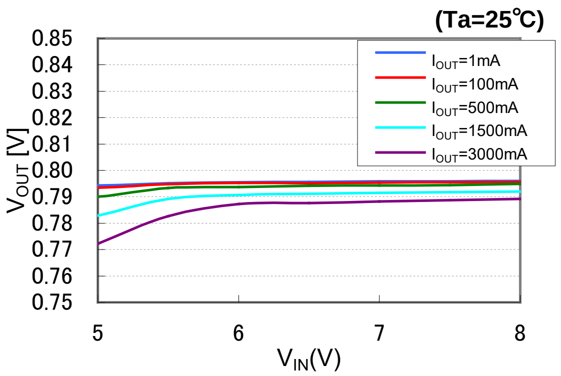


V_{OUT}:15V

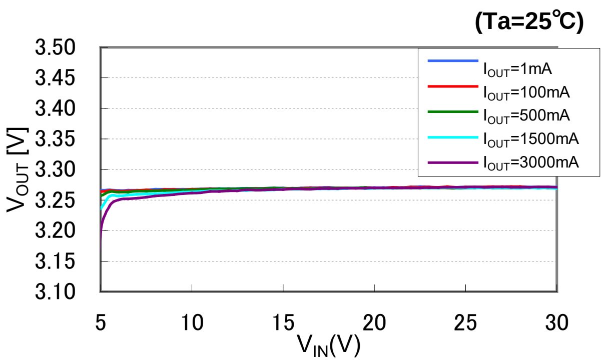


fosc=500kHz

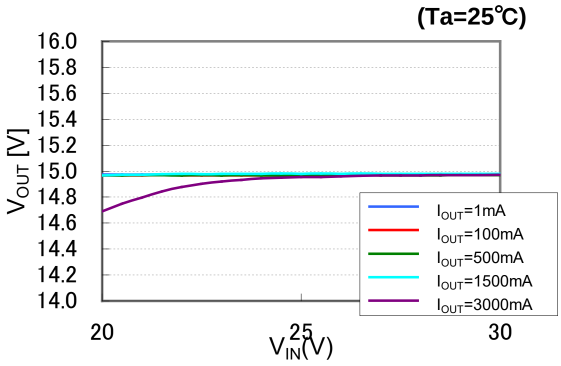
V_{OUT}:0.8V



V_{OUT}:3.3V

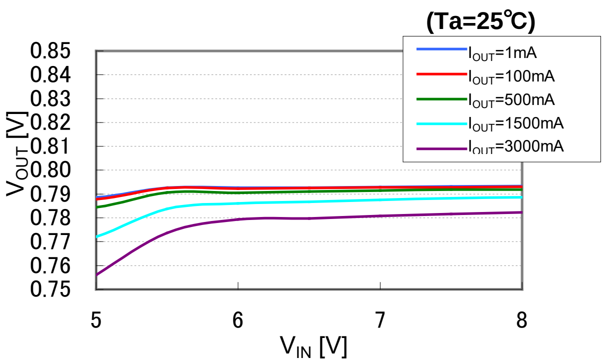


V_{OUT}:15V

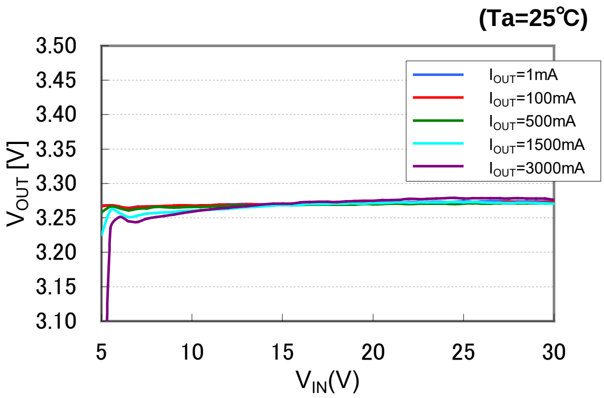


fosc=1000kHz

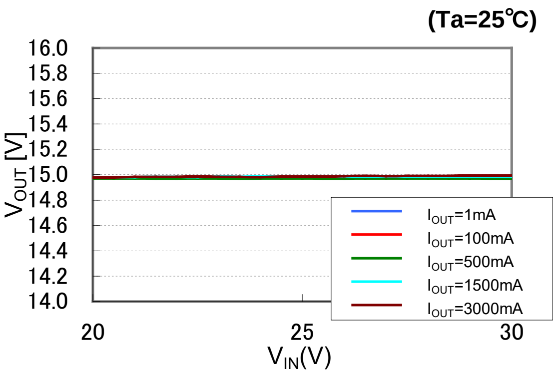
V_{OUT}:0.8V



V_{OUT}:3.3V



V_{OUT}:15V



Ver. A

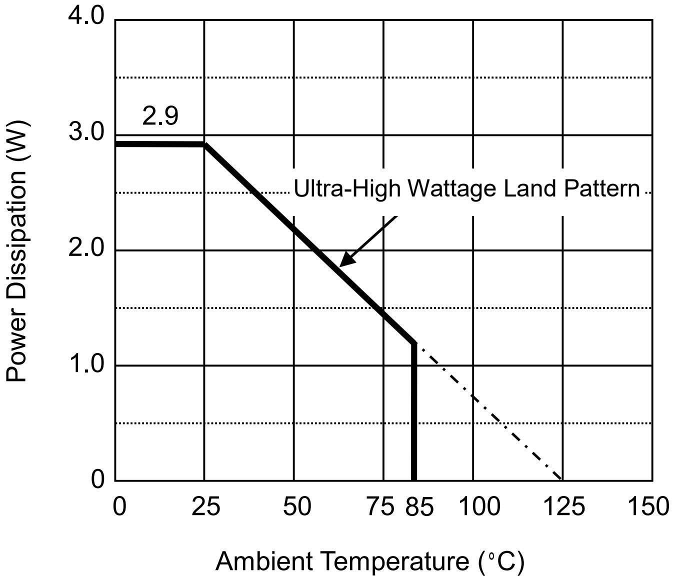
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

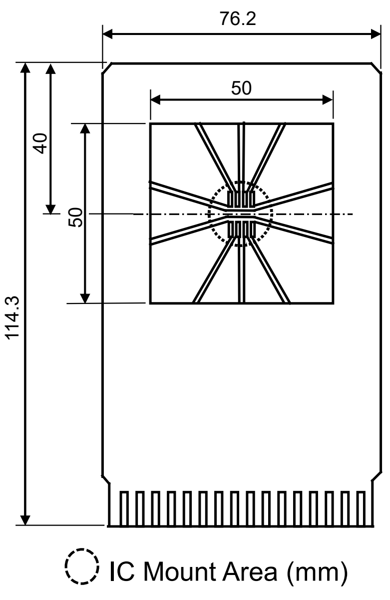
	Ultra-High Wattage Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layers (First and Fourth Layers): Approx. 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.4 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

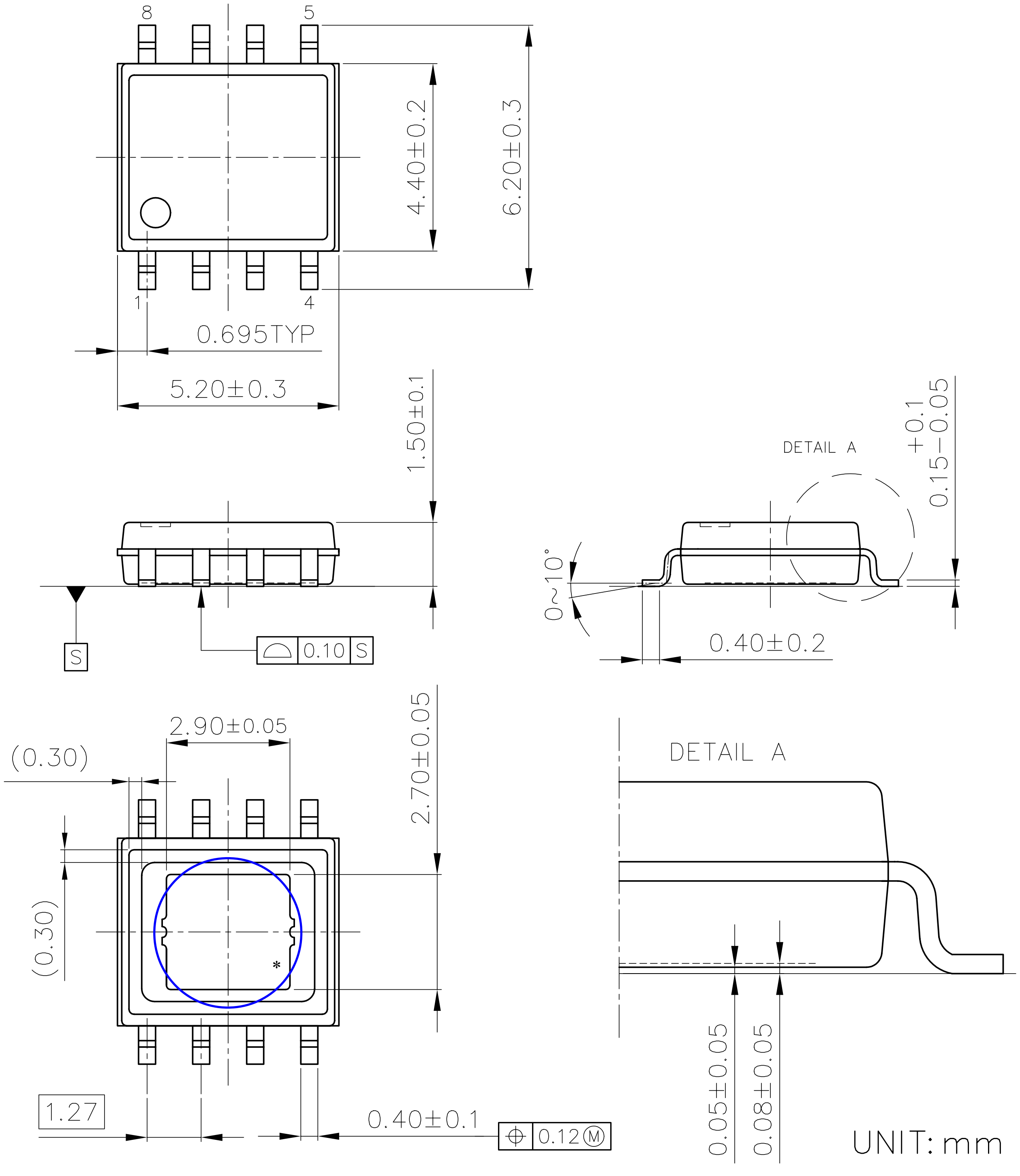
	Ultra-High Wattage Land Pattern
Power Dissipation	2.9 W
Thermal Resistance	$\theta ja = (125 - 25°C) / 2.9 W = 35°C/W$ $\theta jc = 10°C/W$



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



HSOP-8E Package Dimensions

∗ The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

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Halogen Free

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RICOH ELECTRONIC DEVICES CO., LTD.

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Sales & Support Offices

Ricoh Electronic Devices Co., Ltd.
Shin-Yokohama Office (International Sales)
2-3, Shin-Yokohama 3-chome, Kohoku-ku, Yokohama-shi, Kanagawa, 222-8530, Japan
Phone: +81-50-3814-7687 Fax: +81-45-474-0074

Ricoh Americas Holdings, Inc.
675 Campbell Technology Parkway, Suite 200 Campbell, CA 95008, U.S.A.
Phone: +1-408-610-3105

Ricoh Europe (Netherlands) B.V.
Semiconductor Support Centre
Prof. W.H. Keesomlaan 1, 1183 DJ Amstelveen, The Netherlands
Phone: +31-20-5474-309

Ricoh International B.V. - German Branch
Semiconductor Sales and Support Centre
Oberrather Strasse 6, 40472 Düsseldorf, Germany
Phone: +49-211-6546-0

Ricoh Electronic Devices Korea Co., Ltd.
3F, Haesung Bldg, 504, Teheran-ro, Gangnam-gu, Seoul, 135-725, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2051-5713

Ricoh Electronic Devices Shanghai Co., Ltd.
Room 403, No.2 Building, No.690 Bibo Road, Pu Dong New District, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

Ricoh Electronic Devices Shanghai Co., Ltd.
Shenzhen Branch
1205, Block D(Jinlong Building), Kingkey 100, Hongbao Road, Luohu District, Shenzhen, China
Phone: +86-755-8348-7600 Ext 225

Ricoh Electronic Devices Co., Ltd.
Taipei office
Room 109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan (R.O.C.)
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623