RoboClockII CY7B994V CY7B993V

ADVANCED INFORMATION

High-Speed Multi-Phase PLL Clock Buffer

Features

- **Matched pair outputs skew <200 ps (200 ps MAX)**
- **3.3V BiCMOS Technology**
- **12–100 MHz (CY7B993V), or 24–185 MHz (CY7B994V) output operation**
- **18 3.3V LVTTL outputs**
- **User-selectable output functions**
  - **—Minimum Phase adjustments of 625ps**
  - **—Operation at input:output frequency ratios of (1,2,3,4,5,6,8,10,12):(1,2,3,4,5,6,8,10,12)**
  - **—Individual Output disable per output bank for agressive power management and EMI reduction**
  - **—Output high impedance option for testing purposes**
- **PLL Lock indicator pin**
- **Zero input to output delay**
- **3.3V LVTTL/LvPECL reference inputs**
- **50% duty-cycle outputs**
- **Outputs capable of driving 50Ω terminated lines**
- **Fault Tolerant and Hot Insertable reference inputs**
- **Fully integrated PLL for reduced jitter**
- **Low Cycle-to-Cycle Jitter (<100 ps peak-peak)**
- **100-pin TQFP package A100**

Functional Description

The CY7B993V and CY7B994V, High-Speed Multi-Phase PLL Clock buffers, offer user-selectable control over system clock functions. This multiple-output clock driver provides the system integrator with functions necessary to optimize the timing of high-performance computer and communication systems. Eighteen configurable outputs can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews at LVTTL logic levels.

The 18 outputs are arranged in five banks. There are four banks of four outputs which allow both phase and frequency adjustments. The fifth bank consists of two outputs, which allow divide-by functionality from 1 to 12 and limited phase adjustments. These outputs are intended to be connected to the feedback input as well as driving other inputs. The completely integrated PLL reduces jitter and simplifies board layout.

Logic Block Diagram