

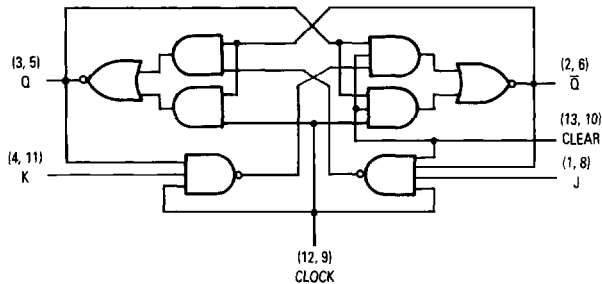


Dual J-K Flip-Flop With Clear

**ELECTRICALLY TESTED PER:
MIL-M-38510/30108**

The 54LS107A is a Dual J-K flip-flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH to LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

**LOGIC DIAGRAM
(one half show)**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT — TRUTH TABLE						
Operating Mode	Inputs			Outputs		
	\bar{C}_D	J	K	Q	\bar{Q}	
Reset (Clear)	L	X	X	L	H	
Toggle	H	h	h	\bar{q}	q	
Load "0" (Reset)	H	l	h	L	H	
Load "1" (Set)	H	h	l	H	L	
Hold	H	l	l	q	\bar{q}	

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

Military 54LS107A



AVAILABLE AS:

- 1) JAN: JM38510/30108BXA
- 2) SMD: *
- 3) 883C: 54LS107A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

*Call Factory for latest update

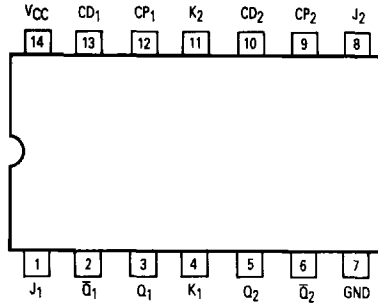
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
J ₁	1	1	2	VCC
\bar{Q}_1	2	2	3	VCC
Q ₁	3	3	4	OPEN
K ₁	4	4	6	VCC
Q ₂	5	5	8	OPEN
\bar{Q}_2	6	6	9	VCC
GND	7	7	10	GND
J ₂	8	8	12	VCC
CLK ₂	9	9	13	VCC
CLR ₂	10	10	14	GND
K ₂	11	11	16	VCC
CLK ₁	12	12	18	VCC
CLR ₁	13	13	19	GND
VCC	14	14	20	VCC

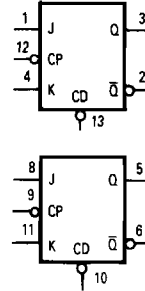
**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

54LS107A

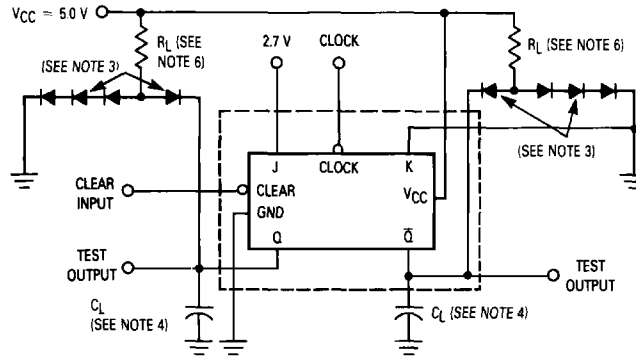
CONNECTION DIAGRAM



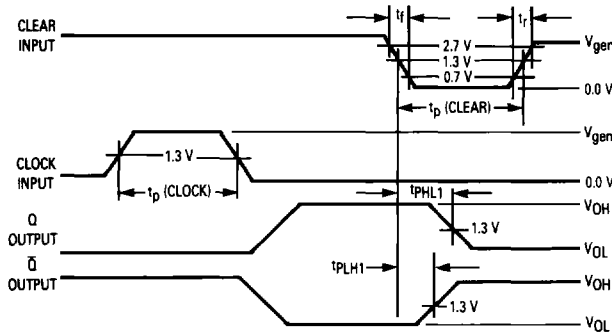
LOGIC SYMBOL



AC TEST CIRCUIT



WAVEFORMS



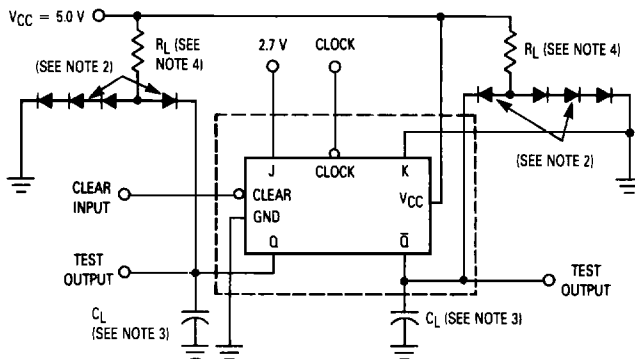
Clear Switching Test Circuit and Waveforms

NOTES:

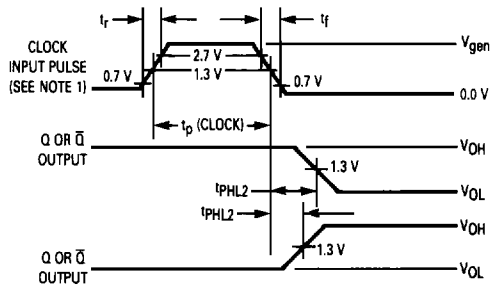
1. Clear inputs dominate regardless of the state of the clock or J-K inputs.
2. Clear input pulse characteristics:
 $V_{gen} = 3.0\text{ V}$, $t_r \leq 15\text{ ns}$, $t_f \leq 6.0\text{ ns}$,
 $t_p(\text{clear}) = 30\text{ ns}$, $\text{PRR} \leq 1.0\text{ MHz}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. Voltage measurements are to be made with respect to network ground terminal.
6. $R_L = 2.0\text{ k}\Omega \pm 5.0\%$.
7. Clock input pulse characteristics:
 $V_{gen} = 3.0\text{ V}$, $t_p(\text{clock}) = 25\text{ ns}$,
 $\text{PRR} \leq 1.0\text{ MHz}$.

54LS107A

AC TEST CIRCUIT



WAVEFORMS



Synchronous Switching Test Circuit

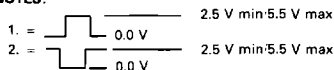
NOTES:

1. Clock input characteristics for t_{PLH} , t_{PHL} (clock to output):
 $V_{gen} = 3.0\text{ V}$, $t_r \leq 15\text{ ns}$, $t_f = 6.0\text{ ns}$, $t_p(\text{clock}) = 25\text{ ns}$ and
 $PRR \leq 1.0\text{ MHz}$. When testing t_{MAX} the clock input characteristics
are: $V_{gen} = 3.0\text{ V}$, $t_r = t_f \leq 6.0\text{ ns}$, $t_p(\text{clock}) \leq 20\text{ ns}$ and
 $PRR = \text{see table 1}$.
2. All diodes are 1N3064, or equivalent.
3. $C_L = 50\text{ pF} \pm 10\%$ (including jig and probe capacitance).
4. $R_L = 2.0\text{ k}\Omega \pm 5.0\%$.

54LS107A

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
Static Parameters:		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -0.4 mA, V _{IN} = 2.0 V, V _{IL} = 0.7 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V, V _{IL} = 0.7 V.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current (J & K inputs)		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other input = 4.5 V, CLK & CLR = GND.
I _{IHH}	Logical "1" Input Current (J & K inputs)		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other input = 4.5 V, CLK & CLR = GND.
I _{IH}	Logical "1" Input Current (CLR inputs)		60		60		60	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other input = 4.5 V, CLK & J = GND.
I _{IHH}	Logical "1" Input Current (CLR inputs)		300		300		300	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other input = 4.5 V, CLK & J = GND.
I _{IH}	Logical "1" Input Current (CLK inputs)		80		80		80	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, CLR - K & J = GND.
I _{IHH}	Logical "1" Input Current (CLK inputs)		400		400		400	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, CLR - K & J = GND.
I _{IL}	Logical "0" Input Current (J & K inputs)	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, CLR & J = 4.5 V, CLK = (See Note 2).
I _{IL}	Logical "0" Input Current (CLK inputs)	-0.24	-0.72	-0.24	-0.72	-0.24	-0.72	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, J & K = 4.5 V, CLR = (See Note 2).
I _{IL}	Logical "0" Input Current (CLR inputs)	-0.12	-0.72	-0.12	-0.72	-0.12	-0.72	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, CLR - J & K = 4.5 V.
I _{OS}	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, CLK - CLR & J = GND, V _{OUT} = 2.25 V.
I _{CC}	Power Supply Current		8.0		8.0		8.0	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), or V _{IN} = 5.5 V, other inputs = 0 V.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

NOTES:



54LS107A

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
	Min	Max	Min	Max	Min	Max			
t _{PHL1} t _{PHL1}	Propagation Delay Data-Output Output <u>High-Low</u>	5.0	28 20	5.0	40 35	5.0	40 35	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH1} t _{PLH1}	Propagation Delay Data-Output Output <u>Low-High</u>	5.0	21 20	5.0	32 27	5.0	32 27	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PHL2} t _{PHL2}	Propagation Delay Data-Output Output <u>High-Low</u>	5.0	30 20	5.0	42 37	5.0	42 37	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
t _{PLH2} t _{PLH2}	Propagation Delay Data-Output Output <u>Low-High</u>	5.0	22 20	5.0	32 27	5.0	32 27	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	25		25		25		MHz	V _{CC} = 5.0 V, V _{IN} = 2.7 V, C _L = 50 pF, R _L = 2.0 kΩ ± 5.0%.
f _{MAX}	Maximum Clock Frequency	30						MHz	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ ± 5.0%.

NOTES:

1. f_{MAX}, min. limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
2. Tests shall be performed in sequence, attributes data only.
3. The limits specified for C_L = 15 pF are guaranteed but not tested.