

74LVC126A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

Rev. 7 — 9 December 2011

Product data sheet

1. General description

The 74LVC126A consists of four non-inverting buffers/line drivers with 3-state outputs, which are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC126AD	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC126ADB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVC126APW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC126ABQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1



4. Functional diagram

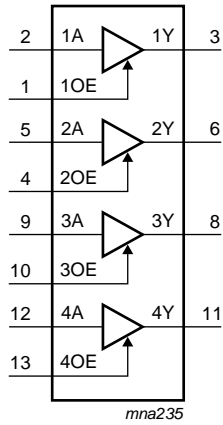


Fig 1. Logic symbol

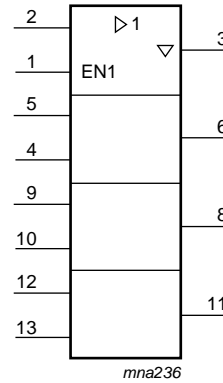


Fig 2. IEC logic symbol

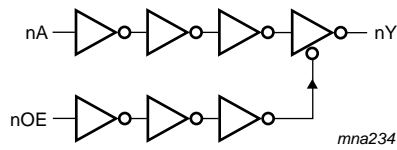
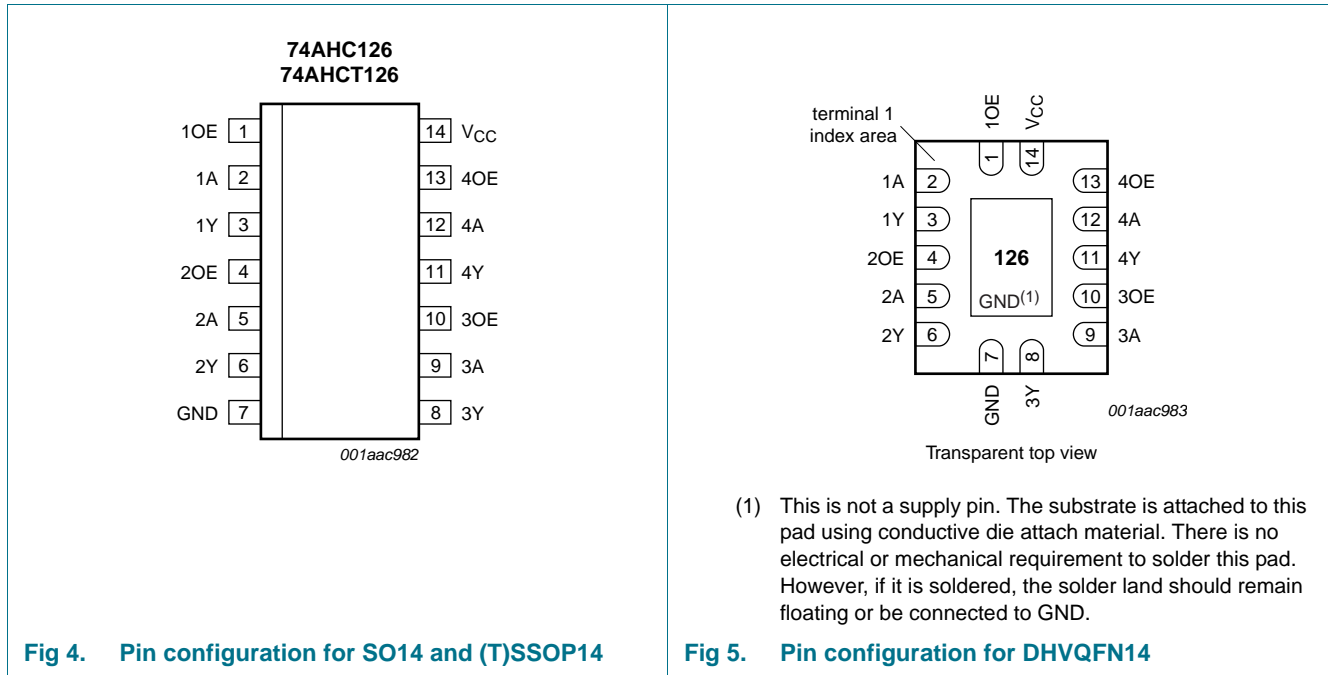


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	data enable input (active HIGH)
1A	2	data input
1Y	3	data output
2OE	4	data enable input (active HIGH)
2A	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3OE	10	data enable input (active HIGH)
4Y	11	data output
4A	12	data input
4OE	13	data enable input (active HIGH)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Inputs		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

- [1] H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH or LOW-state	[2] -0.5	V _{CC} + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		[3] -65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	-	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.
 [3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
		output 3-state	0	-	5.5	V

Table 5. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND;	-	±0.1	±5	-	±20	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 1.65 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit		
			Min	Typ ^[1]	Max	Min	Max			
t _{pd}	propagation delay	nA to nY; see Figure 6 ^[2]								
		V _{CC} = 1.2 V	-	11.0	-	-	-	ns		
		V _{CC} = 1.65 V to 1.95 V	1.5	5.2	10.8	1.5	12.6	ns		
		V _{CC} = 2.3 V to 2.7 V	1.0	2.8	5.6	1.0	6.6	ns		
		V _{CC} = 2.7 V	1.5	2.7	5.2	1.5	6.5	ns		
t _{en}	enable time	nOE to nY; see Figure 7 ^[2]								
		V _{CC} = 1.2 V	-	15.0	-	-	-	ns		
		V _{CC} = 1.65 V to 1.95 V	2.4	6.7	12.9	2.4	15.0	ns		
		V _{CC} = 2.3 V to 2.7 V	2.0	3.8	7.1	2.0	8.3	ns		
		V _{CC} = 2.7 V	1.5	3.1	6.3	1.5	8.0	ns		
t _{dis}	disable time	nOE to nY; see Figure 7 ^[2]								
		V _{CC} = 1.2 V	-	8.0	-	-	-	ns		
		V _{CC} = 1.65 V to 1.95 V	1.0	3.3	10.0	1.0	11.5	ns		
		V _{CC} = 2.3 V to 2.7 V	0.5	1.8	5.6	0.5	6.5	ns		
		V _{CC} = 2.7 V	1.5	3.4	6.7	1.5	8.5	ns		
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V ^[3]	-	-	1.0	-	1.5	ns		
		C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ^[4]						
				V _{CC} = 1.65 V to 1.95 V	-	6.0	-	-	-	pF
				V _{CC} = 2.3 V to 2.7 V	-	9.3	-	-	-	pF
				V _{CC} = 3.0 V to 3.6 V	-	12.2	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

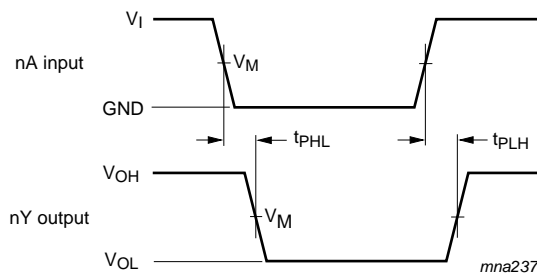
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. AC waveforms

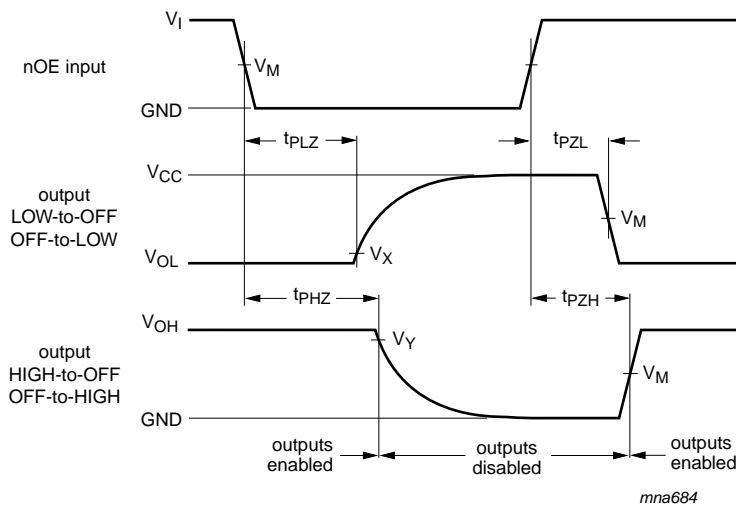


$V_M = 1.5 V$ at $V_{CC} \geq 2.7 V$;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 V$;

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The input nA to output nY propagation delays



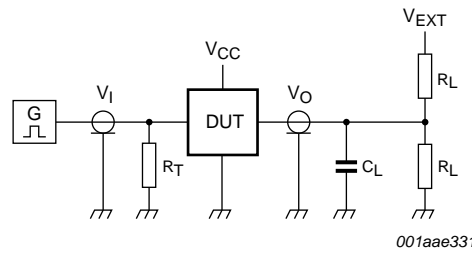
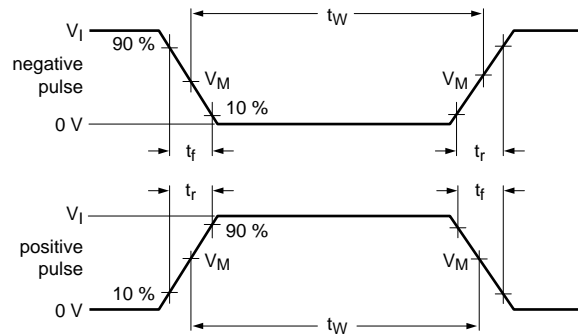
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V _{CC}	V _M	V _M	V _X	V _Y
V _{CC} < 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
V _{CC} ≥ 2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

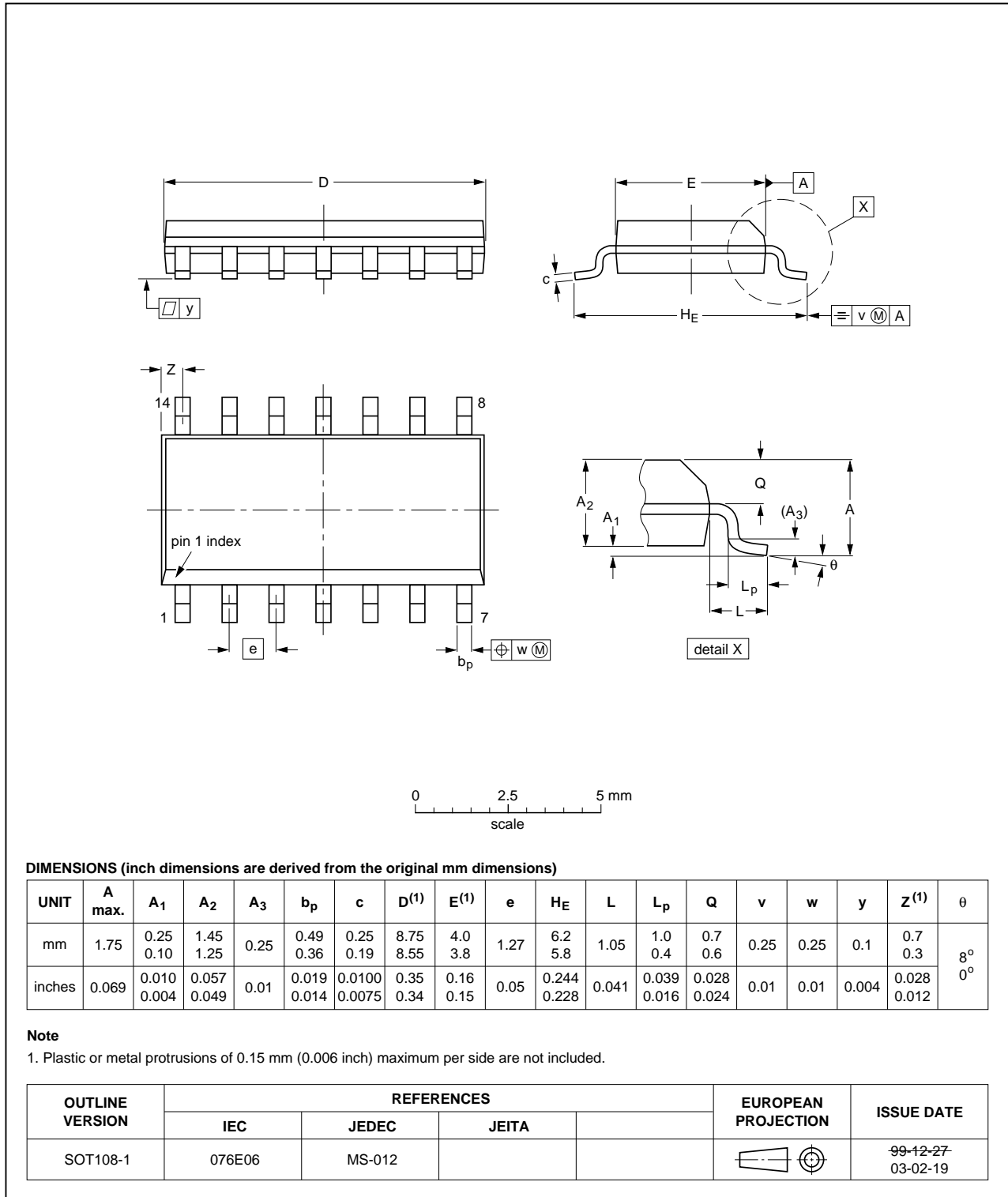


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

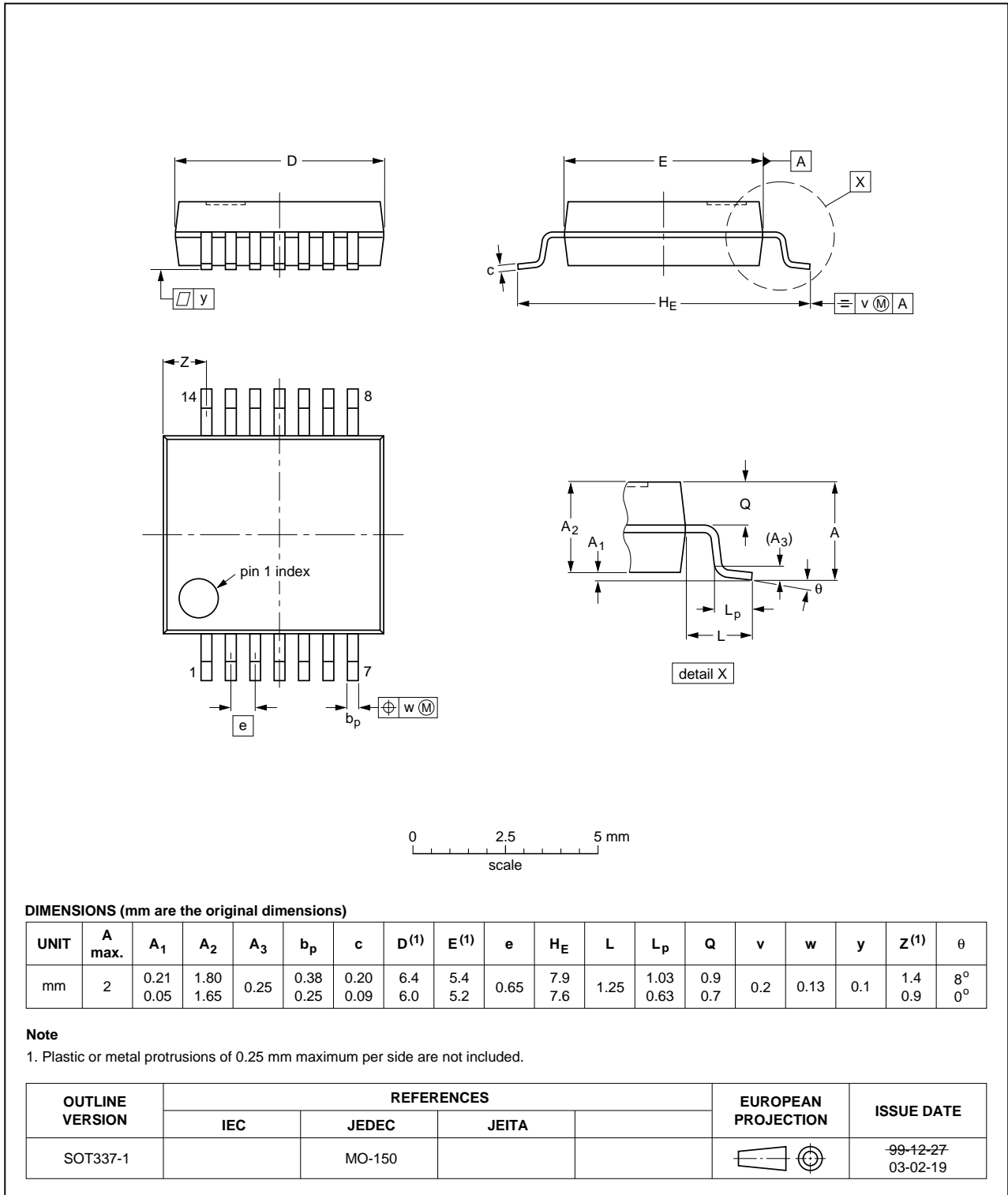


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

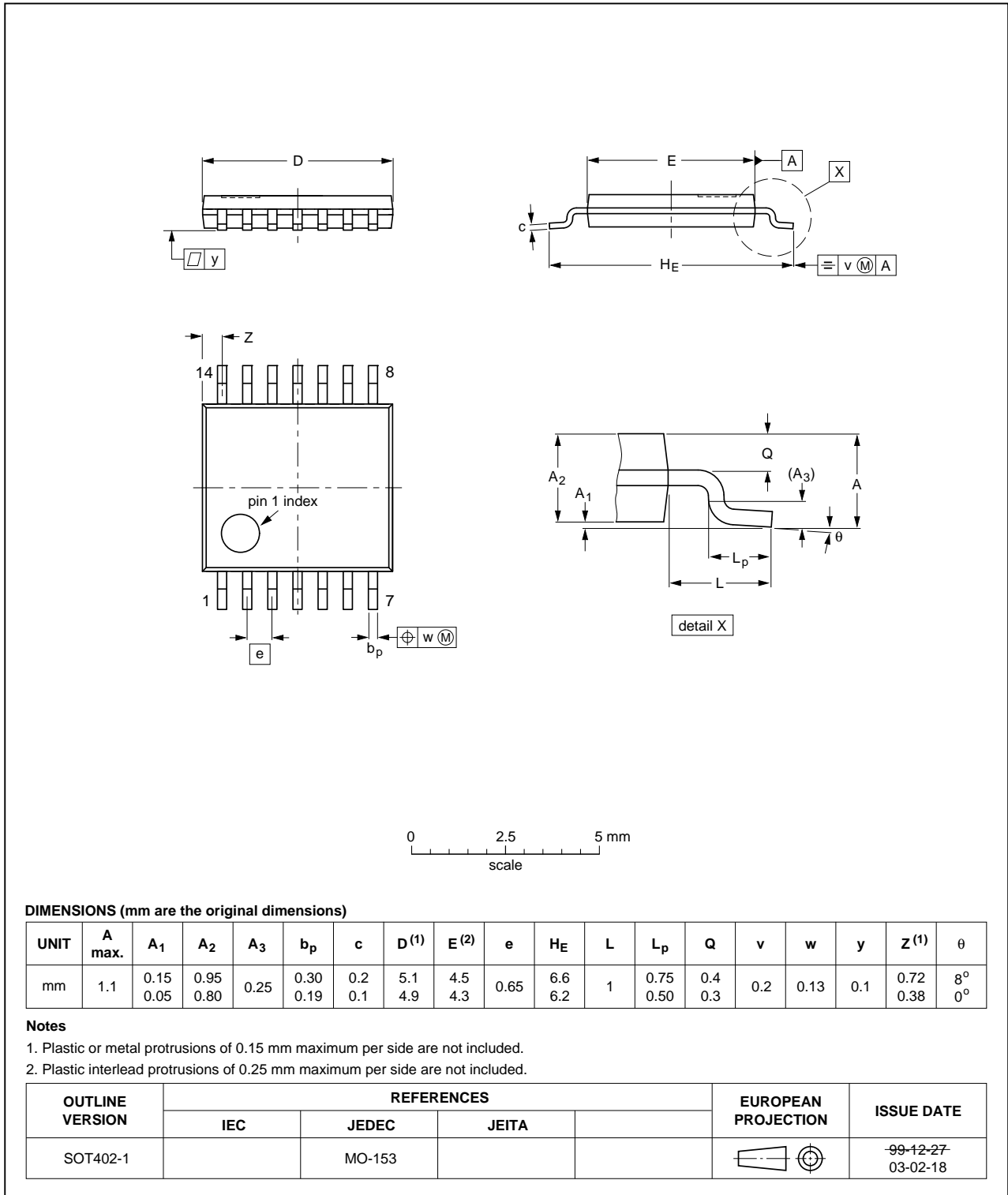


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

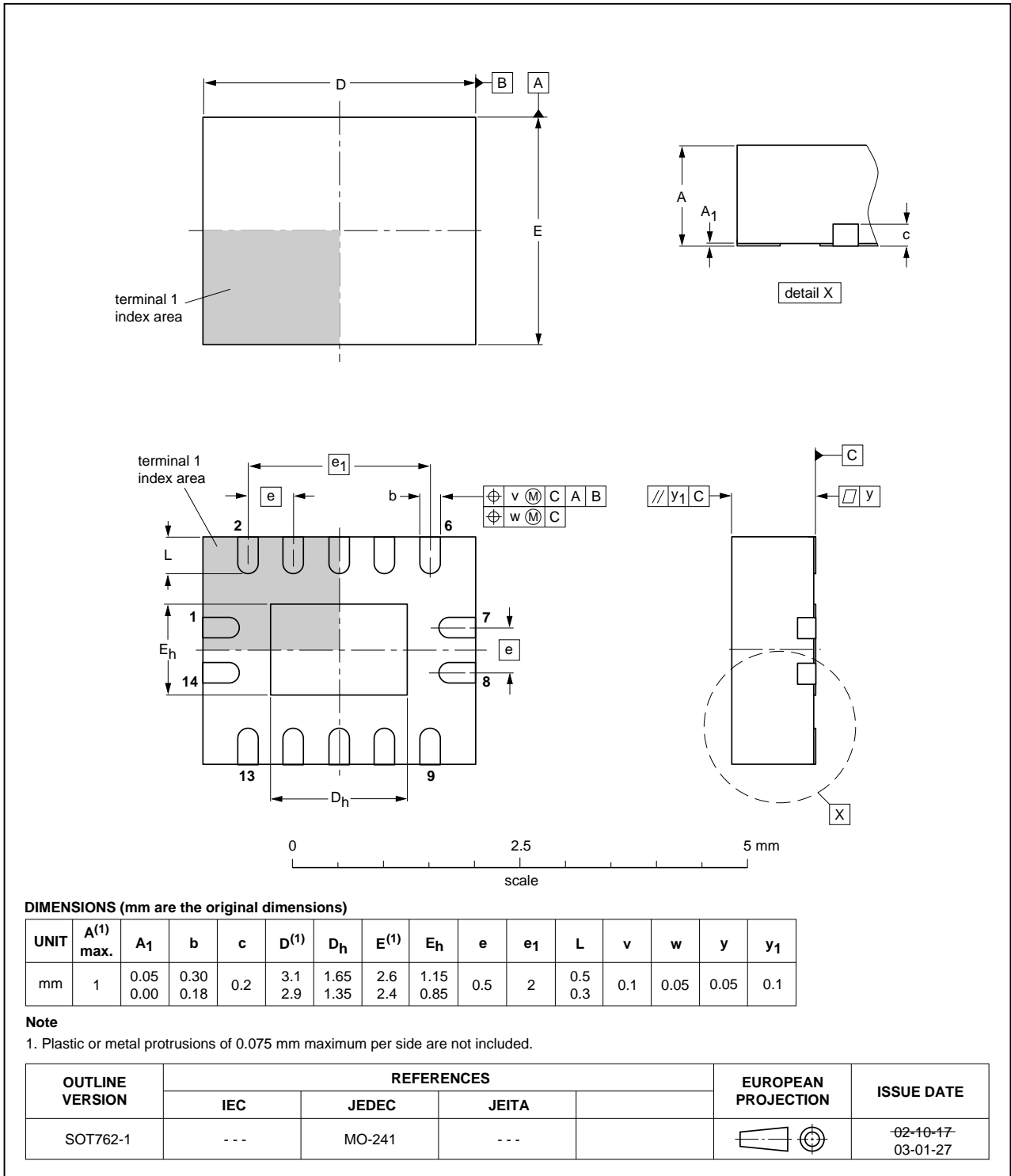


Fig 12. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC126A v.7	20111209	Product data sheet	-	74LVC126A v.6
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC126A v.6	20110926	Product data sheet	-	74LVC126A v.5
74LVC126A v.5	20030228	Product specification	-	74LVC126A v.4
74LVC126A v.4	20020308	Product specification	-	74LVC126A v.3
74LVC126A v.3	19980428	Product specification	-	74LVC126A v.2
74LVC126A v.2	19970801	Product specification	-	74LVC126A v.1
74LVC126A v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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