HARRIS SEMICONDUCTOR

CDP1852/3, CDP1852C/3

March 1997

High-Reliability Byte-Wide Input/Output Port

Features

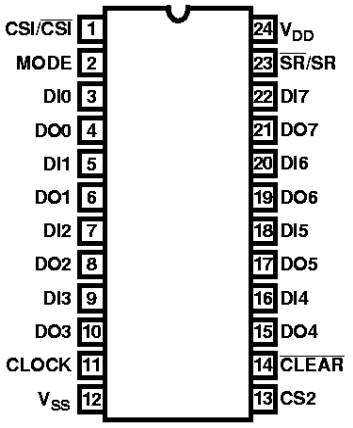
- Static Silicon-Gate CMOS Circuitry
- Parallel 8-Bit Data Register and Buffer
- Handshaking Via Service Request Flip-Flop
- Low Quiescent and Operating Power
- Interfaces Directly with CDP1800-Series Microprocessors
- Single Voltage Supply
- Full Military Temperature Range (-55°C to +125°C)

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO
SBDIP	-55°C to +125°C	CDP1852CD3	CDP1852D3	D24.6

Pinout

CDP1852/3, CDP1852C/3 (SBDIP)
TOP VIEW



Description

The CDP1852/3 and CDP1852C/3 are parallel, 8-bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800-Series microprocessors. They are also useful as 8-bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

The mode control is used to program the device as an input port (mode = 0) or as an output port (mode = 1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852/3, and microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852/3, and handshaking is established with a peripheral device when the CDP1852/3 is deselected.

In the input mode, data at the data-in terminals (DI0-DI7) is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low (SR/$\overline{SR}$ = 0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2 = 1), the three-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (DO0-DO7). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2 = 0), the data-out terminals are tristated and the service request output returns high ($\overline{SR}$/SR =1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (DI0-DI7) is strobed into the 8-bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$ = 0) and CS2 and the clock are high (1), and are present at the data-out terminals (DO0-DO7). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR = 1) when the device is deselected (CS1/$\overline{CS1}$ = 1 or CS2 = 0) and returns low ($\overline{SR}$/SR = 0) on the following trailing edge of the clock.

A $\overline{CLEAR}$ control is provided for resetting the port's register (DO0-DO7 = 0) and service request flip-flop (input mode: $\overline{SR}$/SR = 1 and output mode: $\overline{SR}$/SR = 0).

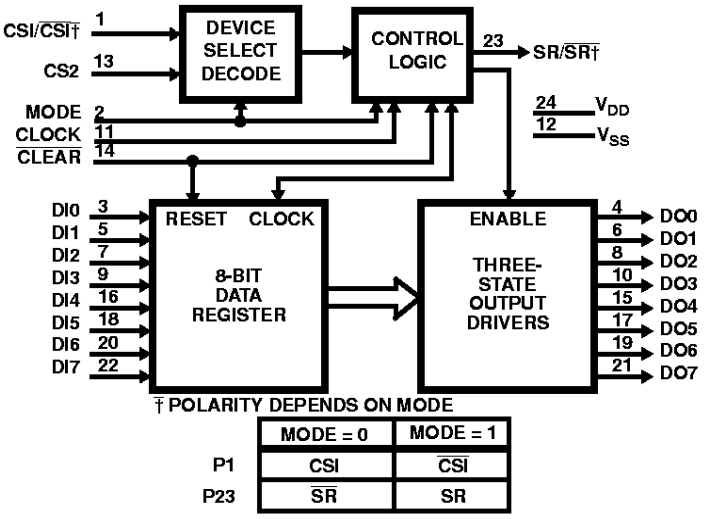
The CDP1852/3 is functionally identical to the CDP1852C/3. The CDP1852/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1852C/3 has a recommended operating voltage range of 4V to 6.5V.

The CDP1852/3 and CDP1852C/3 are supplied in 24-lead, dual-in-line side-brazed ceramic packages (D suffix).

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1694.2**

Block Diagram of CDP1852/3



† POLARITY DEPENDS ON MODE

	MODE = 0	MODE = 1
P1	CSI	$\overline{CSI}$
P23	$\overline{SR}$	SR

FIGURE 1.

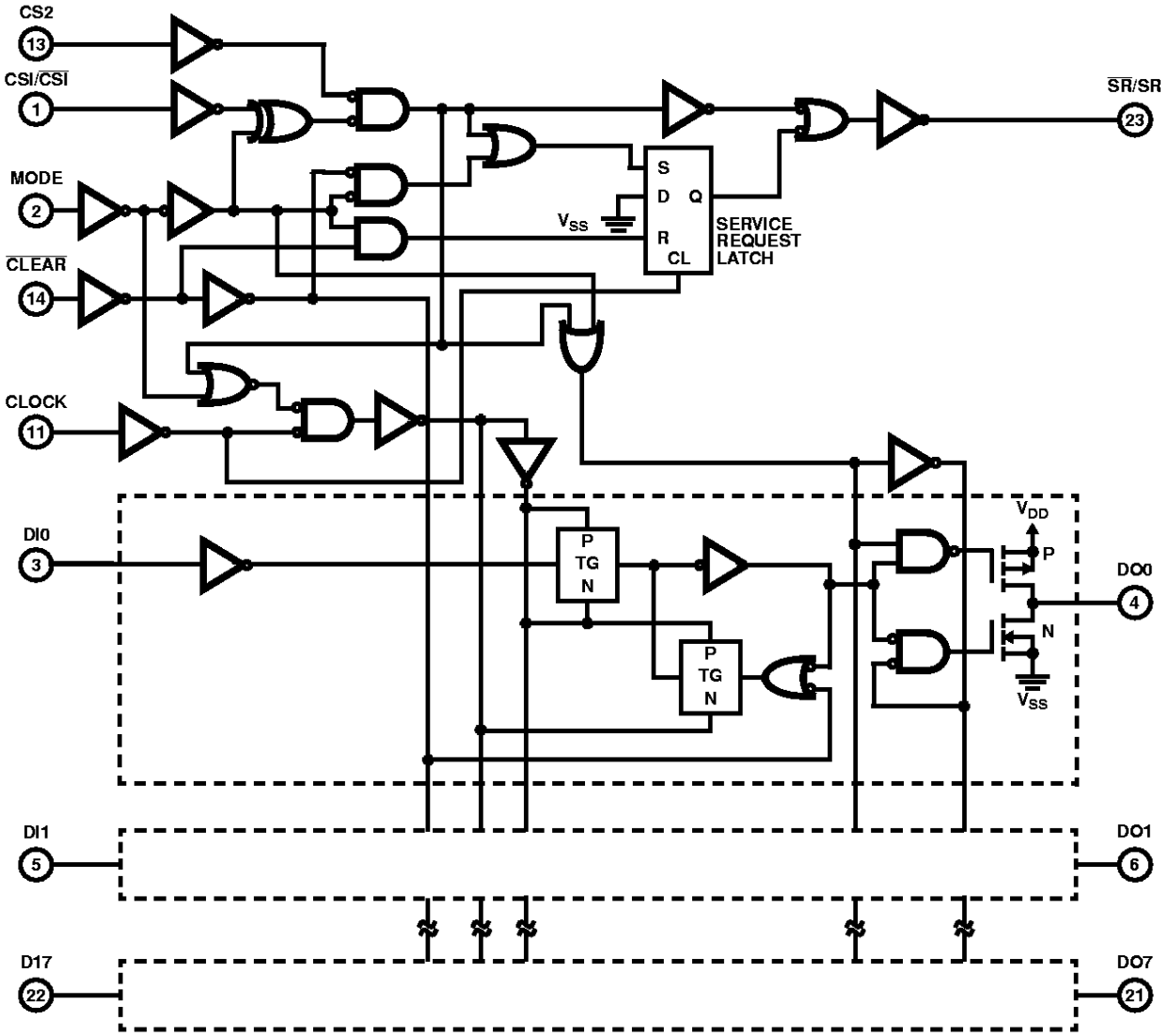


FIGURE 2. CDP1852/3 LOGIC DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}):
(All Voltages Referenced to V_{SS} Terminal)
CDP1852/3 . . . . . -0.5V to +11V
CDP1852C/3 . . . . . -0.5V to +7V
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, any One Input . . . . . ±10mA

Thermal Information

	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Thermal Resistance (Typical)		
SBDIP Package	65	20

Device Dissipation Per Output Transistor
T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D . . . . . -55°C to +125°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 in (1.59 ± 0.79mm)
From Case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

T_A = Full-Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges.

PARAMETER	LIMITS				UNITS
	CPP1852/3		CDP1852C/3		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Static Electrical Specifications

V_{IN} = 0 or V_{DD}, Except as Noted

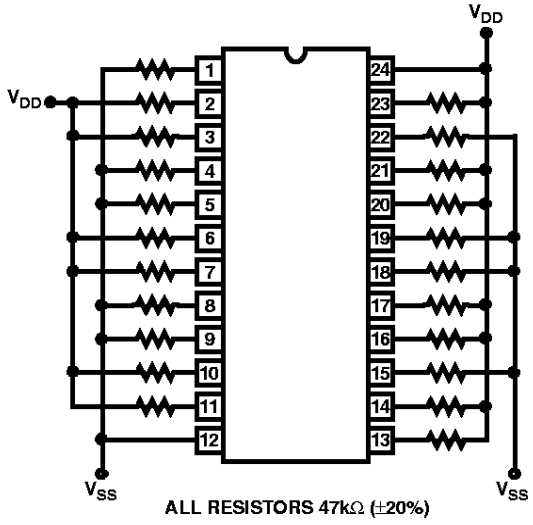
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	I_{DD}	V_{DD} = 5V	-	10	-	100	µA
		V_{DD} = 10V	-	20	-	300	µA
Output Low Drive (Sink) Current	I_{OL}	V_{DD} = 5V, V_O = 0.4V	2.6	-	1.9	-	mA
		V_{DD} = 10V, V_O = 0.5V	6.1	-	4.1	-	mA
Output High Drive (Source) Current	I_{OH}	V_{DD} = 5V, V_O = 4.6V	-1.8	-	-1.3	-	mA
		V_{DD} = 10V, V_O = 9.5V	-4.4	-	-2.9	-	mA
Output Voltage Low Level	V_{OL}	V_{DD} = 5V, I_{OL} = 0µA	-	0.1	-	0.2	V
		V_{DD} = 10V, I_{OL} = 0µA	-	0.1	-	0.2	V
Output Voltage High Level	V_{OH}	V_{DD} = 5V, I_{OL} = 0µA	4.9	-	4.8	-	V
		V_{DD} = 10V, I_{OL} = 0µA	9.9	-	9.8	-	V
Input Low Voltage	V_{IL}	V_{DD} = 5V, V_O = 0.2, 4.8V	-	1.5	-	1.5	V
		V_{DD} = 10V, V_O = 0.2, 9.8V	-	3	-	3	V
Input High Voltage	V_{IH}	V_{DD} = 5V, V_O = 0.2, 4.8V	3.5	-	3.5	-	V
		V_{DD} = 10V, V_O = 0.2, 9.8V	7	-	7	-	V
Input Leakage Low	I_{IL}	V_{DD} = 5V, V_{IN} = 0V	-	-1	-	-5	µA
		V_{DD} = 10V, V_{IN} = 0V	-	-1	-	-5	µA
Input Leakage High	I_{IH}	V_{DD} = 5V, V_{IN} = 5V	-	1	-	5	µA
		V_{DD} = 10V, V_{IN} = 10V	-	1	-	5	µA

Static Electrical Specifications V_{IN} = 0 or V_{DD}, Except as Noted (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS -55°C, +25°C MIN	LIMITS -55°C, +25°C MAX	LIMITS +125°C MIN	LIMITS +125°C MAX	UNITS
Three-State Output Leakage Low	I_{OZL}	V_{DD} = 5V, V_O = 0V	-	-1	-	-5	µA
		V_{DD} = 10V, V_O = 0V	-	-1	-	-5	µA
Three-State Output Leakage High	I_{OZH}	V_{DD} = 5V, V_O = 5V	-	1	-	5	µA
		V_{DD} = 10V, V_O = 10V	-	1	-	5	µA
Input Capacitance	C_{IN}	Note 2	-	10	-	10	pF
Output Capacitance	C_{OUT}	Note 2	-	15	-	15	pF

NOTES:
1. The CDP1852C/3 meets all 5V static electrical specifications of the CDP1852/3 except +125°C quiescent device current for which the limit is I_{DD} = 300µA.
2. Input and output capacitance are guaranteed but not tested.

Static Burn-In Circuit



TYPE NO.	V_{DD}	TEMPERATURE	TIME
CDP1852/3	11V	+125°C	160 Hrs. Min.
CDP1852C/3	7V	+125°C	160 Hrs. Min.

Dynamic Electrical Specifications Mode = 0 Input Port, See Figure 3, Input t_r, $t_f \leq$ 15ns; C_L = 50pF

PARAMETER	SYMBOL	V_{DD} VOLTS	LIMITS (NOTE 1) -55°C, +25°C (NOTE 1) MIN	LIMITS (NOTE 1) -55°C, +25°C MAX	LIMITS (NOTE 1) +125°C (NOTE 1) MIN	LIMITS (NOTE 1) +125°C MAX	UNITS
Select Duration	t_{SW}	5	250	-	360	-	ns
		10	150	-	180	-	ns
Clock Pulse Width	t_{WW}	5	150	-	200	-	ns
		10	90	-	110	-	ns
Clear Pulse Width	t_{CLR}	5	110	-	160	-	ns
		10	50	-	80	-	ns
Data-In to Clock Fall Setup Time	t_{DS}	5	-10	-	-10	-	ns
		10	-5	-	-5	-	ns

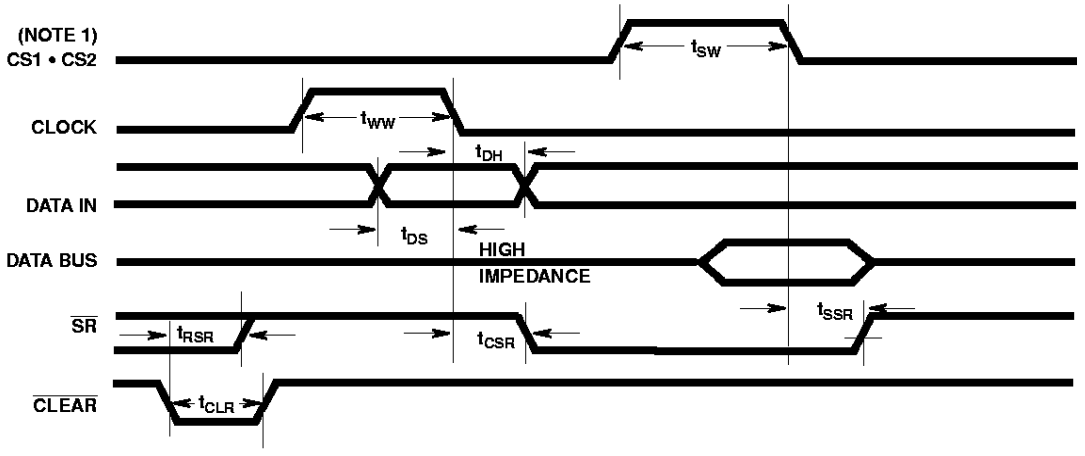
Dynamic Electrical Specifications

Mode = 0 Input Port, See Figure 3, Input t_r, $t_f \leq 15ns$; $C_L = 50pF$ **(Continued)**

PARAMETER	SYMBOL	V_{DD} VOLTS	LIMITS (NOTE 1) -55°C, +25°C (NOTE 1) MIN	-55°C, +25°C MAX	+125°C (NOTE 1) MIN	+125°C MAX	UNITS
Data-In After Clock Fall Hold Time	t_{DH}	5	150	-	170	-	ns
		10	70	-	100	-	ns
Propagation Delay Times: Clear to $\overline{SR}$	t_{RSR}	5	-	200	-	340	ns
		10	-	110	-	170	ns
Clock to $\overline{SR}$	t_{CSR}	5	-	175	-	220	ns
		10	-	110	-	130	ns
Deselect to $\overline{SR}$	t_{SSR}	5	-	175	-	240	ns
		10	-	110	-	120	ns

NOTE:

1. Time required by a device to allow for the indicated function.



NOTE:

1. CS1 • CS2 is the overlap of CS1 = 1 and CS2 = 1.

MODE = 0 TRUTH TABLE			
CLOCK	CS1 • CS2 (Note 1)	$\overline{CLEAR}$	DATA OUT EQUALS
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

SERVICE REQUEST TRUTH TABLE	
Clock = ↘	CS1 or CS2 = ↘ or $\overline{CLEAR}$ = 0
$\overline{SR}$ = 0	$\overline{SR}$ = 1

NOTE:

1. CS1 • CS2 = CS1 = 1, CS2 = 1.

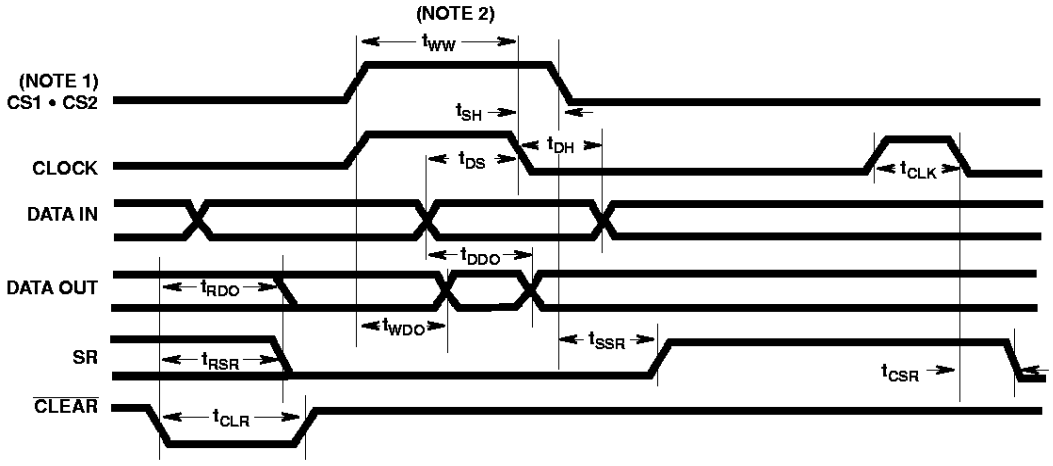
FIGURE 3. MODE = 0 INPUT PORT TIMING WAVEFORMS AND TRUTH TABLES

Dynamic Electrical Specification Mode = 1 Output Port, See Figure 4, Input tr, tf ≤ 15ns; C_L = 50pF

PARAMETER	SYMBOL	V_{DD} VOLTS	LIMITS (NOTE 1) -55°C, +25°C (NOTE 1) MIN	-55°C, +25°C MAX	+125°C (NOTE 1) MIN	+125°C MAX	UNITS
Clock Pulse Width	t_{CLK}	5	170	-	260	-	ns
		10	90	-	130	-	ns
Write Width Duration	t_{WW}	5	200	-	260	-	ns
		10	110	-	130	-	ns
Clear Pulse Width	t_{CLR}	5	110	-	135	-	ns
		10	60	-	75	-	ns
Data-In to Clock Fall Setup Time	t_{DS}	5	-10	-	-10	-	ns
		10	-5	-	-5	-	ns
Data Hold from Write Termination	t_{DH}	5	130	-	170	-	ns
		10	70	-	90	-	ns
Select-After Clock-Fall Hold Time	t_{SH}	5	0	-	0	-	ns
		10	0	-	0	-	ns
Propagation Delay Times: Clear to Data	t_{RDO}	5	-	215	-	290	ns
		10	-	140	-	190	ns
Write to Data Out	t_{WDO}	5	-	250	-	350	ns
		10	-	130	-	190	ns
Data In to Data Out	t_{DDO}	5	-	150	-	200	ns
		10	-	80	-	100	ns
Clear to SR	t_{RSR}	5	-	175	-	240	ns
		10	-	120	-	160	ns
Clock to SR	t_{CSR}	5	-	170	-	240	ns
		10	-	90	-	120	ns
Deselect to SR	t_{SSR}	5	-	170	-	240	ns
		10	-	90	-	120	ns

NOTE:

1. Time required by a device to allow for the indicated function.



NOTES:

1. CS1 • CS2 is the overlap of the $\overline{CS1}$ = 0 and CS2 = 1.
2. Write is the overlap of CS1 • CS2 and clock.

MODE = 1 TRUTH TABLE			
CLOCK	$\overline{CS1}$ • CS2 (NOTE 1)	$\overline{CLEAR}$	DATA OUT EQUALS
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

SERVICE REQUEST TRUTH TABLE	
$\overline{CS1}$ ↗ or CS2 ↘	Clock • ($\overline{CS1}$ • $\overline{CS2}$) ↘ or $\overline{CLEAR}$ = 0
SR = 1	SR = 0

NOTE:

1. $\overline{CS1}$ • CS2 = $\overline{CS1}$ = 0, CS2 = 1

FIGURE 4. MODE = 1 OUTPUT PORT TIMING WAVEFORMS AND TRUTH TABLES