

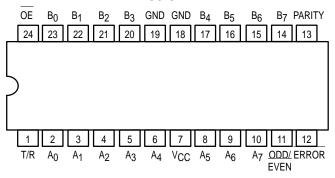
OCTAL BIDIRECTIONAL TRANSCEIVER WITH 8-BIT PARITY **GENERATOR CHECKER** (3-STATE OUTPUTS)

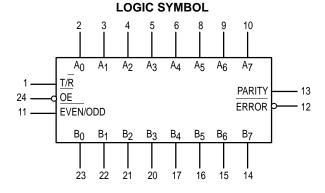
The MC74F657A and MC74F657B are Octal Bidirectional Transceivers with an 8-bit parity Generator/Checker and 3-state outputs.

The A and B options are faster versions of the F657 and contain eight noninverting buffers with 3-state outputs and an 8-bit parity generator/checker. These devices are intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A ports and 64 mA at the B ports. The Transmit/Receiver (T/R) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

- High-Impedance NPN Base Input for Reduced Loading (20 μA in HIGH and LOW States)
- Ideal in Applications Where High Output Drive and Light Bus Loading are Required (III is 20 μA versus Fast std of 600 μA)
- Combines F245 and F280A Functions in One Package
- 3-State Outputs
- B Outputs, PARITY, ERROR, Sink 64 mA and Source 15 mA
- 15 mA Source Current
- Input Diodes for Termination Effects
- Glitchless Outputs During Power Up and Power Down
- High Impedance Outputs During Power Off
- ESD Protection > 4000 Volts

PIN ASSIGNMENT

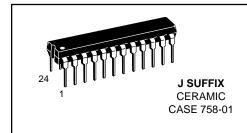




MC74F657A,B

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 8-BIT PARITY **GENERATOR CHECKER** (3-STATE OUTPUTS)

FAST™ SCHOTTKY TTL







DW SUFFIX SOIC CASE 751E-03

ORDERING INFORMATION

MC74FXXXAJ/BJ Ceramic MC74FXXXAN/BN Plastic MC74FXXXADW/BDW SOIC

MC74F657A, B

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Тур	Max	Unit	
Vcc	Supply Voltage		4.5	5.0	5.5	V
TA	Operating Ambient Temperature Range	74	0	25	70	°C
loн	Output Current — High				-3.0/-15	mA
lOL	Output Current — Low	74			24/64	mA

FUNCTION TABLE

	Number of Inputs That are High	Inputs			Input/Output	Outputs		
Γ		OE	T/R	Even/Odd	Parity	Error	Outputs Mode	
-		L	Н	Н	Н	Z	Transmit	
ı		L	Н	L	L	Z	Transmit	
N		L	L	Н	Н	Н	Receive	
1	0, 2, 4, 6, 8	L	L	Н	L	L	Receive	
ı.		L	L	L	Н	L	Receive	
		L	L	L	L	Н	Receive	

	Number of Inputs That are High		In	puts	Input/Output	Outputs		
		OE	T/R	Even/Odd	Parity	Error	Outputs Mode	
		L	Н	Н	L	Z	Transmit	
		L	Н	L	Н	Z	Transmit	
_		L	L	Н	Н	L	Receive	
7	1, 3, 5, 7	L	L	Н	L	Н	Receive	
П		L	L	L	Н	Н	Receive	
		L	L	L	L	L	Receive	
Ī	Don't Care	Н	Х	Х	Z	Z	Z	

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = HIGH impedance state.

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MC74F657A, B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

		Limits								
Symbol	Parameter			Min	Тур	Max	Unit	Test Conditions		
V _{IH}	Input HIGH Voltage			2.0			V	Guaranteed Inpu	ıt HIGH Voltage	
V _{IL}	Input LOW Voltage					0.8	V	Guaranteed Input LOW Voltage		
VIK	Input Clamp Diode Voltage				-0.73	-1.2	V	V _{CC} = MIN, I _{IN}	= –18 mA	
		All Outputs	74	2.4			V	1 2.0 mA	V _{CC} = 4.5 V	
VOH				2.7	3.4		V	$I_{OH} = -3.0 \text{ mA}$	V _{CC} = 4.75 V	
	Output HIGH Voltage	B0-B7 <u>PARITY,</u> ERROR	74	2.0			V	I _{OH} = -15 mA	V _{CC} = 4.5 V	
		A0-A7	74		0.35	0.5	V	I _{OL} = 24 mA		
VOL	Output LOW Voltage	B0-B7 PARITY, ERROR	74		0.4	0.55	V	I _{OL} = 64 mA	V _{CC} = MIN	
^I ін		T/R, OE, EVE	N/ODD			100	μΑ	V _{CC} = 0 V, V _{IN} :	= 7.0 V	
	Input HIGH Current	A0-A7				2.0	^	V _{CC} = 5.5 V, V _{IN} = 5.5 V		
		B0-B7, PARITY				1.0	mA	V _C C = 5.5 V, V _I	_V = 5.5 V	
		EVEN/ODD				20	μΑ	V _{CC} = MAX, V _{IN} = 2.7 V		
		T/R, OE				40		VUC - IVIAA, VIIN - 2.7 V		
l	Input LOW Current	EVEN/ODD				-20	μΑ	V _{CC} = MAX, V _{IN} = 0.5 V		
lIL		T/R, OE				-40	μΑ	VCC = IVIAAA, VIN = 0.5 V		
I _{IH} + ^I OZH	Off-State Current HIGH Level Voltage Applied	A0–A7 B0–B7				70	μΑ	V _{CC} = MAX, V _{OUT} = 2.7 V		
I _{IL} +IOZL	Off-State Current LOW Level Voltage Applied	PARITY				-70	μΛ	$V_{CC} = MAX, V_{C}$	_{UT} = 0.5 V	
lozh	Off-State Output Current, High-Level Voltage Applied		_			50	μΑ	$V_{CC} = MAX, V_{OUT} = 2.7 V$ $V_{CC} = MAX, V_{OUT} = 0.5 V$		
lozL	Off-State Output Current, Low-Level Voltage Applied	ERROF	₹			-50	μΛ			
	Output Short Circuit	A _n Outputs PARIT <u>Y, B_n O</u> utputs, ERROR		-60		-150				
los	Current (Note 2)			-100		-225	mA $V_{CC} = MAX, V_{C}$		OUT = 0 V	
		ICCH			90	135				
ICC	Total Supply Current	ICCL ICCZ			106	150	mA	$V_{CC} = MAX$	CC = MAX	
					98	145				

NOTES:

^{1.} For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.

^{2.} Not more than one output should be shorted at one time, nor for more than 1 second.

MC74F657A, B

F657A AC ELECTRICAL CHARACTERISTICS

			74F		74		
		v	T _A = +25°C CC = +5.0 C _L = 50 pF	v V	T _A = 0°C V _{CC} = +5. C _L =		
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit
tPLH tPHL	Propagation Delay A _n to B _n or B _n to A _n	2.0 2.0		7.0 7.0	2.0 2.0	7.5 7.5	ns
tPLH tPHL	Propagation Delay A _n to PARITY	6.0 6.5		13 13	5.5 6.5	14 14	ns
^t PLH ^t PHL	Propagation Delay EVEN /ODD to PARITY, ERROR	4.5 4.5		10.5 10.5	4.5 4.5	11 11.5	ns
t _{PLH}	Propagation Delay B _n to ERROR	7.0 7.0		18 18	6.5 6.5	19 19	ns
^t PLH ^t PHL	Propagation <u>Delay</u> PARITY to ERROR	8.0 7.0		14 14	7.0 7.0	15 15	ns
tPZH tPZL	Output Enable Time to HIGH or LOW Level	3.0 4.0		8.0 9.0	3.0 4.0	9.0 10	ns
^t PHZ ^t PLZ	Output Disable Time from HIGH or LOW Level	2.0 2.0		7.5 6.0	2.0 2.0	8.0 6.5	ns

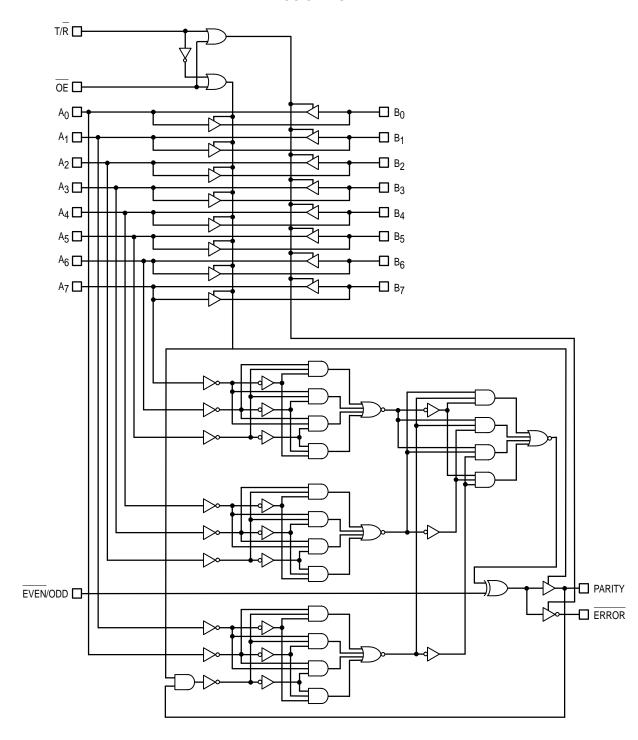
F657B AC ELECTRICAL CHARACTERISTICS

				74F		74	ŀF		1
Ī			v	T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C V _{CC} = +5. C _L =			
	Symbol	Parameter	Min	Тур	Max	Min	Max	Unit	l
	tPLH tPHL	Propagation Delay A _n to B _n or B _n to A _n	2.0 2.0		6.0 6.0	2.0 2.0	6.5 6.5	ns	l
J	tPLH tPHL	Propagation Delay A _n to PARITY	4.5 4.5		11.5 11.5	4.5 4.5	13 13	ns	1
	tPLH tPHL	Propagation Delay EVEN/ODD to PARITY, ERROR	2.0 2.0		7.5 7.5	2.0 2.0	8.5 8.5	ns	
	^t PLH ^t PHL	Propagation <u>D</u> elay B _n to ERROR	4.0 4.0		15 15	3.5 3.5	16 16	ns	
	^t PLH ^t PHL	Propagation Delay PARITY to ERROR	5.0 5.0		11 11	4.0 4.0	12 12	ns	
	^t PZH ^t PZL	Output Enable Time to HIGH or LOW Level	2.0 2.0		7.0 7.0	2.0 2.0	8.0 8.0	ns	Ì
	^t PHZ ^t PLZ	Output Disable Time from HIGH or LOW Level	2.0 2.0		6.0 6.0	2.0 2.0	6.5 6.5	ns	Ì

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LOGIC DIAGRAM



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