

# FDR8702H

## 20V N & P-Channel PowerTrench® MOSFET

### General Description

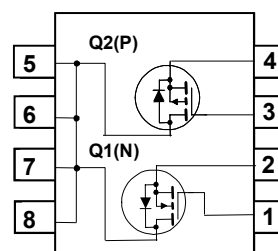
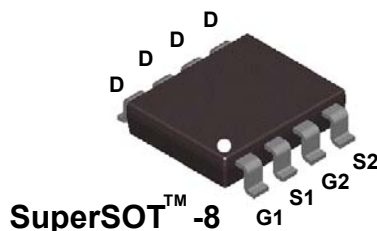
These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

### Applications

DC/DC converter  
Power management

### Features

- N channel  $R_{DS(ON)} = 38\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$   
3.6 A, 20V  $R_{DS(ON)} = 54\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- P channel  $R_{DS(ON)} = 80\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$   
-2.6 A, -20V  $R_{DS(ON)} = 110\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- Fast switching speed.
- High performance trench technology for extremely low  $R_{DS(ON)}$



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings		Units
		Q1 (N)	Q2 (P)	
V <sub>DSS</sub>	Drain-Source Voltage	20	-20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	±8	V
I <sub>D</sub>	Drain Current— Continuous (Note 1a) — Pulsed	3.6	-2.6	A
		15	-10	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a)	0.8		W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	146	°C/W
		76	
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	40	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.8702	FDR8702H	13"	12mm	2500 units

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

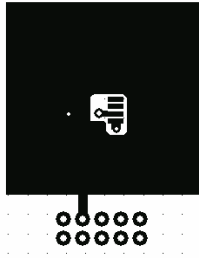
Symbol	Parameter	Test Conditions	Q	Min	Typ	Max	Units
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 Q2	20 -20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{Ref to } 25^\circ\text{C}$ $I_D = -250\ \mu\text{A}, \text{Ref to } 25^\circ\text{C}$	Q1 Q2		36 -15		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA
<b>On Characteristics</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	Q1 Q2	0.6 -0.4	0.8 -0.7	1.5 -1.6	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{Ref to } 25^\circ\text{C}$ $I_D = -250\ \mu\text{A}, \text{Ref to } 25^\circ\text{C}$	Q1 Q2		-2 2.5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 3.1\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 3.6\text{ A}, T_J = 125^\circ\text{C}$	Q1		31 42 41	38 54 58	m $\Omega$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -2.6\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.2\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -2.6\text{ A}, T_J = 125^\circ\text{C}$	Q2		66 85 83	80 110 108	m $\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	Q1 Q2	10 -10			A
$g_{FS}$	Forward Transconductance	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	Q1 Q2		15 9		S
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	Q1 Q2		1 4.8		$\Omega$
<b>Dynamic Characteristics</b>							
$C_{iss}$	Input Capacitance	For Q1: $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		650 607		pF
$C_{oss}$	Output Capacitance		Q1 Q2		170 165		pF
$C_{riss}$	Reverse Transfer Capacitance	For Q2: $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		80 60		pF
<b>Switching Characteristics</b> (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	For Q1: $V_{DS} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		8 12	16 22	ns
$t_r$	Turn-On Rise Time		Q1 Q2		9 11	18 20	ns
$t_{d(off)}$	Turn-Off Delay Time	For Q2: $V_{DS} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		16 26	29 42	ns
$t_f$	Turn-Off Fall Time		Q1 Q2		7 8	14 16	ns
$Q_g$	Total Gate Charge	For Q1: $V_{DS} = 10\text{ V}, I_D = 3.6\text{ A},$ $V_{GS} = 4.5\text{ V}$	Q1 Q2		7 6	10 8	nC
$Q_{gs}$	Gate-Source Charge		Q1 Q2		1.3 1.2		nC
$Q_{gd}$	Gate-Drain Charge	For Q2: $V_{DS} = -10\text{ V}, I_D = -2.6\text{ A},$ $V_{GS} = -4.5\text{ V}$	Q1 Q2		2.2 1.6		nC

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

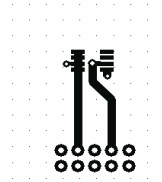
Symbol	Parameter	Test Conditions	Q	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			0.7 -0.7	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 0.7\text{ A}$ , Note 2 $V_{GS} = 0\text{ V}$ , $I_S = -0.7\text{ A}$ , Note 2	Q1 Q2		0.7 -0.7	1.2 -1.2	V
$t_{rr}$	Reverse Recovery Time	For Q1: $I_F = 3.6\text{ A}$ , $dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		16 22		ns
$I_{rm}$	Maximum Reverse Recovery Current		Q1 Q2		0.6 0.7		A
$Q_{rr}$	Reverse Recovery Charge	For Q2: $I_F = -2.6\text{ A}$ , $dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		5 8		nC

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $76^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



- b)  $146^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics : Q1

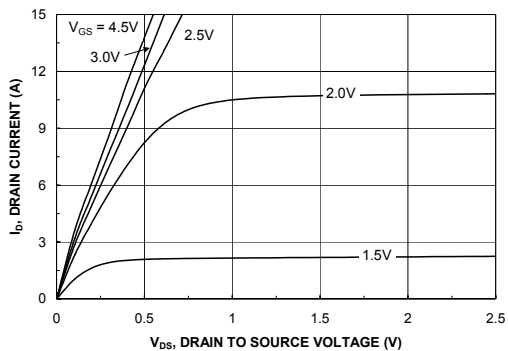


Figure 1. On-Region Characteristics.

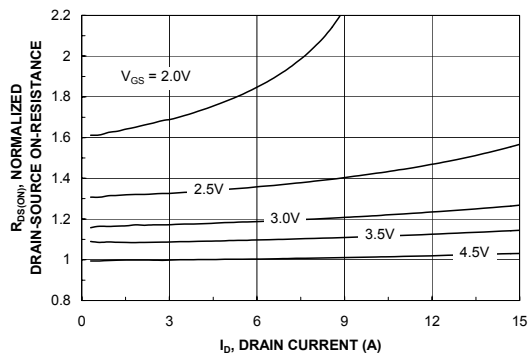


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

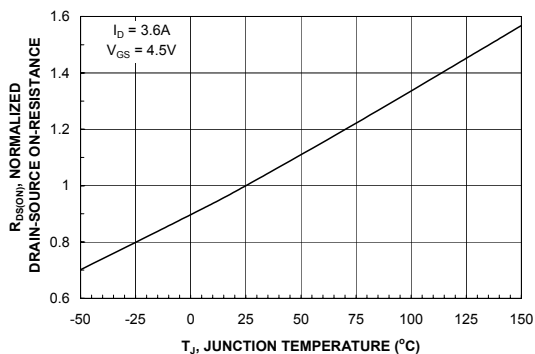


Figure 3. On-Resistance Variation with Temperature.

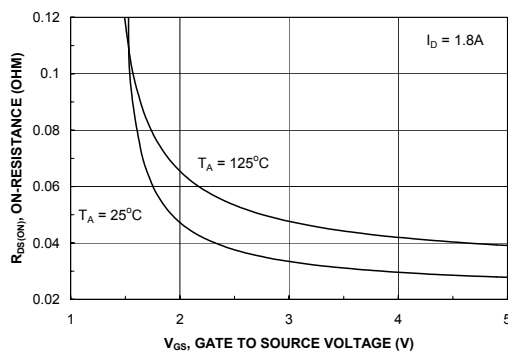


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

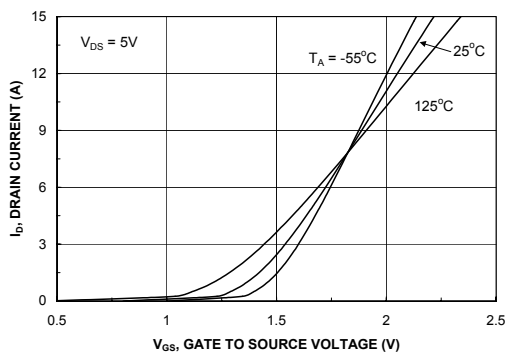


Figure 5. Transfer Characteristics.

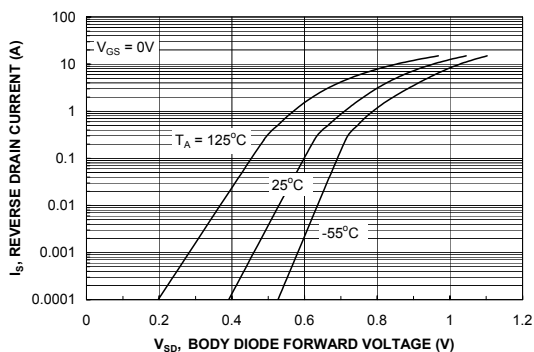


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics : Q1

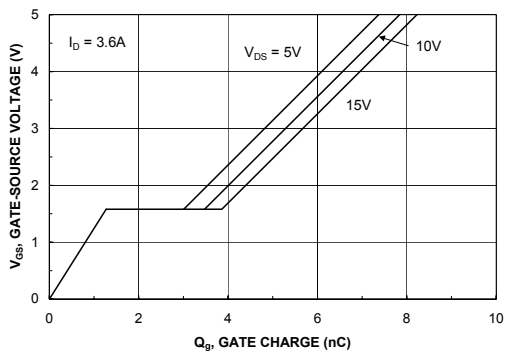


Figure 7. Gate Charge Characteristics.

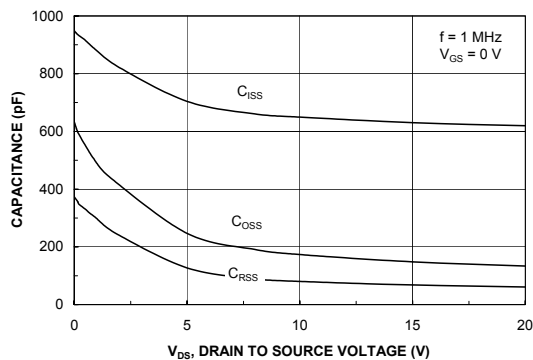


Figure 8. Capacitance Characteristics.

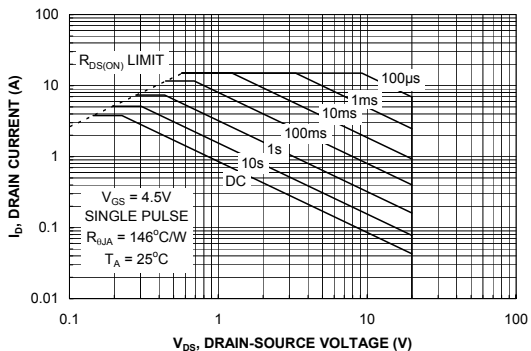


Figure 9. Maximum Safe Operating Area.

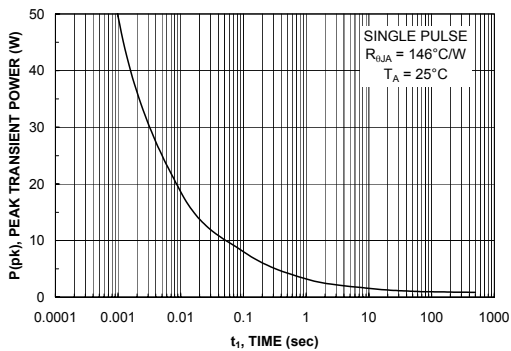


Figure 10. Single Pulse Maximum Power Dissipation.

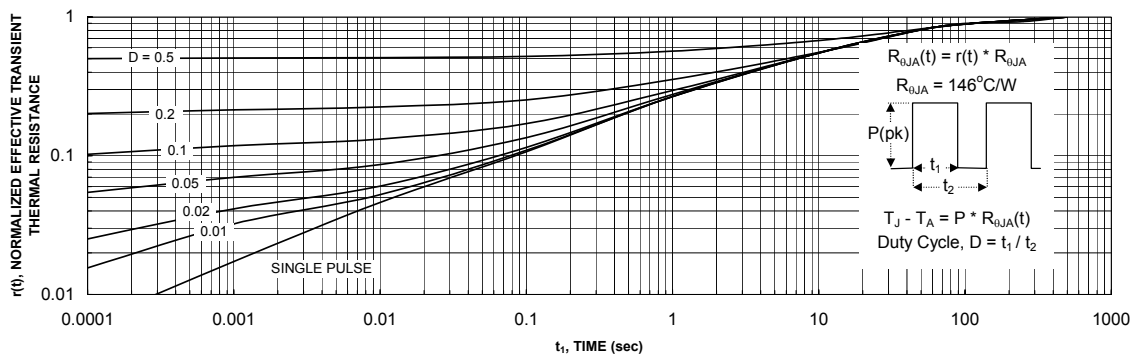


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.

Typical Characteristics : Q2

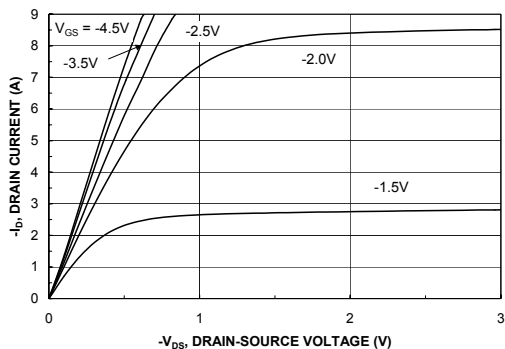


Figure 12. On-Region Characteristics.

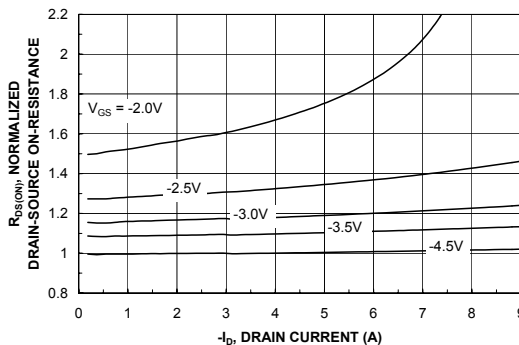


Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

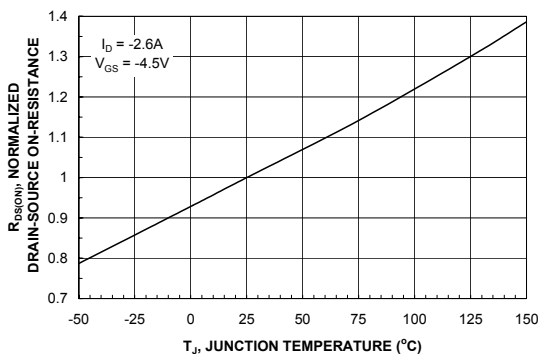


Figure 14. On-Resistance Variation with Temperature.

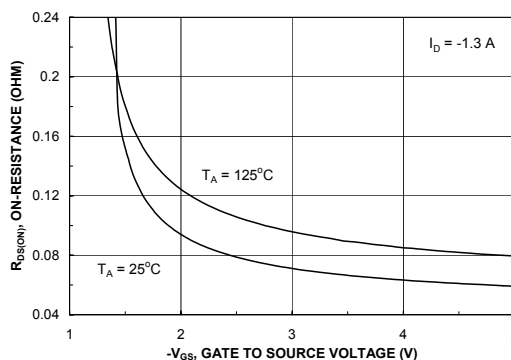


Figure 15. On-Resistance Variation with Gate-to-Source Voltage.

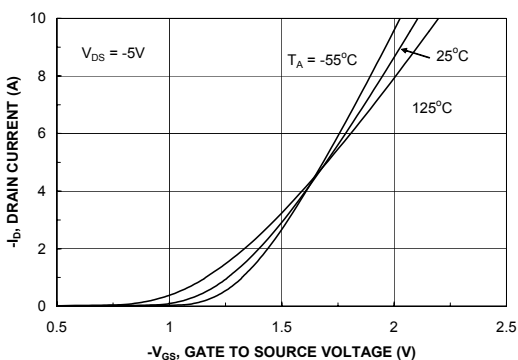


Figure 16. Transfer Characteristics.

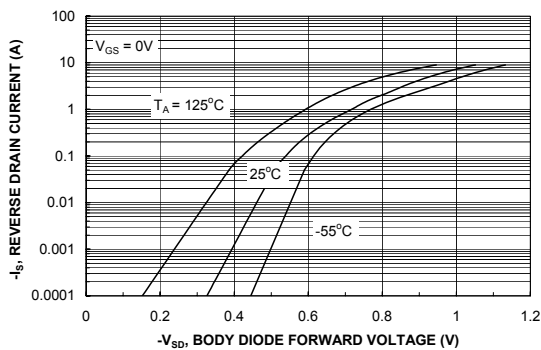


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q2

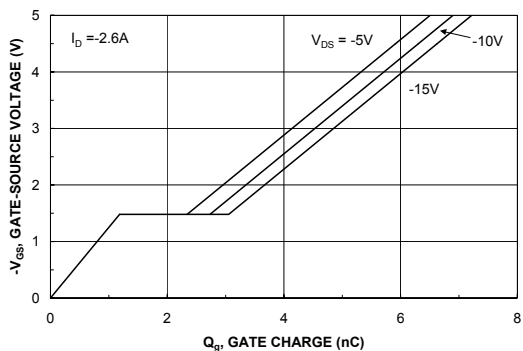


Figure 18. Gate Charge Characteristics.

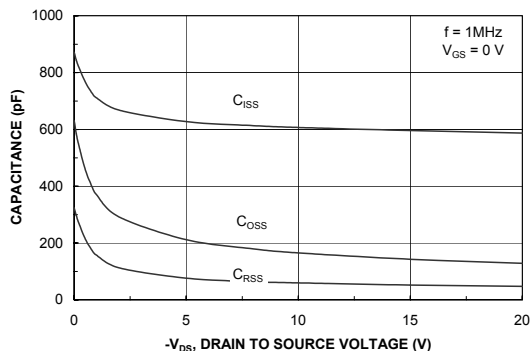


Figure 19. Capacitance Characteristics.

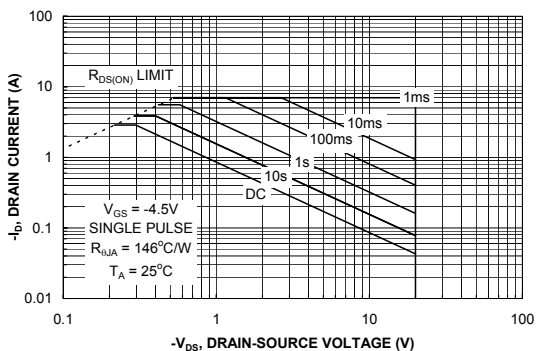


Figure 20. Maximum Safe Operating Area.

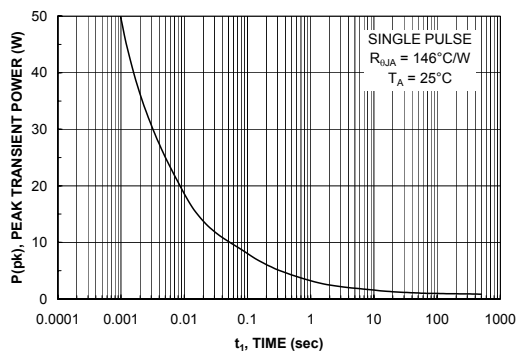


Figure 21. Single Pulse Maximum Power Dissipation.

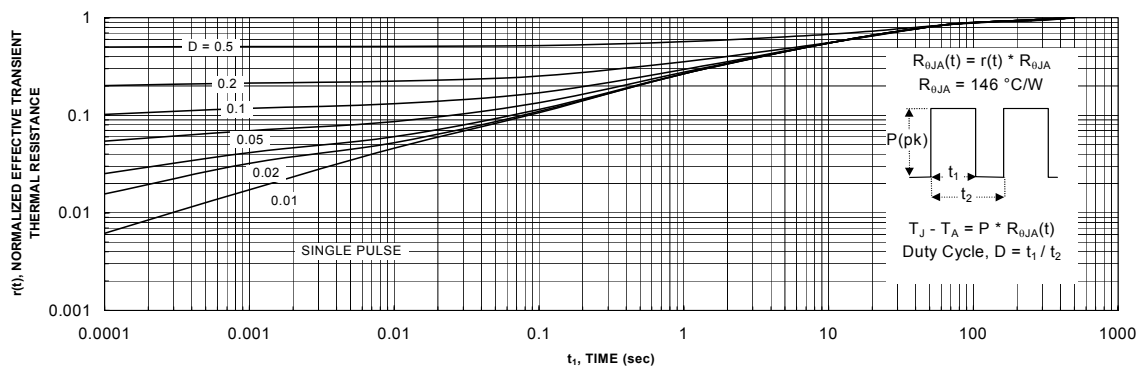


Figure 22. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.

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CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
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EnSigna™	I <sup>2</sup> C™	OCX™	RapidConfigure™	UHC™
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Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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