SANYO *SANYO Semiconductors*

DATA SHEET

Thick-Film Hybrid IC

STK433-270-E — 3-channel class AB audio power IC, 60W×3ch

Overview

The STK433-270-E is a hybrid IC designed to be used in 60W × 3ch class AB audio power amplifiers.

Applications

- Audio power amplifiers.

Features

- Pin-to-pin compatible outputs ranging from 40W to 60W.
- Can be used to replace the STK433-000/-100 series (30W to 150W × 2ch) and STK433-300 series (80W to 150W × 3ch) due to its pin compatibility.
- Miniature package (67.0mm × 25.6mm × 9.0mm)
- Output load impedance: R_L = 6Ω to 4Ω supported
- Allowable load shorted time: 0.3 second
- Allows the use of predesigned applications for standby and mute circuits.

Series Models

	STK433-240A-E	STK433-260A-E	STK433-270-E
Output 1 (10%/1kHz)	40W×3ch	50W×3ch	60W×3ch
Output 2 (0.6%/20Hz to 20kHz)	25W×3ch	35W×3ch	40W×3ch
Maximum rating V_{CC} max (quiescent)	±38V	±46V	±50V
Maximum rating V_{CC} max (6Ω)	±36V	±40V	±44V
Maximum rating V_{CC} max (4Ω)	±30V	±33V	±38V
Recommended operating V_{CC} (6Ω)	±24V	±27V	±29V
Dimensions (excluding pin height)	67.0mm×25.6mm×9.0mm		

Specifications

Absolute Maximum Ratings at Ta = 25°C (excluding rated temperature items), Tc=25°C unless otherwise specified

| Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage 0	V_{CC} max (0)	Non signal	±50	V
Maximum power supply voltage 1	V_{CC} max (1)	$R_L \geq 6\Omega$	±44	V
Maximum power supply voltage 2	V_{CC} max (2)	$R_L = 4\Omega$	±38	V
Minimum operating supply voltage	V_{CC} min		±10	V
Pin 13 input voltage	VST max		-0.3 to +5.5	V
Thermal resistance	θj-c	Per power transistor	3.5	°C/W
Junction temperature	Tj max	Both the Tj max and Tc max conditions must be met.	150	°C
Operating substrate temperature	Tc max		125	°C
Storage temperature	Tstg		-30 to +125	°C
Available time for load short-circuit *4	ts	V_{CC}=±29V, R_L=6Ω, f=50Hz, P_O=40W, 1-channel drive	0.3	s

Operating Characteristics at Tc=25°C, R_L=6Ω, Rg=600Ω, VG=30dB, non-inductive load R_L, unless otherwise specified

Parameter	Symbol	Conditions *2					Ratings			unit
		V_{CC} (V)	f (Hz)	P_O (W)	THD (%)		min	typ	max	
Output power *1	P_O (1)	±29	20 to 20k		0.6		38	40		W
	P_O (2)	±29.5	1k		10			60		
	P_O (3)	±26	1k		1	R_L=4Ω		40		
Total harmonic distortion *1	THD (1)	±29	20 to 20k	5.0					0.6	%
	THD (2)	±29	1k					0.1		
Frequency characteristics *1	f_L, f_H	±29		1.0		+0 -3dB	20 to 50k			Hz
Input impedance	ri	±29	1k	1.0				55		kΩ
Output noise voltage *3	V_{NO}	±35				Rg=2.2kΩ			1.0	mVrms
Quiescent current	I_{CCO}	±35				No loading	30	70	120	mA
Standby current	I_{CST}	±35							1.0	mA
Output neutral voltage	V_N	±35					-70	0	+70	mV
Pin 13 voltage when standby ON *7	VST ON	±29				Standby		0	0.6	V
Pin 13 voltage when standby OFF *7	VST OFF	±29				Operating	2.5		5.5	V

[Remarks]

*1: For 1-channel operation

*2: Unless otherwise specified, use a constant-voltage power supply to supply power when inspections are carried out.

*3: The output noise voltage values shown are peak values read with a VTVM. However, an AC stabilized (50Hz) power supply should be used to minimize the influence of AC primary side flicker noise on the reading.

*4: Use the transformer power supply circuit shown in the figure below for allowable load shorted time and output noise voltage measurement.

*5: Please connect -PreV_{CC} pin (#1 pin)with the stable minimum voltage, and connect so that current does not flow in by reverse bias.

*6: Thermal design must be implemented based on the conditions under which the customer's end products are expected to operate on the market.

*7: The impression voltage of '#13 (Stand-By) pin' must not exceed the maximum rating.
 Power amplifier operate by impressing voltage +2.5 to +5.5V to '#13 (Stand-By) pin'.
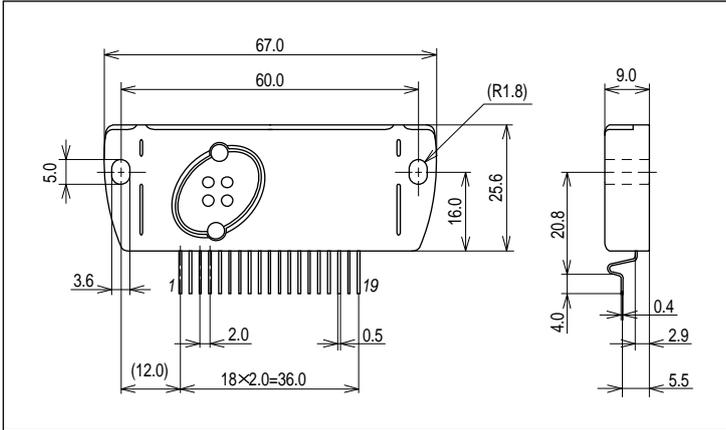
*8: A thermoplastic adhesive is used to adhere the case.
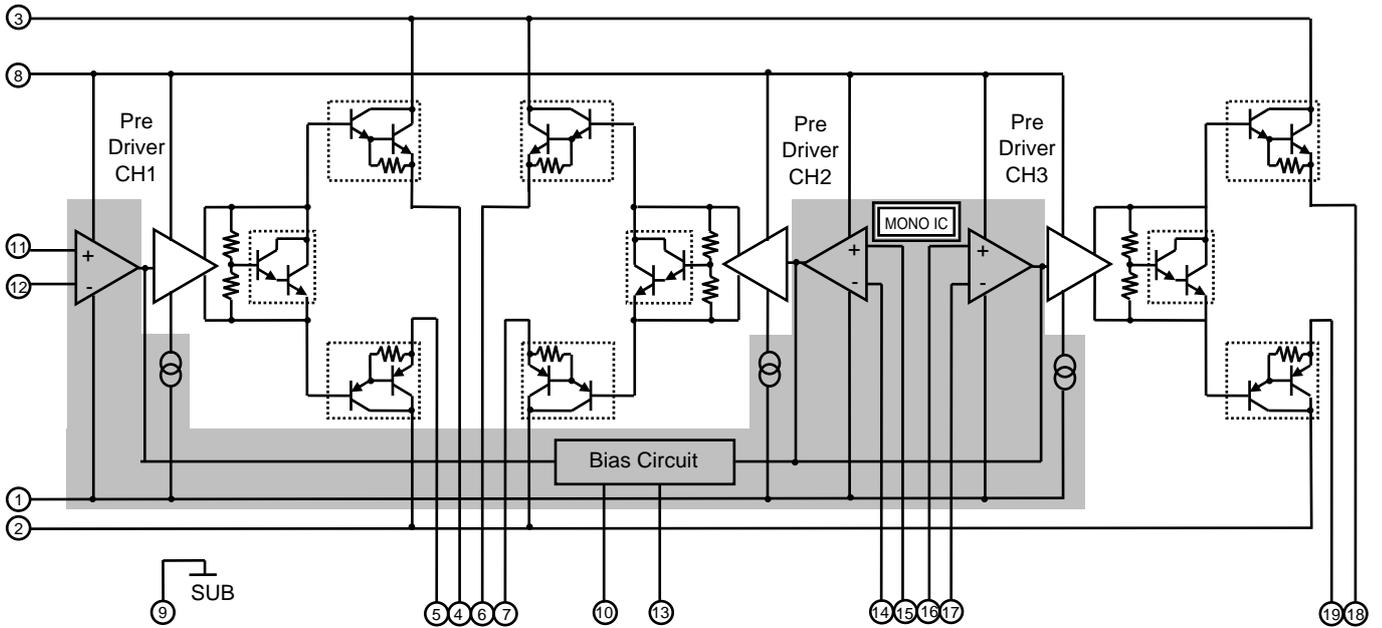
Designated transformer power supply
(MG-200 equivalent)
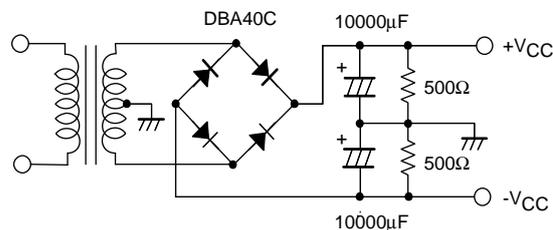
Package Dimensions

unit:mm (typ)

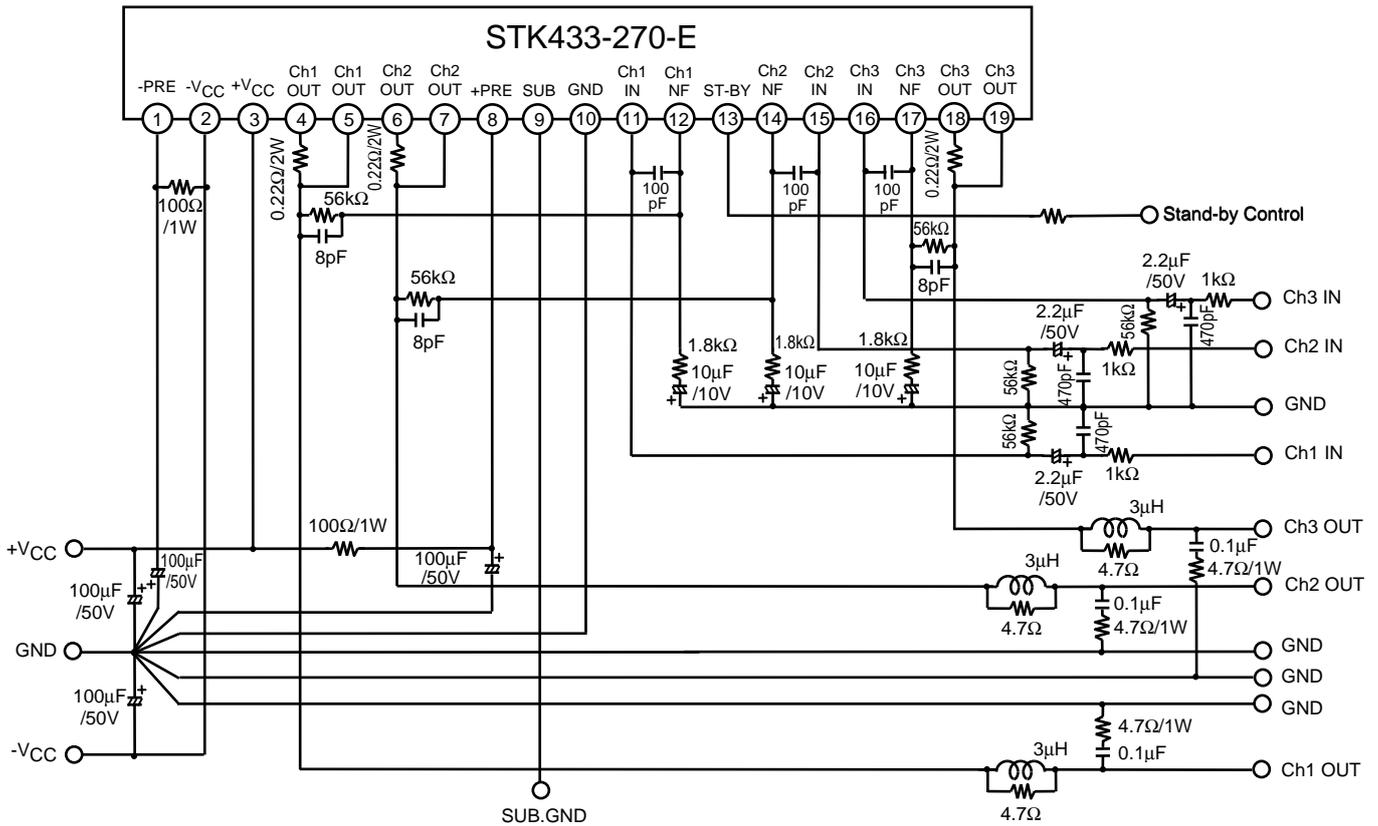## Internal Equivalent Circuit

Test Circuit
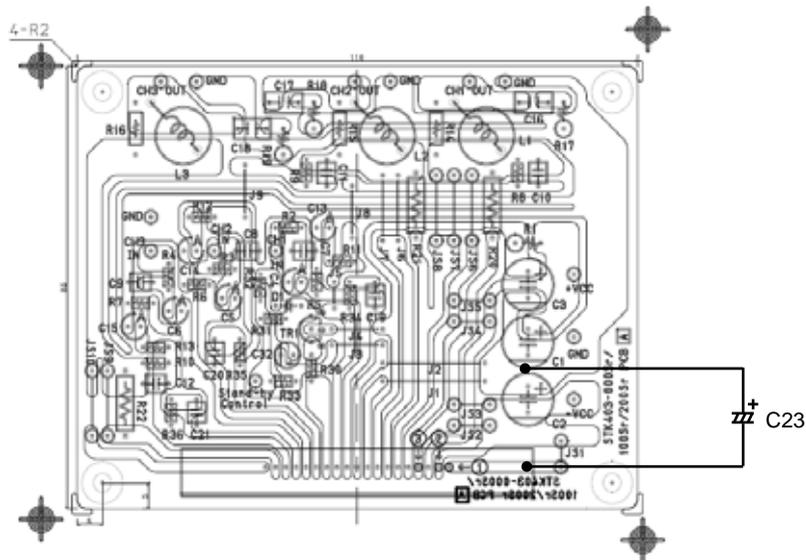

Sample PCB Trace Pattern
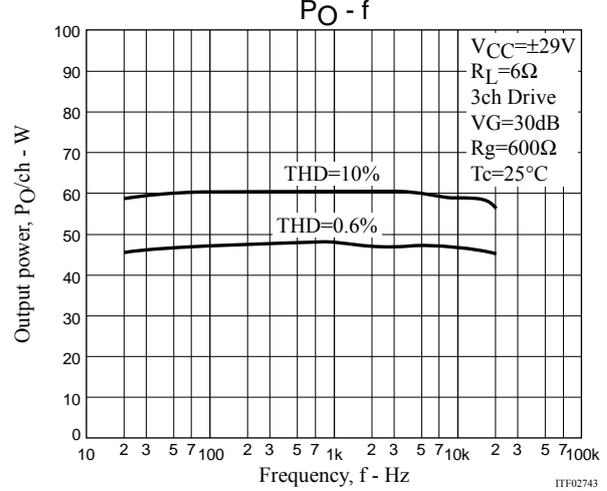
Discontinued

STK433-200-ESr PCB PARTS LIST

Location No.		PARTS	RATING	Component STK433-200-E Series (3ch)		
				-240A	-260A	-270
Hybrid IC #1 Pin Position		-	-	①		
R01		ERG1SJ101	100Ω, 1W	○	○	○
R02, R03, R04		RN16S102FK	1kΩ, 1/6W	○	○	○
R05, R06, R08, R09, R07, R10		RN16S563FK	56kΩ, 1/6W	○	○	○
R11, R12, R13		RN16S182FK	1.8kΩ, 1/6W	○	○	○
R14, R15, R16		RN14S4R7FK	4.7Ω, 1/4W	○	○	○
R17, R18, R19		ERX1SJ4R7	4.7Ω, 1W	○	○	○
R20, R21, R22		ERX2SJR22	0.22Ω, 2W	short	○	○
C01, C02, C03, C23 (*2)		100MV100HC	100μF, 100V	○	○	○
C04, C05, C06 (*1)		50MV2R2HC	2.2μF, 50V	○	○	○
C07, C08, C09		DD104-63B471K50	470pF, 50V	○	○	○
C10, C11, C12		DD104-63CJ0*0C50	*pF, 50V	3pF	3pF	8pF
C13, C14, C15 (*1)		10MV10HC	10μF, 10V	○	○	○
C16, C17, C18		ECQ-V1H104JZ	0.1μF, 50V	○	○	○
C19, C20, C21		DD104-63B101K50	100pF, 50V	○	○	○
R34, R35, R36		-	-	short	short	short
L01, L02, L03		-	3μH	○	○	○
Stand-By Control Circuit	Tr1	2SC3332 (Reference)	$V_{CE} \geq 50V, I_C \geq 1mA$	○	○	○
	D1	GMB01 (Reference)	Di	○	○	○
	R30	RN16S272FK	2.7kΩ, 1/6W	○	○	○
	R31	RN16S333FK	33kΩ, 1/6W	○	○	○
	R32	RN16S102FK	1kΩ, 1/6W	○	○	○
	R33	RN16S202FK	2kΩ, 1/6W	○	○	○
	C32	10MV33HC	33μF, 10V	○	○	○
J1, J2, J3, J4, J5, J6, J8, J9		-	-	○	○	○
J7, JS2, JS3, JS4, JS5, JS7, JS8, JS9		-	-	-	-	-
JS6, JS10		-	-	○	○	○
JS1		ERG1SJ101	100Ω, 1W	○	○	○

(*1) Capacitor mark "A" side is "-" (negative).

(*2) Add parts C23 to the other side of PCB.

Pin Assignments

[STK433-000/-100/-200Sr & STK415/416-100Sr Pin Layout]

2-channel class-AB — 2-channel class AB/2.00mm

Devices: STK433-030-E 30W/JEITA, STK433-040-E 40W/JEITA, STK433-060-E 50W/JEITA, STK433-070-E 60W/JEITA, STK433-090-E 80W/JEITA, STK433-100-E 100W/JEITA, STK433-120-E 120W/JEITA, STK433-130-E 150W/JEITA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
-PRE	-VCC	+VCC	OUT/CH1+	OUT/CH1-	OUT/CH2+	OUT/CH2-	+PRE	SUB•GND	GND	IN/CH1	NF/CH1	STAND|BY	NF/CH2	IN/CH2

3-channel class-AB — 3-channel class AB/2.00mm

Devices: STK433-240A-E 40W/JEITA, STK433-260A-E 50W/JEITA, **STK433-270-E 60W/JEITA**, STK433-290-E 80W/JEITA, STK433-300-E 100W/JEITA, STK433-320-E 120W/JEITA, STK433-330-E 150W/JEITA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
-PRE	-VCC	+VCC	OUT/CH1+	OUT/CH1-	OUT/CH2+	OUT/CH2-	+PRE	SUB•GND	GND	IN/CH1	NF/CH1	STAND|BY	NF/CH2	IN/CH2	IN/CH3	NF/CH3	OUT/CH3+	OUT/CH3-

2-channel class-H — 2-channel class H/2.00mm

Devices: STK415-090-E 80W/JEITA, STK415-100-E 90W/JEITA, STK415-120-E 120W/JEITA, STK415-130-E 150W/JEITA, STK415-140-E 180W/JEITA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
+VL	-VL	+OFFSET	-OFFSET	-PRE	-VH	+VH	OUT/CH1+	OUT/CH1-	OUT/CH2+	OUT/CH2-	+PRE	SUB•GND	GND	IN/CH1	NF/CH1	STAND|BY	NF/CH2	IN/CH2

3-channel class-H — 3-channel class H/2.00mm

Devices: STK416-100-E 90W/JEITA, STK416-120-E 120W/JEITA, STK416-130-E 150W/JEITA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
+VL	-VL	+OFFSET	-OFFSET	-PRE	-VH	+VH	OUT/CH1+	OUT/CH1-	OUT/CH2+	OUT/CH2-	+PRE	SUB•GND	GND	IN/CH1	NF/CH1	STAND|BY	NF/CH2	IN/CH2	IN/CH3	NF/CH3	OUT/CH3+	OUT/CH3-

Evaluation Board Characteristics

THD - P_O

Pd - P_O

P_O - V_{CC}

P_O - f
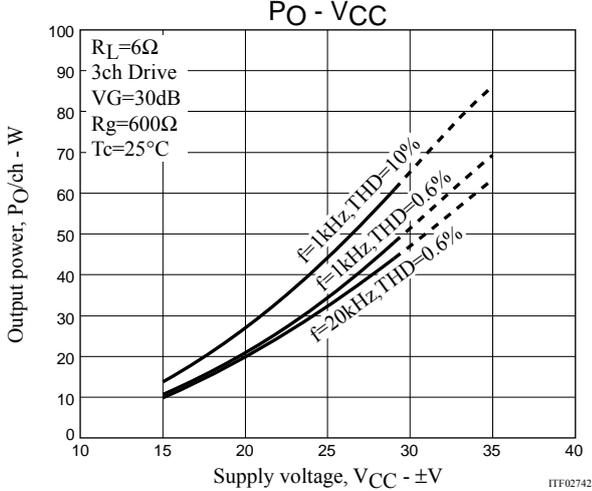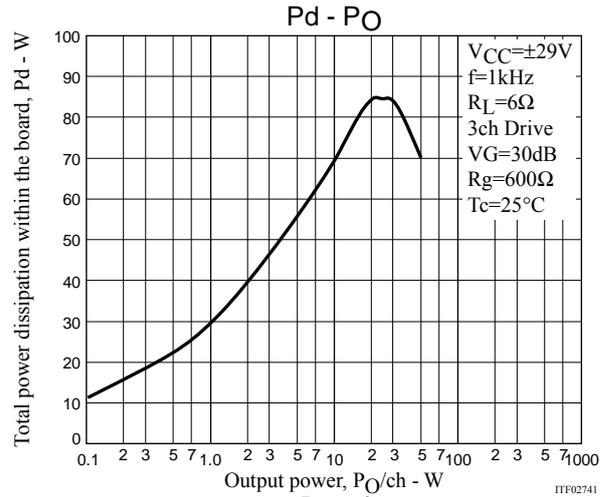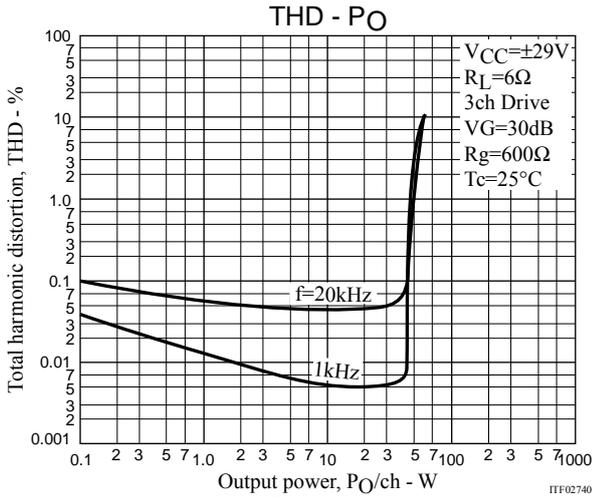
[Thermal Design Example for STK433-270-E ($R_L = 6\Omega$)]

The thermal resistance, θc-a, of the heat sink for total power dissipation, Pd, within the hybrid IC is determined as follows.

Condition 1: The hybrid IC substrate temperature, Tc, must not exceed 125°C.

$$Pd \times \theta c\text{-}a + Ta < 125°C \quad\text{.. (1)}$$

Ta: Guaranteed ambient temperature for the end product

Condition 2: The junction temperature, Tj, of each power transistor must not exceed 150°C.

$$Pd \times \theta c\text{-}a + Pd/N \times \theta j\text{-}c + Ta < 150°C \quad\text{.. (2)}$$

N: Number of power transistors

θj-c: Thermal resistance per power transistor

However, the power dissipation, Pd, for the power transistors shall be allocated equally among the number of power transistors.

The following inequalities result from solving equations (1) and (2) for θc-a.

$$\theta c\text{-}a < (125 - Ta)/Pd \quad\text{.. (1)'}$$

$$\theta c\text{-}a < (150 - Ta)/Pd - \theta j\text{-}c/N \quad\text{.. (2)'}$$

Values that satisfy these two inequalities at the same time represent the required heat sink thermal resistance.

When the following specifications have been stipulated, the required heat sink thermal resistance can be determined from formulas (1)' and (2)' .

- Supply voltage $\quad\quad\quad V_{CC}$
- Load resistance $\quad\quad\quad R_L$
- Guaranteed ambient temperature $\quad Ta$

[Example]

When the IC supply voltage, V_{CC}, is ±29V and R_L is 6Ω, the total power dissipation, Pd, within the hybrid IC, will be a maximum of 105W at 1kHz for a continuous sine wave signal according to the Pd-P_O characteristics. For the music signals normally handled by audio amplifiers, a value of 1/8P_O max is generally used for Pd as an estimate of the power dissipation based on the type of continuous signal. (Note that the factor used may differ depending on the safety standard used.)

This is:

$\quad$ Pd $\approx$ 75.0W $\qquad\qquad$ (when 1/8P_O max. = 5W, P_O max. = 40W).

The number of power transistors in audio amplifier block of these hybrid ICs, N, is 6, and the thermal resistance per transistor, θj-c, is 3.5°C/W. Therefore, the required heat sink thermal resistance for a guranteed ambient temperature, Ta, of 50°C will be as follows.

$\quad$ From formula (1)' $\qquad$ θc-a < (125 − 50)/75.0
$\qquad\qquad\qquad\qquad\qquad\qquad$ < 1.00
$\quad$ From formula (2)' $\qquad$ θc-a < (150 − 50)/75.0 − 3.5/6
$\qquad\qquad\qquad\qquad\qquad\qquad$ < 0.75

Therefore, the value of 0.75°C/W, which satisfies both of these formulae, is the required thermal resistance of the heat sink.

Note that this thermal design example assumes the use of a constant-voltage power supply, and is therefore not a verified design for any particular user's end product.

STK433-200(A)-E series Stand-by control, Mute control, Load-short protection & DC offset protection application
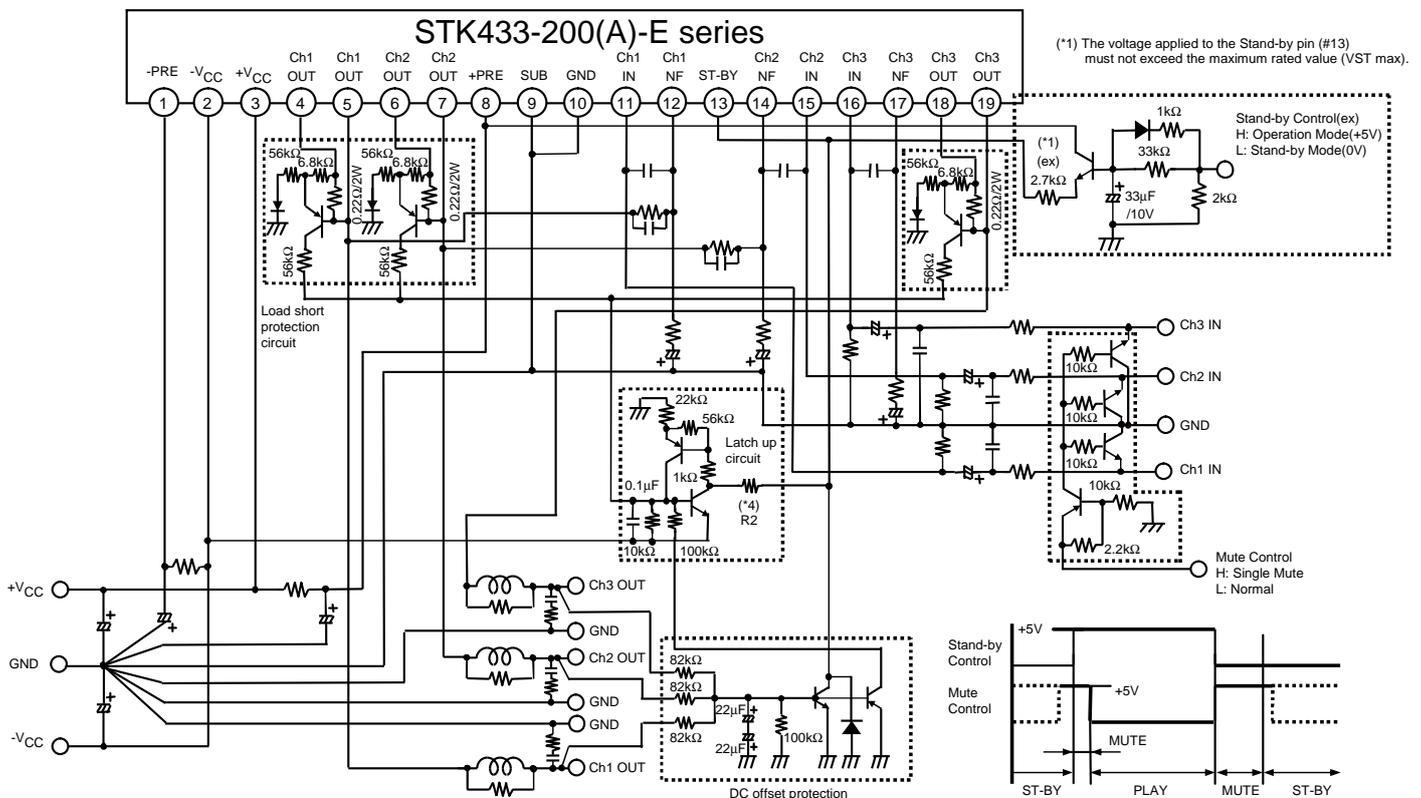
STK433-200(A)series Stand-by Control & Mute Control & Load-Short Protection Application
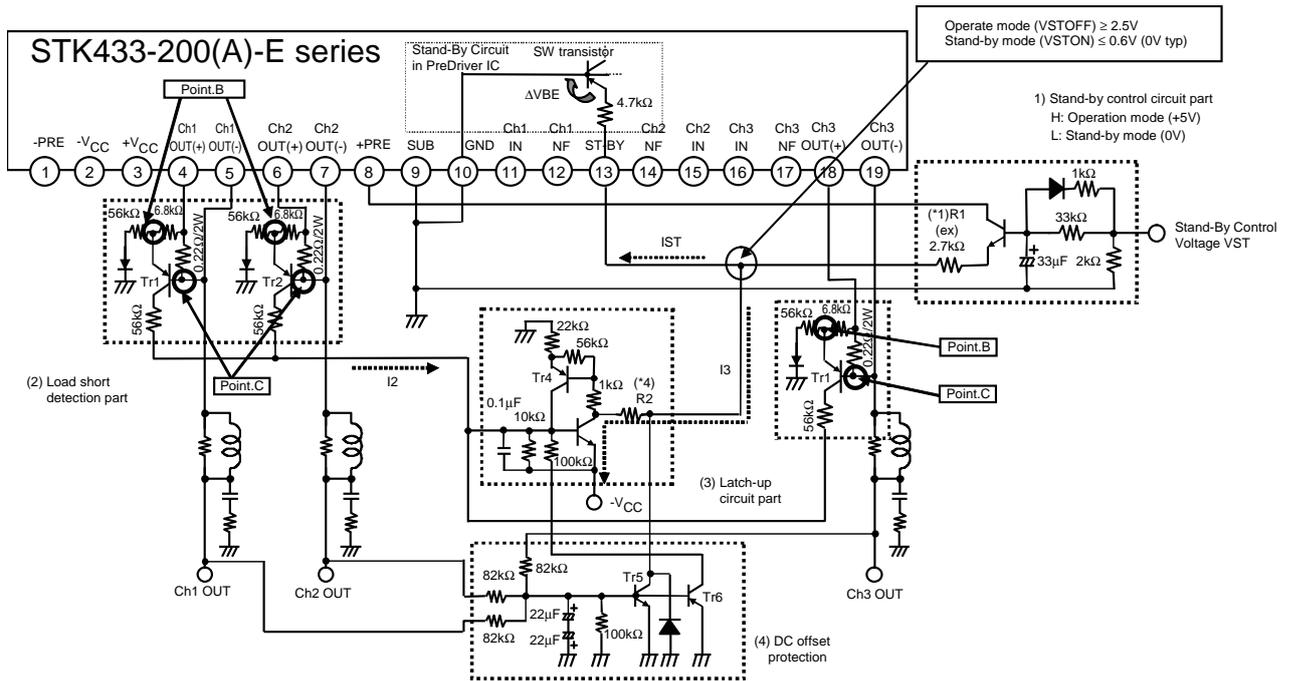
The protection circuit application for the STK433-200(A)-Esr consists of the following blocks (blocks (1) to (4)).
(1) Standby control circuit block
(2) Load short-circuit detection block
(3) Latch-up circuit block
(4) DC voltage protection block

1) Stand-by control circuit block
   (Reference example) STK433-200(A)-E series test circuit (when +5V is applied to Stand-by control.)

$$ex) VST=(V1-VBE\times2)\times(*2)/((*1)+(*2))+VBE$$
$$=(5V-0.6V\times2)\times4.7k\Omega/(4.7k\Omega+2.7k\Omega)+0.6V$$
$$=3.0(V)$$
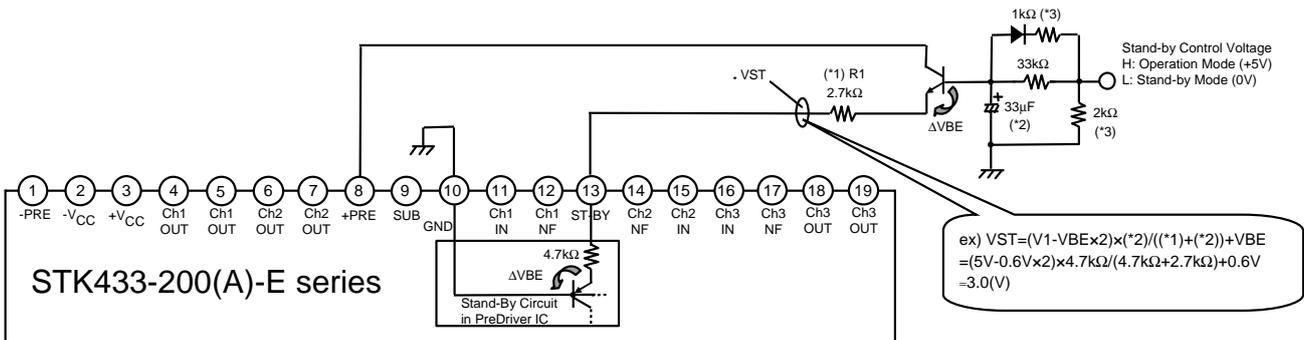
Concerning pin 13 reference voltage VST

<1> Operation Mode
     The switching transistor in the bias circuit turns on and places the amplifier into the operating mode when the voltage flowing into pin 13 (VST) becomes 0.25V or greater.
<2> Stand-By Mode
     When the voltage flowing into pin 13 (VST) is stopped (=0V), the switching transistor in the bias circuit turns off, placing the amplifier into the standby mode.
(*1) The current limiting resistor (R1) must be used to ensure that the voltage flowing into the stand-by pin (pin 13) does not exceed its maximum rated value VST max.
(*2) The pop noise level when the power is turned on can be reduced by setting the time constant with a capacitor in operating mode.
(*3) Determines the time constant at which the capacitor (*2) is discharged in standby mode.

2) Load short detection block

Since the voltage between point B and point C is less than 0.6V in normal operation mode (V_{BE} < 0.6V) and TR1 (or TR2) is not activated,

the load short-circuit detection block does not operate.

When a load short-circuit occurs, however, the voltage between point B and point C becomes larger than 0.6V, causing TR1 (or TR2) to turn on (V_{BE} > 0.6V), and current I2 to flows

3) Latch-up circuit block

When I2 was supplied to latch-up circuit, TR3 operate.

VST becomes Stand-By Mode (0V) when TR3 operates (I3 flows), the power amplifier is protected.

Stand-By Mode is maintained when once TR3 operates because TR3 and TR4 compose the thyristor.

It is necessary to make the Stand-By Control voltage (*2) L (0V) once to release Stand-By mode and to make the power amplifier operate again.

After, when Stand-By Control (*2) is returned to H (ex, +5V), it operates again.

(*4) I3 is changed depending on the power-supply voltage (-V_{CC}).

Please set resistance (R2) to become I1 < I3 by the following calculation types.

$$I1 \leq I3 = V_{CC}/R2$$

4) DC offset protection block

The DC offset protection circuit is activated when ±0.5V (typ) voltage is applied to either "OUT CH1" or "OUT CH2," or "OUT CH3," and the hybrid IC is shut down (standby mode). To release the IC from the standby mode and reactivate the power amplifier, it is necessary to set the standby control voltage temporarily low (0V). Subsequently, when the standby control is returned to high (+5V, for example), the power amplifier will become active again.

The protection level must be set using the 82kΩ resistor. Furthermore, the time constant must be determined using 22μ//22μ capacitors to prevent the amplifier from malfunctioning due to the audio signal.