MOTOROLA
**SEMICONDUCTOR**
TECHNICAL DATA

**MC54/74HC241A**

*Advance Information*

# Octal 3-State Noninverting Buffer/Line Driver/ Line Receiver

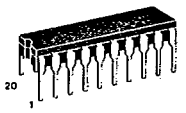
## High-Performance Silicon-Gate CMOS

The MC54/74HC241A is identical in pinout to the LS241. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

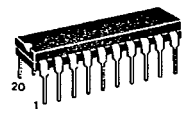
This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has noninverted outputs and two output enables. Enable A is active-low and Enable B is active-high.

The HC241A is similar in function to the HC244A and HC240A.

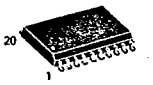
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



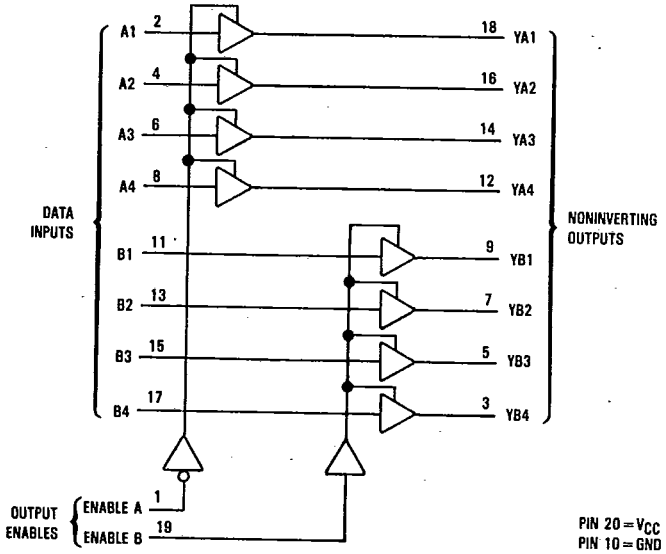
DW SUFFIX
SOIC
CASE 751D-03

**ORDERING INFORMATION**

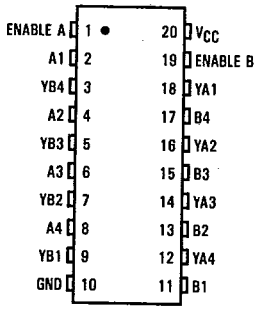
| | |
|---|---|
| MC74HCXXXAN | Plastic |
| MC54HCXXXAJ | Ceramic |
| MC74HCXXXADW | SOIC |

$T_A = -55°$ to 125°C for all packages.

**LOGIC DIAGRAM**




**PIN ASSIGNMENT**




**FUNCTION TABLE**

| Inputs | | Output | Inputs | | Output |
|---|---|---|---|---|---|
| Enable A | A | YA | Enable B | B | YB |
| L | L | L | H | L | L |
| L | H | H | H | H | H |
| H | X | Z | L | X | Z |

Z = high impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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# MC54/74HC241A

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | −0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | −1.5 to $V_{CC}$+1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | −0.5 to $V_{CC}$+0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±75 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† | 750 500 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP) | 260 300 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) | $V_{CC}$ = 2.0 V | 0 | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | 0 | 500 | |
| | | $V_{CC}$ = 6.0 V | 0 | 400 | |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit 25°C to −55°C | Guaranteed Limit ≤85°C | Guaranteed Limit ≤125°C | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{out}$ = $V_{CC}$ − 0.1 V, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| $V_{IL}$ | Maximum Low-Level Input Voltage | $V_{out}$ = 0.1 V, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 6.0 | 1.8 | 1.8 | 1.8 | |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in}$ = $V_{IH}$, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{in}$ = $V_{IH}$, $\|I_{out}\|$ ≤ 6.0 mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | $V_{in}$ = $V_{IH}$, $\|I_{out}\|$ ≤ 7.8 mA | 6.0 | 5.48 | 5.34 | 5.20 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{in}$ = $V_{IL}$, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{in}$ = $V_{IL}$, $\|I_{out}\|$ ≤ 6.0 mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | $V_{in}$ = $V_{IL}$, $\|I_{out}\|$ ≤ 7.8 mA | 6.0 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three-State Leakage Current | Output in High-Impedance State, $V_{in}$ = $V_{IL}$ or $V_{IH}$, $V_{out}$ = $V_{CC}$ or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND, $I_{out}$ = 0 μA | 6.0 | 4 | 40 | 160 | μA |

NOTE: Information on typical parametric values along with high frequency or heavy load considerations, can be found in Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

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**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3) | 2.0<br>4.5<br>6.0 | 90<br>18<br>15 | 115<br>23<br>20 | 135<br>27<br>23 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 110<br>22<br>19 | 140<br>28<br>24 | 165<br>33<br>28 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 110<br>22<br>19 | 140<br>28<br>24 | 165<br>33<br>28 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0<br>4.5<br>6.0 | 60<br>12<br>10 | 75<br>15<br>13 | 90<br>18<br>15 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three-State Output Capacitance (Output in High-Impedance State) | — | 15 | 15 | 15 | pF |

| | | | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Transceiver Channel)<br>Used to determine the no-load dynamic power consumption:<br>$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ | Typical @ 25°C, $V_{CC}$ = 5.0 V<br>34 | pF |

NOTE: For propagation delays with loads other than 50 pF and information on typical parametric values and load considerations, see Chapter 4, of the Motorola High-Speed CMOS Logic Data Book — DL129/R3.

## SWITCHING WAVEFORMS

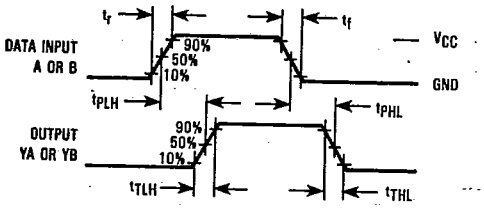



Figure 1

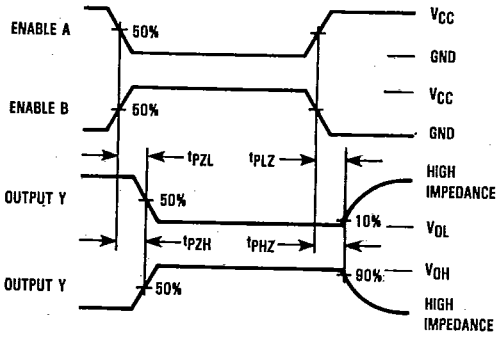
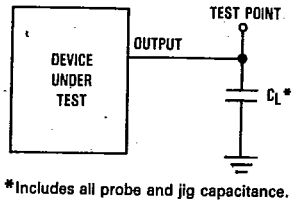
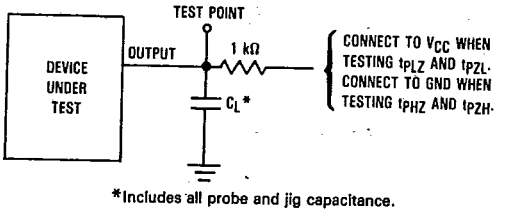



Figure 2




*Includes all probe and jig capacitance.

Figure 3. Test Circuit




*Includes all probe and jig capacitance.

Figure 4. Test Circuit

# MC54/74HC241A

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, B1, B2, B3, B4 (PINS 2, 4, 6, 8, 11, 13, 15, 17)** — Data input pins. Data on these pins appear in noninverted form on the corresponding Y outputs when the outputs are enabled.

### CONTROLS

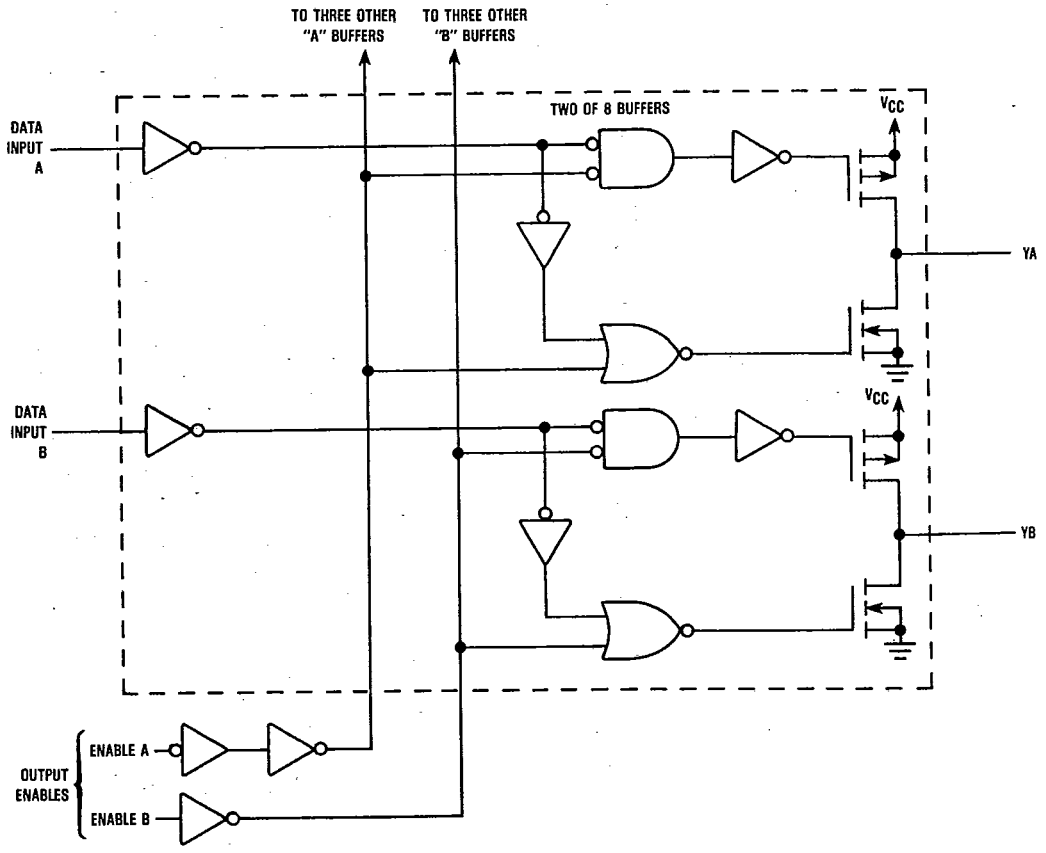
**Enable A (PIN 1)** — Output enable (active-low). When a low level is applied to this pin, the outputs of the "A" devices are enabled and the devices function as noninverting buffers. When a high level is applied, the outputs assume the high-impedance state.

**Enable B (PIN 19)** — Output enable (active-high). When a high level is applied to this pin, the outputs of the "B" devices are enabled and the devices function as noninverting buffers. When a low level is applied, the outputs assume the high-impedance state.

### OUTPUTS

**YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4 (PINS 18, 16, 14, 12, 9, 7, 5, 3)** — Device outputs. Depending upon the state of the output-enable pins, these outputs are either noninverting outputs or high-impedance outputs.

## LOGIC DETAIL

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