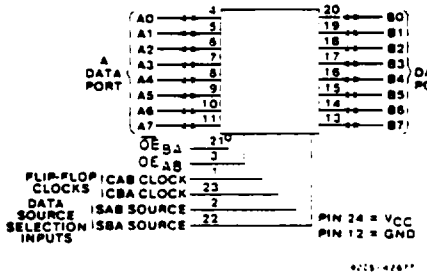
HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

RCA High-Speed CMOS Logic

CD54/74HC651, CD54/74HC652
CD54/74HCT651, CD54/74HCT652

Advance Information



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver/Registers, 3-State

CD54/74HC/HCT651 - Inverting
CD54/74HC/HCT652 - Non-Inverting

Type Features:

- *Independent Registers for A and B Buses*
- *3-State Outputs*
- *Drives 15 LSTTL loads*
- *Typical Propagation Delay = 12 ns @ V_{CC} = 5 V, C_L = 15 pF*

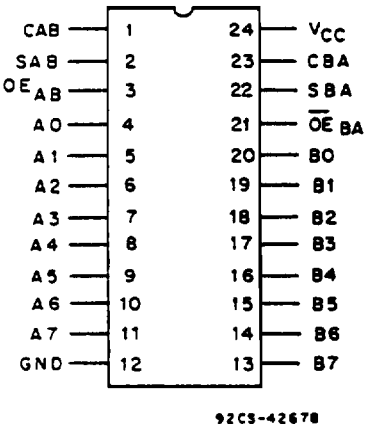
The RCA-CD54/74HC651 and CD54/74HC652 and the CD54/74HCT651 and CD54/74HCT652 3-state, octal-bus transceiver/registers use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits. The CD54/74HC651 and CD54/74HCT651 have inverting outputs. The CD54/74HC652 and CD54/74HCT652 have non-inverting outputs. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and $\overline{OE}_{BA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD54HC651 and CD54HC652 and the CD54HCT651 and CD54HCT652 are supplied in 24-lead dual-in-line frit-seal ceramic packages (F suffix). The CD74HC651 and CD74HC652 and the CD74HCT651 and CD74HCT652 are supplied in 24-lead dual-in-line, narrow-body, plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating-Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



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TERMINAL ASSIGNMENT

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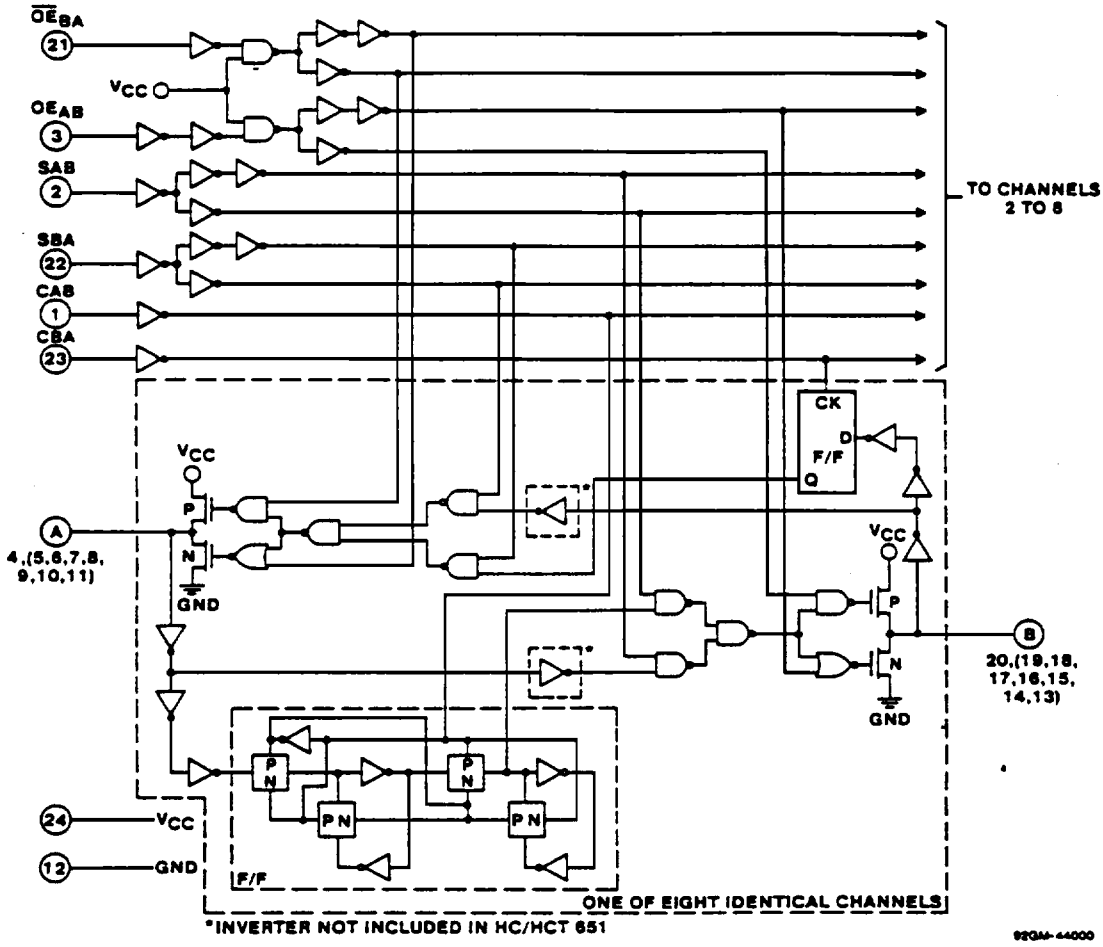


Fig. 1 - Logic Diagram.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE_{AB}	$\overline{OE}_{BA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	651	652
L	H	H or L	H or L	X	X	Input	Input	Isolation *	Isolation*
L	H	⎍	⎍	X	X			Store A and B Data	Store A and B Data
X	H	⎍	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	⎍	⎍	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	⎍	X	X	Unspecified†	Input	Hold A, Store B	Hold A, Store B
L	L	⎍	⎍	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A bus	Stored A Data to B Bus Stored B Data to A Bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE_{AB} or $\overline{OE}_{BA}$ inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V) ..... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +100°C (PACKAGE TYPE EN) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE EN) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE EN, M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}*:			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature T_A			
CD74 Types	-40	+125	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC651/CD54HC651 CD74HC652/CD54HC652										CD74HCT651/CD54HCT651 CD74HCT652/CD54HCT652									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5		—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.3	—	0.3	—	0.3	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	0.9	—	0.9	—	0.9										
			6	—	—	1.2	—	1.2	—	1.2										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{OE}_{BA}$	1.3
OE_{AB}	0.75
Clock A—B, B—A	0.6
Select A, Select B	0.45
Inputs A_0-A_7, B_0-B_7	0.3

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delays					
Store A Data to B Bus (652)	t_{PLH}, t_{PHL}	15	18	18	ns
Store B Data to A Bus (652)	t_{PLH}, t_{PHL}	15	18	18	ns
Store $\overline{A}$ Data to B Bus (651)	t_{PLH}, t_{PHL}	15	20	23	ns
Store $\overline{B}$ Data to A Bus (651)	t_{PLH}, t_{PHL}	15	20	23	ns
A Data to B Bus (652)	t_{PLH}, t_{PHL}	15	12	15	ns
B Data to A Bus (652)	t_{PLH}, t_{PHL}	15	12	15	ns
$\overline{A}$ Data to B Bus (651)	t_{PLH}, t_{PHL}	15	12	15	ns
$\overline{B}$ Data to A Bus (651)	t_{PLH}, t_{PHL}	15	12	15	ns
Select to Data (652)	t_{PLH}, t_{PHL}	15	14	19	ns
Select to Data (651)	t_{PLH}, t_{PHL}	15	16	19	ns
3-State Disabling Time	t_{PLZ}, t_{PHZ}	15	14	14	ns
3-State Enabling Time	t_{PZL}, t_{PZH}	15	14	19	ns
Maximum Frequency	f_{MAX}	15	60	45	MHz
Power Dissipation Capacitance*	C_{PD}	—	52	52	pF

*C_{PD} is used to determine the dynamic power consumption, per package
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o$ where: C_L = output load capacitance
V_{CC} = supply voltage
f_i = input frequency
f_o = output frequency

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	17	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	
Setup Time Data to Clock	t_{su}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time Data to Clock	t_H	2	35	—	—	—	45	—	—	—	55	—	—	—	ns
		4.5	7	—	5	—	9	—	5	—	11	—	5	—	
		6	6	—	—	—	8	—	—	—	9	—	—	—	
Clock Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	25	—	20	—	31	—	24	—	38	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,		2	—	220	—	—	—	275	—	—	—	300	—	—	
Store A data to B Bus	t_{PLH}	4.5	—	44	—	44	—	55	—	55	—	66	—	66	ns
Store B data to A Bus (652)	t_{PHL}	6	—	37	—	—	—	47	—	—	—	5.6	—	—	
Store $\overline{A}$ data to B Bus	t_{PLH}	2	—	240	—	—	—	300	—	—	—	360	—	—	
Store $\overline{B}$ data to A Bus	t_{PHL}	4.5	—	48	—	54	—	60	—	68	—	72	—	81	ns
(651)		6	—	41	—	—	—	51	—	—	—	61	—	—	
A data to B Bus	t_{PLH}	2	—	135	—	—	—	170	—	—	—	205	—	—	
B data to A Bus	t_{PHL}	4.5	—	27	—	37	—	34	—	46	—	41	—	56	ns
(652)		6	—	23	—	—	—	29	—	—	—	35	—	—	
$\overline{A}$ data to B Bus	t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{B}$ data to A Bus	t_{PHL}	4.5	—	30	—	37	—	38	—	46	—	45	—	56	ns
(651)		6	—	26	—	—	—	33	—	—	—	38	—	—	
Select to Data		2	—	170	—	—	—	215	—	—	—	255	—	—	
	t_{PLH}	4.5	—	34	—	46	—	43	—	58	—	51	—	69	ns
(652)	t_{PHL}	6	—	29	—	—	—	37	—	—	—	43	—	—	
Select to Data		2	—	190	—	—	—	240	—	—	—	285	—	—	
	t_{PLH}	4.5	—	38	—	46	—	48	—	58	—	57	—	69	ns
(651)	t_{PHL}	6	—	32	—	—	—	39	—	—	—	48	—	—	
3-State Disabling Time		2	—	175	—	—	—	220	—	—	—	265	—	—	
Bus to Output or	t_{PLZ}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
Register to Output	t_{PHZ}	6	—	30	—	—	—	37	—	—	—	45	—	—	
3-State Enabling Time		2	—	175	—	—	—	220	—	—	—	265	—	—	
Bus to Output or	t_{PZL}	4.5	—	35	—	45	—	44	—	56	—	53	—	68	ns
Register to Output	t_{PZH}	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Transition Time		2	—	60	—	—	—	75	—	—	—	90	—	—	
	t_{TLH}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
	t_{THL}	6	—	10	—	—	—	13	—	—	—	15	—	—	
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

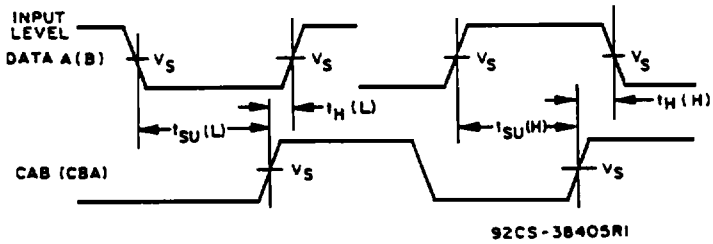
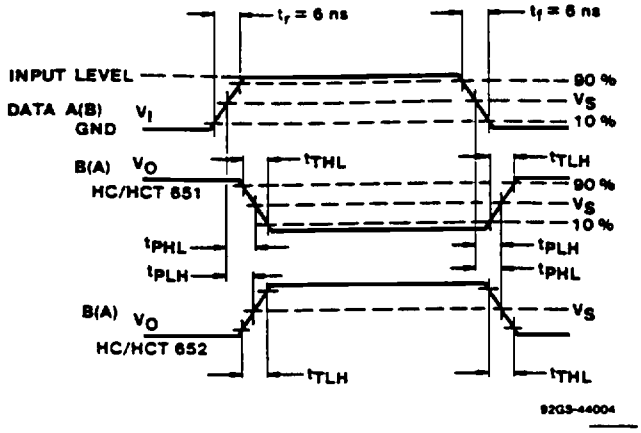
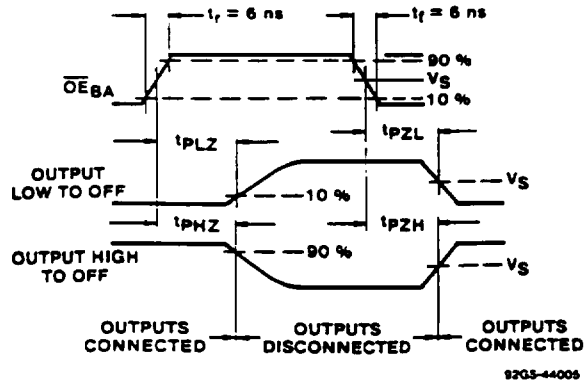


Fig. 2 - Data setup and hold times.

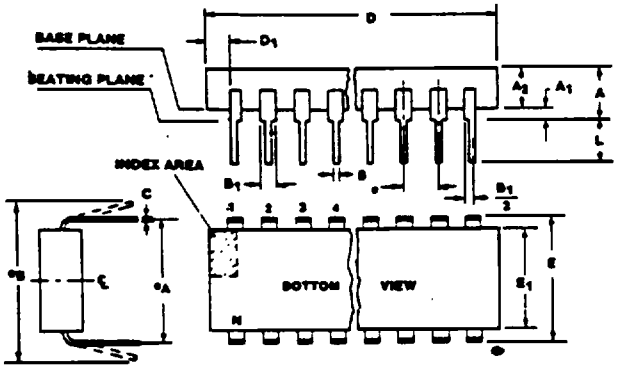




	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 3 - Transition times and propagation delay times.

DIMENSIONAL OUTLINES
(EN) SUFFIX (JEDEC MS-001-AF)
24-Lead Dual-In-Line Narrow-Body Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

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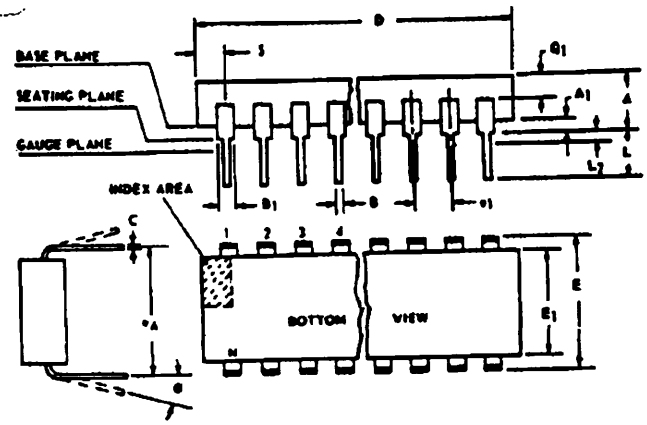
Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

DIMENSIONAL OUTLINES (cont'd)
(F) SUFFIX (JEDEC MO-015-AA)
24-Lead Dual-In-Line Frit-Seal Ceramic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.250	3.10	6.30	
A_1	0.020	0.070	0.51	1.77	
B	0.016	0.020	0.407	0.508	
B_1	0.028	0.070	0.72	1.77	
C	0.008	0.012	0.204	0.304	1
D	1.200	1.290	30.48	32.76	
E	0.600	0.625	15.24	15.87	
E_1	0.515	0.580	13.09	14.73	
e_1	0.100 TP		2.54 TP		2
e_A	0.600 TP		15.24 TP		2,3
L	0.100	0.200	2.54	5.00	
L_2	0.000	0.030	0.00	0.76	
α	0°C	15°C	0°C	15°C	4
N	24		24		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.040	0.100	1.02	2.54	

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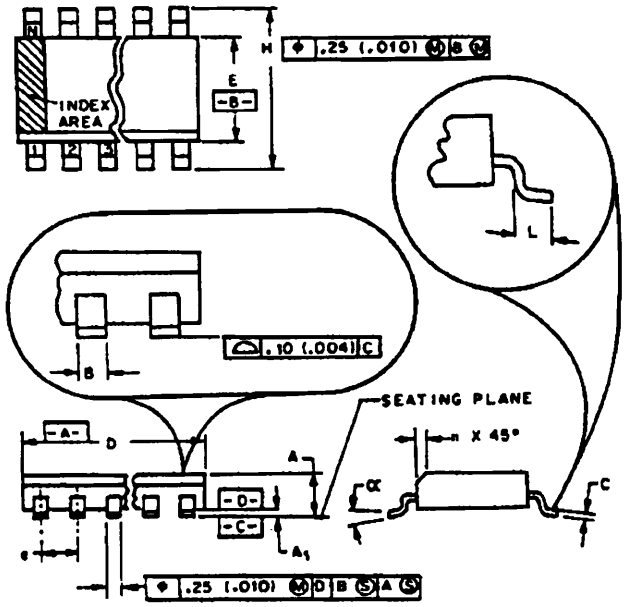
NOTES:

Refer to JEDEC Publication No. 95 for Rules for Dimensioning Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).
2. Leads within 0.005 in. (0.127 mm) radius of True Position (TP) at gauge plane with maximum material condition.
3. e_A applies in zone L_2 when unit is installed.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(M) SUFFIX (JEDEC MS-013-AD)
24-Lead Dual-In-Line
Small-Outline Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA High-Speed CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for High-Speed CMOS devices are similar to those described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} — Gnd to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than Gnd. Input currents must not exceed 20 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or Gnd, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{CC} or Gnd may damage High-Speed CMOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

RCA CMOS device packages are identified by letters indicated in the following chart. When ordering a CMOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Narrow-Body Plastic	EN
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Small-Outline Plastic	M
Chip	H

The CD54HC/HCT series is supplied in dual-in-line frit-seal ceramic packages (F suffix), and in chip form (H suffix). The CD74HC/HCT series is supplied in dual-in-line, narrow-body, plastic packages (EN suffix), dual-in-line, small-outline plastic packages (M suffix), and in chip form (H suffix).

For example, a CD54HC651 will be identified as the CD54HC651F. The CD74HC651 will be identified as the CD74HC651EN or CD74HC651M.