REVISIONS

LTR	DESCRIPTION	DATE(YR-MO-DA)	APPROVED
A	Add three vendors, 18324, 1FN41, and 66579. Add device types 04, 05, 06, and 07. Add margin test method C. Update vendor's PIN. Change code indent. no. to 67268. Editorial changes throughout.	87-12-17	M. A. Frye
B	Add device type 08 with vendors CAGE 1FN41 and CAGE 66579. Added time temperature regression equation for unbiased bake. Removed vendor CAGE 66302. Made technical changes to table I, 4.2 back end margin test method step 3, 4.3.1 step C, table II, and table III. Editorial changes throughout. Added vendor's PIN from XMB/883 to either LM/883 for appropriate device types. Deleted the top CE waveform on figure 6. This was incorrect for this device.	89-01-01	M. A. Frye
C	Added vendor CAGE 34335 to the drawing as a source of supply for device types 01 through 07. Add vendor CAGE number 66579 to device types 01 through 04, also add vendor CAGE number 01295 to devices 04XX and 05XX. Add test condition A to 4.2 and 4.3.2. Add margin test method E for vendor CAGE number 34335. Change to vendor similar PIN for vendor CAGE numbers 1FN41 and 66579. Change to figure 3, margin test method C for vendor CAGE 01295 and change to programming waveforms. Change to 4.5. Editorial changes throughout. Add case outline Z for vendor CAGE number 1FN41.	90-12-05	M. A. Frye
D	Changes in accordance with NOR 5962-R130-92.	92-01-30	M. A. Frye
E	Add case outline U. Add device types 09 and 10. Remove vendor 27014 from drawing. Editorial changes throughout.	93-10-15	M. A. Frye
F	Changes in accordance with NOR 5962-R118-94.	94-02-16	M. A. Frye
G	Updated boilerplate. Added device types 11-21. Removed vendors 1FN41, 18324, 34335, and 61394 from drawing. Added vendor 65786 to drawing. Removed margin test methods from drawing.	97-06-11	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	G	G																		
SHEET	15	16																		

REV STATUS OF SHEETS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
87-02-12

REVISION LEVEL
G

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 262,144-BIT UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**5962-86063**

SHEET 1 OF 16

DSCC FORM 2233
APR 97

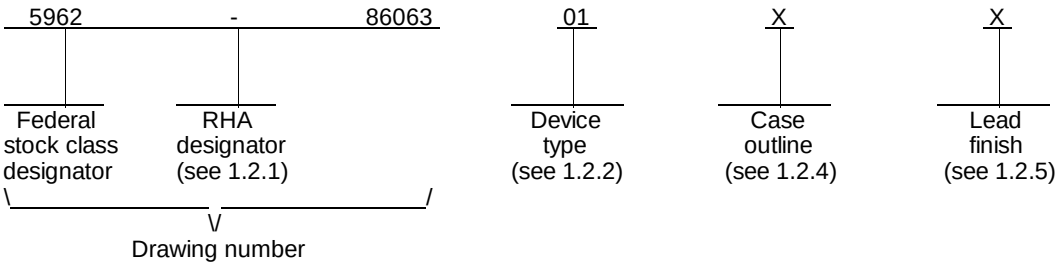
5962-E112-97

1. SCOPE

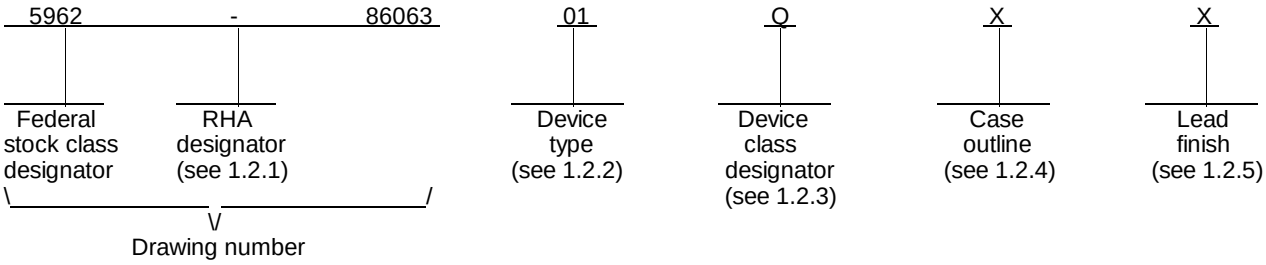
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device class M:



For device classes Q and V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01,11	(see 6.6)	32K x 8-bit UV EPROM	200 ns
02,12	(see 6.6)	32K x 8-bit UV EPROM	250 ns
03,13	(see 6.6)	32K x 8-bit UV EPROM	300 ns
04,14	(see 6.6)	32K x 8-bit UV EPROM	170 ns
05,15	(see 6.6)	32K x 8-bit UV EPROM	150 ns
06,16	(see 6.6)	32K x 8-bit UV EPROM	120 ns
07,17	(see 6.6)	32K x 8-bit UV EPROM	90 ns
08,18	(see 6.6)	32K x 8-bit UV EPROM	70 ns
09,19	(see 6.6)	32K x 8-bit UV EPROM	55 ns
10,20	(see 6.6)	32K x 8-bit UV EPROM	45 ns
21	(see 6.6)	32K x 8-bit UV EPROM	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device class M and Q designators will not be included in the PIN for device types 01 through 10, and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style 1/
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	See figure 1	32	J-lead chip carrier
U	CDIP3-T28 or GDIP4-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +150°C
Input voltages with respect to ground	+6.5 V dc to -0.3 V dc
Output voltages with respect to ground	V_{CC} +0.3 V dc to GND -0.3 V dc
V_{PP} supply voltage with respect to ground	+14.0 V dc to -0.6 V dc
Power dissipation (P_D) 2/	+500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case outlines X, Y, and U	See MIL-STD-1835
Case outline Z	13°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Case operating temperature (T_C)	-55°C to +125°C
Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . . XX percent 3/

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
3/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Truth table. The truth table shall be as specified on figure 3.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical test for each subgroup are described in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6.

3.6.3 Verification of state of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Input load current	I_{LI}	V_{IN} = 0 to 5.5 V	All	1, 2, 3		±10	µA
Output leakage current	I_{LO} 1/	V_{OUT} = 0 to 5.5 V	All	1, 2, 3		±10	µA
Operating current TTL inputs	I_{CC1}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} 8/ 9/ $V_{PP} = V_{CC}$ 0_{0-7} = 0 mA $f = \frac{1}{t_{ACC}}$ maximum	11-20 01-05 06 07 08 09 10 21	1, 2, 3		60 50 65 70 90 115 130 85	mA
Operating current CMOS inputs	I_{CC2}		01,02, 03 04,05 06 07,11-20 08,09 10 21	1, 2, 3		25 40 55 60 90 100 85	mA
Standby current TTL inputs	I_{SB1}	$\overline{CE} = V_{IH}$ V_{CC} = 5.5 V, f = 0 MHz	01-05 06,07, 08,09, 10 11-21	1, 2, 3		3 5 45 25	mA
Standby current CMOS inputs	I_{SB2}		01-07, 08,09, 10 11-21	1, 2, 3		300 45 25	µA mA
V_{PP} read current	I_{PP}	$V_{PP} = V_{CC}$ = 5.5 V	01-10 11-21	1, 2, 3		200 10	µA
Input low voltage (TTL) (±10 percent supply)	V_{IL1} 2/	$V_{PP} = V_{CC}$	All	1, 2, 3	-0.1 3/	0.8	V
Input low voltage (CMOS)	V_{IL2} 2/		All	1, 2, 3	-0.2 3/	0.2	V
Input high voltage (TTL) (±10 percent supply)	V_{IH1} 2/		All	1, 2, 3	2.0	V_{CC} +1.0 3/	V
Input high voltage (CMOS)	V_{IH2} 2/		All	1, 2, 3	V_{CC} -0.2	V_{CC} +0.2 3/	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Output low voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = 5.5 V	All	1, 2, 3		0.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA	All	1, 2, 3	2.4		V
Output short circuit current	I_{OS} 3/ 4/		All	1, 2, 3		-100	mA
V_{PP} read voltage	V_{PPR}		All	1, 2, 3	V_{CC} -0.7	V_{CC}	V
Address to output delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$ 5/ 6/	01,11	9, 10, 11		200	ns
			02,12			250	
			03,13			300	
			04,14			170	
			05,15			150	
			06,16			120	
			07,17			90	
			08,18			70	
			09,19			55	
			10,20			45	
			21			35	
$\overline{CE}$ to output delay	t_{CE}	$\overline{OE} = V_{IL}$ 5/ 6/	01,11	9, 10, 11		200	ns
			02,12			250	
			03,13			300	
			04,14			170	
			05,15			150	
			06,16			120	
			07,17			90	
			08,18			70	
			09,19			55	
			10,20			45	
			21			40	
$\overline{OE}$ to output delay	t_{OE}	$\overline{CE} = V_{IL}$ 5/ 6/	11-13	9, 10, 11		60	ns
			01			75	
			02			100	
			03			150	
			04,05			70	
			14,15			40	
			06,08,16			35	
			07,17			30	
			09,18			25	
			10,19,21			20	
			20			15	
$\overline{OE}$ high to output float	t_{DF} 3/		01	9, 10, 11	0	55	ns
			02,11-13			60	
			03			105	
			04,05			50	
			14,15			40	
			06,08,16			35	
			07,17			30	
			09,18			25	
			10,19			20	
			20,21			15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output hold from addresses $\overline{CE}$ or $\overline{OE}$ (whichever occurred first)	t_{OH} 3/	$\overline{CE} = \overline{OE} = V_{IL}$ 5/ 6/	All	9, 10, 11	0		ns
Input capacitance	C_{IN} 7/	$V_{IN} = 0\ V$ $f = 1\ MHz$ See 4.4.1c	All	4		12	pF
Output capacitance	C_{OUT} 7/	$V_{OUT} = 0\ V$ $f = 1\ MHz$ See 4.4.1c	All	4		14	pF
Functional tests		See 4.4.1e	All	7,8A,8B			

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{LO} with the output under test connected to V_{OUT}.
2/ Tests for all input and control pins.
3/ Guaranteed if not tested.
4/ V_{PP} may be one diode drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and be removed simultaneously or after V_{PP}.
5/ See figures 4 and 5.
6/ Equivalent ac test conditions (actual load conditions vary by tester):
Output load: 1 TTL gate and $C_L = 100$ pF.
Input rise and fall times $\le$ 20 ns.
Input pulse levels: 0.45 V and 2.4 V.
Timing measurement reference levels:
Inputs = 0.8 V and 2.0 V.
Outputs = 0.8 V and 2.0 V.
7/ All pins not being tested are to be grounded.
8/ Devices 11-20 operate at V_{CC} = Maximum, $I_{OUT} = 0$ mA, f = 5 Mhz.
9/ Device 21 operates at V_{CC} = Maximum, $I_{OUT} = 0$ mA, f = 10 Mhz.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

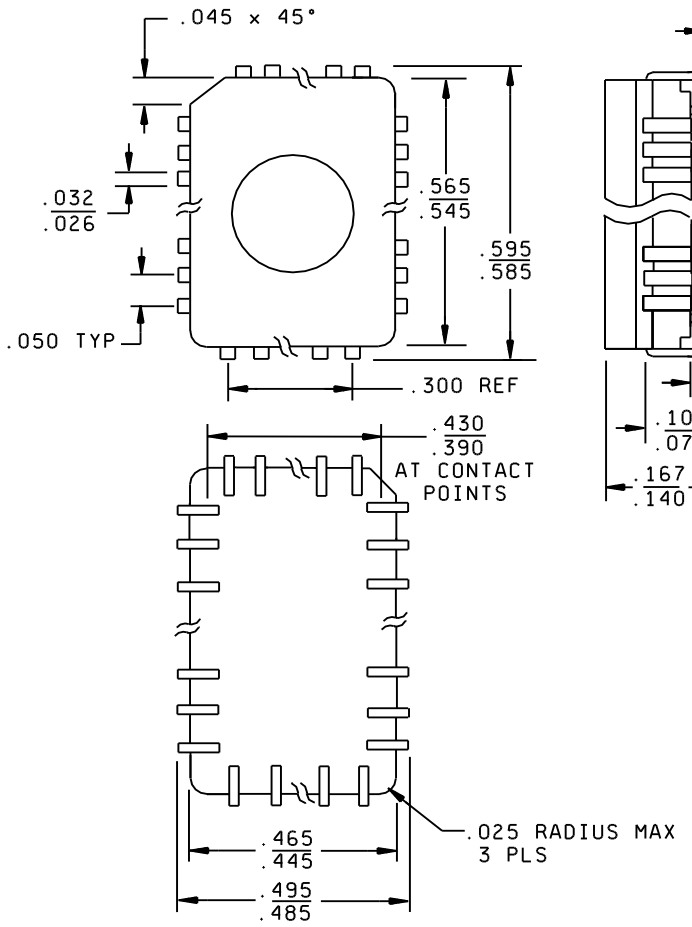
a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

Case Z



Inches	mm
.006	0.15
.010	0.25
.017	0.43
.021	0.53
.025	0.63
.026	0.66
.032	0.81
.035	0.89
.045	1.14
.050	1.27
.073	1.85
.103	2.62
.140	3.56
.167	4.24
.300	7.62
.390	9.90
.430	10.90
.445	11.36
.465	11.83
.485	12.34
.490	12.40
.495	12.67
.530	13.53
.545	13.81
.565	14.46
.585	14.97
.595	15.11

FIGURE 1. 32-lead, windowed ceramic J-leaded chip carrier (JLCC).

Device types	01-21	
Case outlines	X, U	Y, Z
Terminal number	Terminal symbol	
1	V_{PP}	NC
2	A_{12}	V_{PP}
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	O_0	A_0
12	O_1	NC
13	O_2	O_0
14	GND	O_1
15	O_3	O_2
16	O_4	GND
17	O_5	NC
18	O_6	O_3
19	O_7	O_4
20	$\overline{CE}$	O_5
21	A_{10}	O_6
22	$\overline{OE}$	O_7
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	A_{13}	NC
27	A_{14}	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	A_{13}
31	---	A_{14}
32	---	V_{CC}

NC = no connection

FIGURE 2. Terminal connections.

Mode	$\overline{CE}$	$\overline{OE}$	V_{PP} 2/	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X 1/	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP} 2/	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP} 2/	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP} 2/	High Z

1/ X can be either V_{IL} or V_{IH}.

2/ For V_{PP} see 4.6.

FIGURE 3. Truth table.

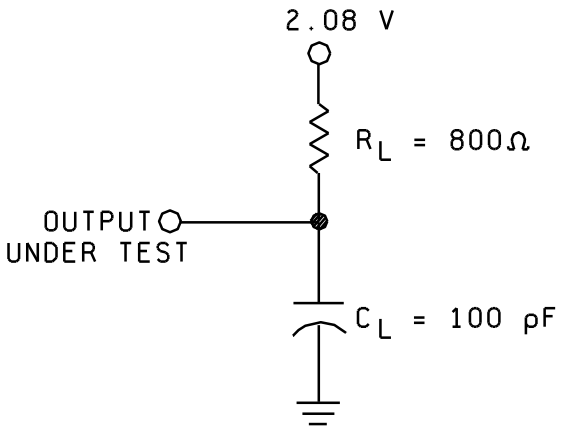
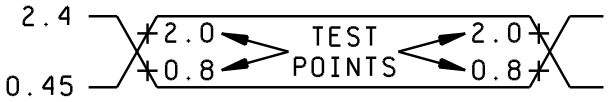


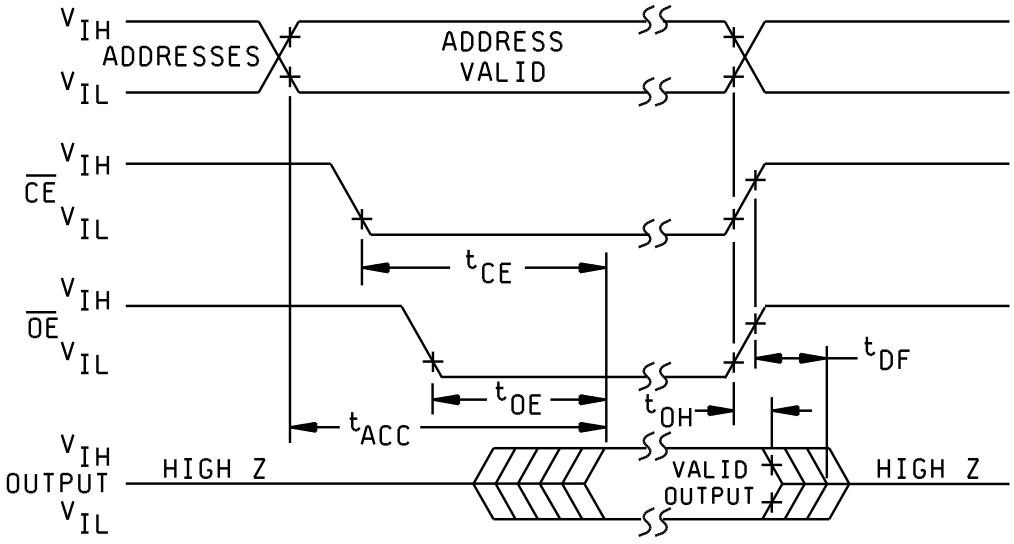
FIGURE 4. Output load circuit.

AC TESTING INPUT, OUTPUT WAVEFORM



AC TESTING: INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC "1" AND 0.8 V FOR A LOGIC "0".

AC WAVEFORMS



NOTES:
1. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

FIGURE 5. Switching waveforms.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005 Table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9	1*, 2, 3, 7*, 8A, 8B, 9	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4***, 7, 8A, 8B, 9, 10**, 11**	1, 2, 3, 4***, 7, 8A, 8B, 9, 10**, 11**	1, 2, 3, 4***, 7, 8A, 8B, 9, 10**, 11**
8	Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ (**) indicates that subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.
3/ (***) see 4.4.1c.
4/ Any subgroups at the same temperature may be combined when using a multifunction tester.
5/ Subgroups 7 and 8 shall consist of verifying the applicable data pattern, see 4.4.1d.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall include verification of the pattern specified in 4.4.1d.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE IIB. Delta limits at +25° C.

Parameter 1/	Device types
I_{SB2}	All
I_{LI}	± 10%
I_{LO}	± 10%

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply CenterColumbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DSCC-VA.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-06-11

Approved sources of supply for SMD 5962-86063 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standardized military drawing 1/ PIN	Vendor CAGE number	Vendor similar 3/ PIN
5962-8606301XA	34649 4/ 01295	MD27C256-20/B SMJ27C256-20JM
5962-8606301YA	34649 4/	MR27C256-20/B
5962-8606301ZX	2/	AT27C256R-20KM/883
5962-8606301UX	2/	WS27C256L-20TMB
5962-8606302XA	34649 4/ 01295	MD27C256-25/B SMJ27C256-25JM
5962-8606302YA	34649 4/	MR27C256-25/B
5962-8606302ZX	2/	AT27C256R-25KM/883
5962-8606303XA	01295	SMJ27C256-30JM
5962-8606303YX	2/	AT27C256R-30LM/883
5962-8606303ZX	2/	AT27C256R-30KM/883
5962-8606304XA	34649 4/ 01295	MD27C256-17/B SMJ27C256-17JM
5962-8606304YA	34649 4/	MR27C256-17/B
5962-8606304ZX	2/	AT27C256R-17KM/883
5962-8606304UX	2/	WS27C256L-17TMB
5962-8606305XA	66579 34649 4/ 01295	WS27C256L-15DMB MD27C256-15/B SMJ27C256-15JM
5962-8606305YC	66579 34649 4/	WS27C256L-15CMB MD27C256-15/B
5962-8606305ZX	2/	
5962-8606305UA	66579	WS27C256L-15TMB
5962-8606306XA	66579	WS27C256L-12DMB
5962-8606306YC	66579	WS27C256L-12CMB
5962-8606306ZX	2/	AT27C256R-12KM/883
5962-8606307XX	2/	AT27C256R-90DM/883
5962-8606307YX	2/	AT27C256R-90LM/883
5962-8606307ZX	2/	AT27C256R-90KM/883

See footnote at end of table.

Standardized military drawing 1/ PIN	Vendor CAGE number	Vendor similar 3/ PIN
5962-8606308XA	66579	WS57C256F-70DMB
5962-8606308YC	66579	WS57C256F-70CMB
5962-8606308ZX	2/	AT27C256R-70KM/883
5962-8606309XA	66579	WS57C256F-55DMB
5962-8606309YA	66579	WS57C256F-55CMB
5962-8606309UA	66579	WS57C256F-55TMB
5962-8606310XA	66579	WS57C256F-45DMB
5962-8606310YA	66579	WS57C256F-45CMB
5962-8606310UA	66579	WS57C256F-45TMB
5962-8606311QXA	65786	CY27C256A-200WMB
5962-8606311QYA	65786	CY27C256A-200QMB
5962-8606312QXA	65786	CY27C256A-250WMB
5962-8606312QYA	65786	CY27C256A-250QMB
5962-8606313QXA	65786	CY27C256A-300WMB
5962-8606313QYA	65786	CY27C256A-300QMB
5962-8606314QXA	65786	CY27C256A-170WMB
5962-8606314QYA	65786	CY27C256A-170QMB
5962-8606315QXA	65786	CY27C256A-150WMB
5962-8606315QYA	65786	CY27C256A-150QMB
5962-8606316QXA	65786	CY27C256A-120WMB
5962-8606316QYA	65786	CY27C256A-120QMB
5962-8606317QXA	65786	CY27C256A-90WMB
5962-8606317QYA	65786	CY27C256A-90QMB
5962-8606318QXA	65786	CY27C256A-70WMB
5962-8606318QYA	65786	CY27C256A-70QMB
5962-8606319QXA	65786	CY27C256A-55WMB
5962-8606319QYA	65786	CY27C256A-55QMB
5962-8606320QXA	65786	CY27C256A-45WMB
5962-8606320QYA	65786	CY27C256A-45QMB
5962-8606321QXA	65786	CY27H256A-35WMB
5962-8606321QYA	65786	CY27H256A-35QMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ No longer available from an approved source of supply.

3/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

4/ Vendor has announced end-of-life for these devices. Please refer to the latest revision of MIL-HDBK-103 for details.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland TX 79711-0448
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051 Point of contact: 5000 West Chandler Boulevard Chandler, AZ 85226-3699
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134
66579	Waferscale Integration, Incorporated 47280 Kato Road Fremont, CA 94538

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.