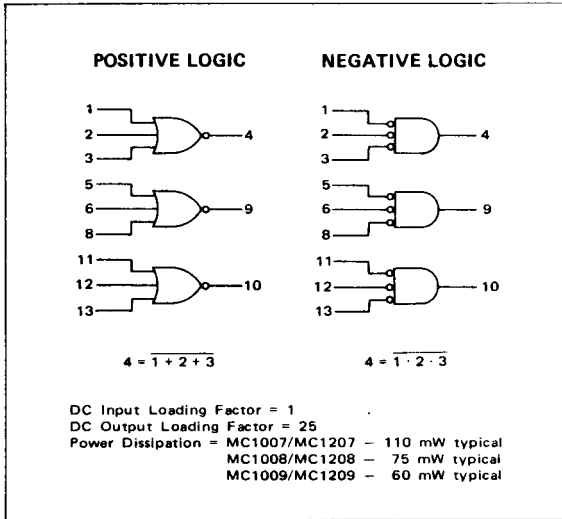


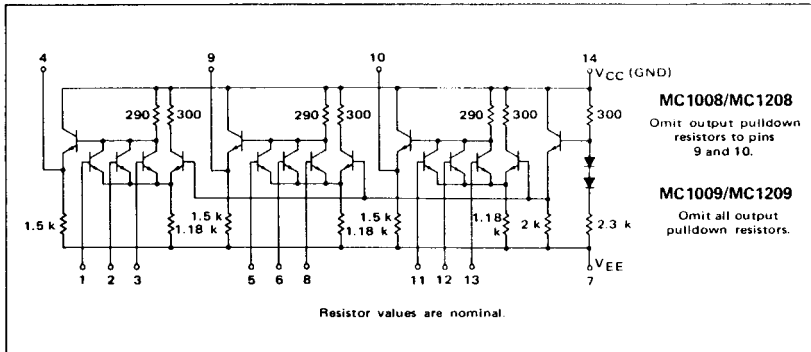
MC1007 thru MC1009
MC1207 thru MC1209

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

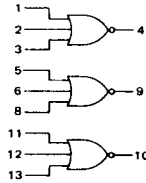
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



MC1007/MC1207 CIRCUIT SCHEMATIC



MC1007 thru MC1009, MC1207 thru MC1209 (continued)



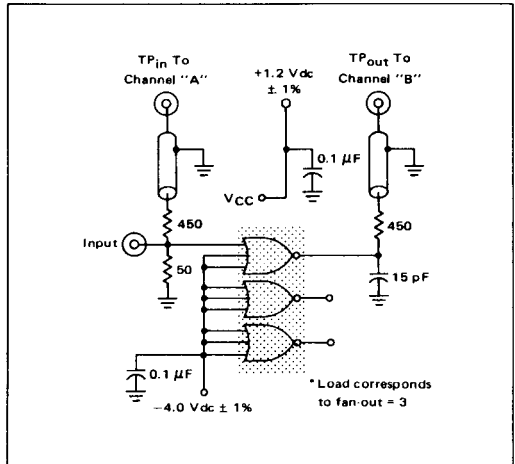
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 k ohm resistor to VEE.

Characteristic	Symbol	Pin Under Test	MC1207-1209 Test Limits						MC1007-1009 Test Limits							
			-55°C		+25°C		+125°C		0°C		+25°C		+75°C		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	7	-	-	-	30	-	-	mAdc	-	-	-	30	-	-	mAdc
			-	-	-	20	-	-		-	-	-	20	-	-	
			-	-	-	16	-	-		-	-	-	16	-	-	
Input Current	I_{in}	1 2 3	-	-	-	100	-	-	μ Adc	-	-	-	100	-	-	μ Adc
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μ Adc	-	-	-	0.2	-	1.0	μ Adc
"NOR" Logical "1" Output Voltage	V_{OH1}	4	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	4	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times Propagation Delay (Fan-Out = 3)	t_{1-4-}	4	Typ	Max	Typ	Max	Typ	Max	ns	Typ	Max	Typ	Max	Typ	Max	ns
			4.0	7.5	4.0	7.5	6.0	9.0		4.0	7.5	4.0	7.5	5.0	8.5	
			4.0	7.0	4.0	7.0	6.0	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
			18	-	18	-	22	-		18	-	18	-	20	-	
(Fan-Out = 15)	t_{1-4-}	4	5.0	-	5.0	-	9.0	-	5.0	-	5.0	-	7.0	-		
Rise Time (Fan-Out = 3)			t_{4+}	5.0	7.5	5.0	7.5	6.0	9.0	5.0	7.5	5.0	7.5	5.5	8.0	
Fall Time (Fan-Out = 3)	t_{4-}	4	6.0	8.5	6.0	8.0	7.0	10	6.0	8.0	6.0	8.0	6.0	9.0		

* Individually test each input using the pin connections shown.
 V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C

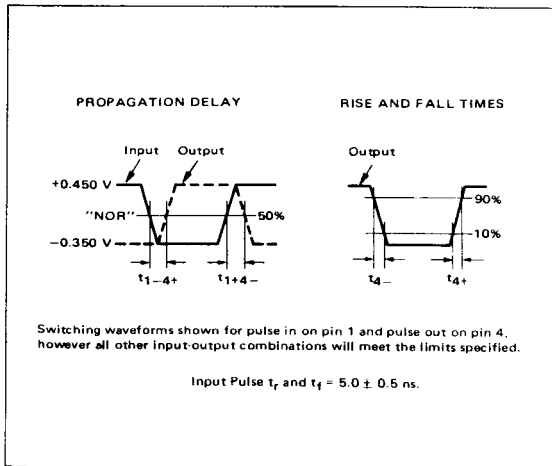


MC1207-1209
MC1007-1009

@Test Temperature
-55°C
+25°C
+125°C
0°C
+25°C
+75°C

		TEST VOLTAGE/CURRENT VALUES					mAdc
		Vdc ± 1.0%					
		V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	I _L	
		-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
		-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
		-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5	
		-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
		-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
		-5.2 to -1.260	-0.950 to 0.615	-	-5.2	-2.5	

		TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					V _{CC} (Gnd)
Characteristic	Symbol	Pin Under Test	V _{IL min} to V _{IL max}	V _{IH min} to V _{IH max}	V _{IH max}	V _{EE}	
Power Supply Drain Current MC1207, MC1007 MC1208, MC1008 MC1209, MC1009	I _E	7 ↓	-	-	-	1, 2, 3, 5, 6, 7, 8, 11, 12, 13	↓ 14
Input Current	I _{in}	1 2 3	-	-	1 2 3	2, 3, 5, 6, 7, 8, 11, 12, 13 1, 3, 5, 6, 7, 8, 11, 12, 13 1, 2, 5, 6, 7, 8, 11, 12, 13	↓ ↓ ↓ 14
Input Leakage Current	I _{IL}	Inputs*	-	-	-	1, 2, 3, 5, 6, 7, 8, 11, 12, 13	↓ 14
NOR* Logical '1' Output Voltage	V _{OH1}	4 ↓	1 2 3	-	-	2, 3, 5, 6, 7, 8, 11, 12, 13 1, 3, 5, 6, 7, 8, 11, 12, 13 1, 2, 5, 6, 7, 8, 11, 12, 13	↓ ↓ ↓ 14
NOR* Logical '0' Output Voltage	V _{OL}	4 ↓	-	1 2 3	-	2, 3, 5, 6, 7, 8, 11, 12, 13 1, 3, 5, 6, 7, 8, 11, 12, 13 1, 2, 5, 6, 7, 8, 11, 12, 13	↓ ↓ ↓ 14
Switching Times			Pulse In	Pulse Out		V _{EE} = -4.0 Vdc	(+1.2 V)
Propagation Delay (Fan-Out = 3)	t ₁₋₄₊ t ₁₋₄₋	4 ↑	↓	↑	-	2, 3, 5, 6, 7, 8, 11, 12, 13	↓ ↓ 14
(Fan-Out = 15)	t ₁₋₄₊ t ₁₋₄₋	4 ↑	↓	↑	-	2, 3, 5, 6, 7, 8, 11, 12, 13	↓ ↓ 14
Rise Time (Fan-Out = 3)	t ₄₊	4 ↓	↓	↑	-	2, 3, 5, 6, 7, 8, 11, 12, 13	↓ 14
Fall Time (Fan-Out = 3)	t ₄₋	4 ↓	↓	↑	-	2, 3, 5, 6, 7, 8, 11, 12, 13	↓ 14



SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

The MC1007-1009/MC1207-1209 triple 3-input gates provide NOR outputs only, due to the pin limitation of the 14-lead package. The three options on the emitter follower pull-down resistors, as on all of the basic gates, provide a significant power savings when the wired-OR feature is utilized. The power dissipation of additional emitter-follower resistors and additional gates to perform the OR function is

eliminated. By making liberal use of the wired-OR feature, power dissipation in a logic system may be reduced by one-half. If fast propagation delay time through a logic chain is required, an additional gate propagation delay of 4.0 to 5.0 ns is saved each time the wired-OR option is employed. Shown below are two examples of an MC1008/MC1208 with the outputs wired together.

