CY7C1324A

128K x 18 Synchronous Flow-thru Burst SRAM

Features

- **Fast access times: 7.5 and 8 ns**
- **Fast clock speed: 117 and 100 MHz**
- **Provide high-performance 2-1-1-1 access rate**
- **Fast $\overline{OE}$ access times: 4.0 ns**
- **3.3V –5% and +10% power supply**
- **2.5V or 3.3V I/O supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SSQ} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Address, data and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **Available in 100-pin TQFP package**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1324A SRAM integrates 131,072 x 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}$), depth-expansion Chip Enables ($\overline{CE2}$ and CE2), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{WEL}$, $\overline{WEH}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

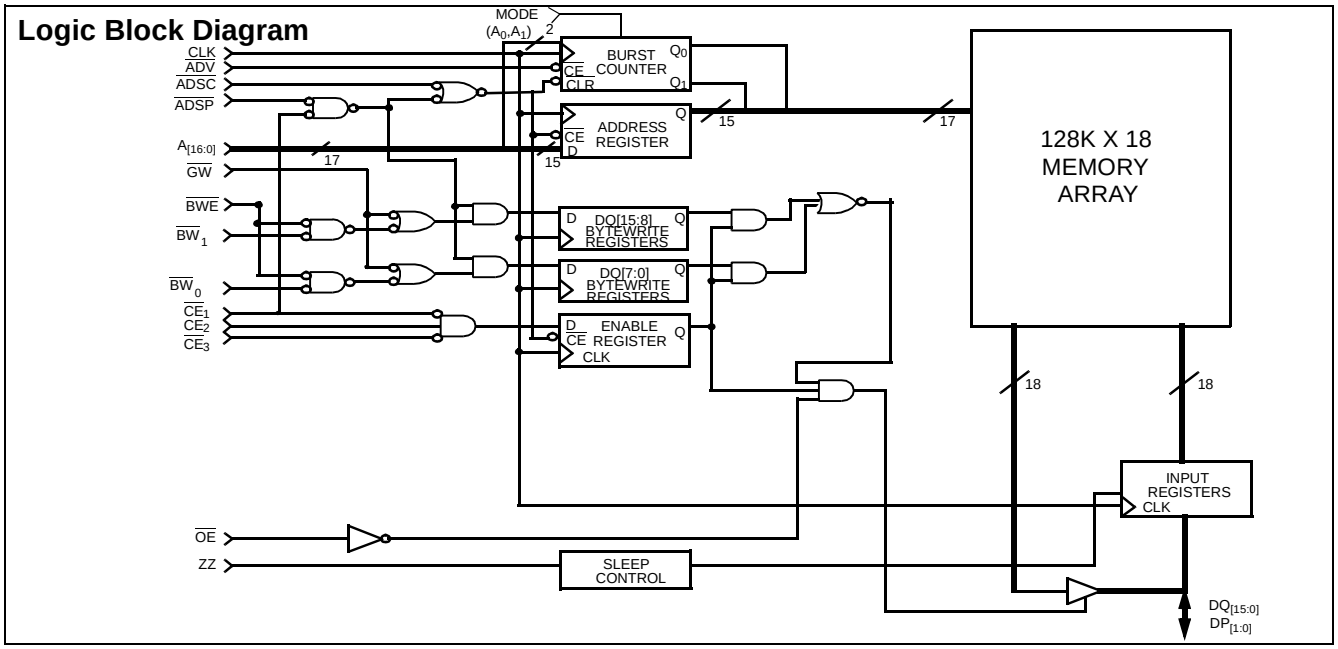
Asynchronous inputs include the Output Enable ($\overline{OE}$) and Burst Mode Control (MODE), and Sleep Mode Control (ZZ). The data outputs (DQ), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. $\overline{WEL}$ controls DQ1–DQ8 and DQP1. $\overline{WEH}$ controls DQ9–DQ16 and DQP2. $\overline{WEL}$ and $\overline{WEH}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written.

The CY7C1324A operates from a +3.3V power supply and all outputs operate on a +2.5V supply. All inputs and outputs are JEDEC standard JESD8-5 compatible. The device is ideally suited for 486, Pentium®, 680x0, and PowerPC™ systems and for systems that benefit from a wide synchronous data bus.

Logic Block Diagram



Note:

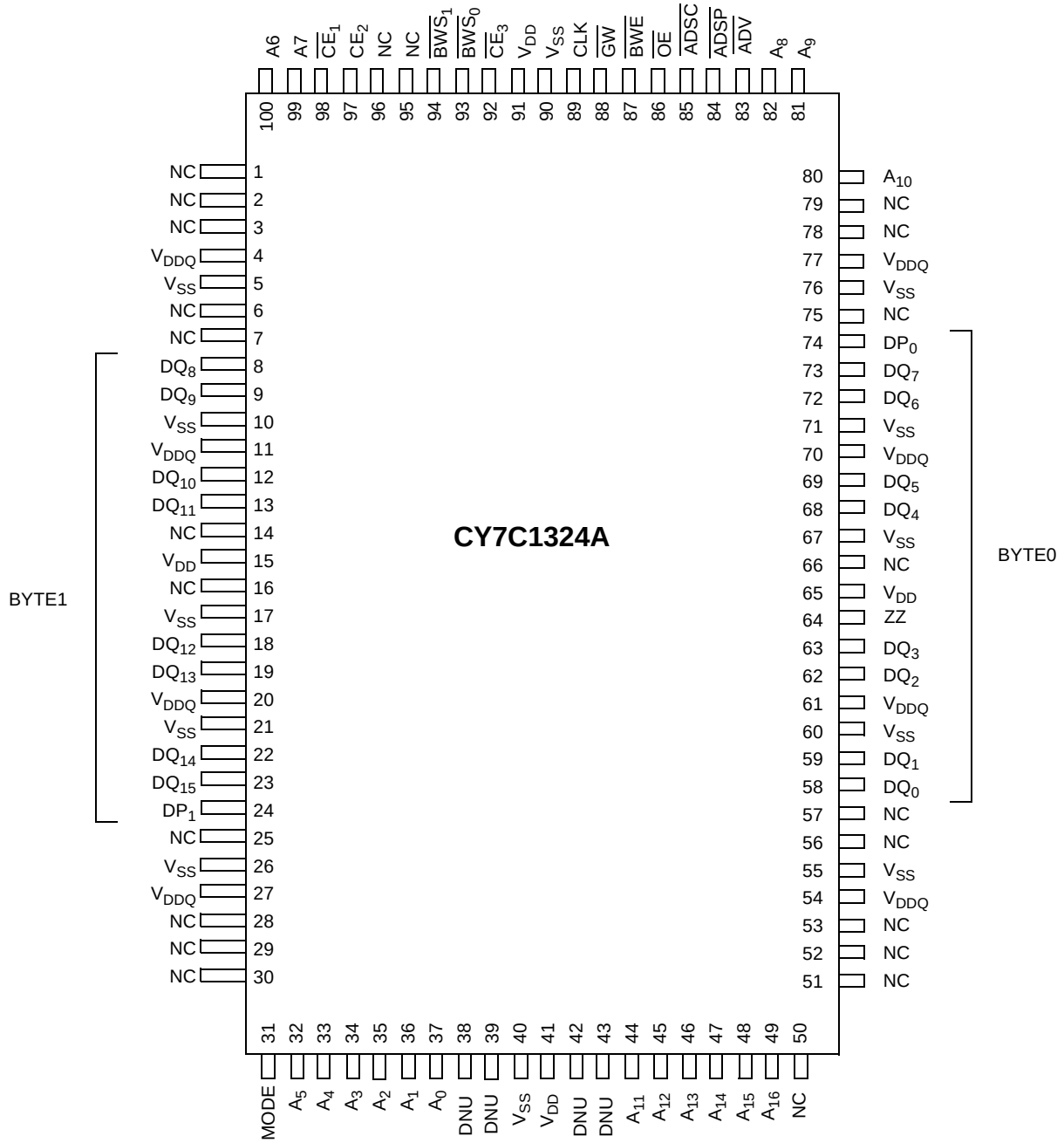
1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions, and timing diagrams for detailed information.

Selection Guide

	7C1324A-117	7C1324A-100	Unit
Maximum Access Time	7.5	8	ns
Maximum Operating Current	370	320	mA
Maximum CMOS Standby Current	10	10	mA

Pin Configurations

100-lead TQFP



Pin Descriptions

QFP Pins	Pin Name	Type	Description
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44, 49	A0–A16	Input-Synchronous	**Addresses**: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
93, 94	$\overline{BWS}_{[1:0]}$	Input-Synchronous	**Byte Write Enables**: A byte write enable is LOW for a Write cycle and HIGH for a Read cycle. $\overline{WEL}$ controls DQ1–DQ8 and DQP1. $\overline{WEH}$ controls DQ9–DQ16 and DQP2. Data I/O are high-impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW.
87	$\overline{BWE}$	Input-Synchronous	**Write Enable**: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	**Global Write**: This active LOW input allows a full 18-bit Write to occur independent of the $\overline{BWE}$ and $\overline{WEn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
89	CLK	Input-Synchronous	**Clock**: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
98	$\overline{CE}$	Input-Synchronous	**Chip Enable**: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.
92	$\overline{CE2}$	Input-Synchronous	**Chip Enable**: This active LOW input is used to enable the device.
97	CE2	input-Synchronous	**Chip Enable**: This active HIGH input is used to enable the device.
86	$\overline{OE}$	Input	**Output Enable**: This active LOW asynchronous input enables the data output drivers.
83	$\overline{ADV}$	Input-Synchronous	**Address Advance**: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
84	$\overline{ADSP}$	Input-Synchronous	**Address Status Processor**: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a Read cycle is initiated using the new address.
85	$\overline{ADSC}$	Input-Synchronous	**Address Status Controller**: This active LOW input causes device to be deselected or selected along with new external address to be registered. A Read or Write cycle is initiated depending upon write control inputs.
31	MODE	Input-Static	**Mode**: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
64	ZZ	Input-Asynchronous	**Snooze**: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/Output	**Data Inputs/Outputs**: Low Byte is DQ1–DQ8. HIgh Byte is DQ9–DQ16. Input data must meet setup and hold times around the rising edge of CLK.
74, 24	DQP1, DQP2	Input/Output	**Parity Inputs/Outputs**: DQP1 is parity bit for DQ1–DQ8 and DQP2 is parity bit for DQ9–DQ16.
15, 41,65, 91	V_{CC}	Supply	**Power Supply**: +3.3V –5% and +10%
17, 40, 67, 90	V_{SS}	Ground	**Ground**: GND
4, 11, 20, 27, 54, 61, 70, 77	V_{CCQ}	I/O Supply	**Output Buffer Supply**: +2.5V (from 2.375V to V_{CC})
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	I/O Ground	**Output Buffer Ground**: GND
1–3, 6, 7, 14, 16, 25, 28-30, 38, 39, 42, 43, 51-53, 56, 57, 66, 75, 78, 79, 80, 95, 96	NC	–	**No Connect**: These signals are not internally connected.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Notes:

2. X means "Don't Care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means [$\overline{BWE}$ + $\overline{WEL}$*$\overline{WEH}$]*$\overline{GW}$ equals LOW. $\overline{WRITE}$ = H means [$\overline{BWE}$ + $\overline{WEL}$*WEH]*GW equals HIGH.
3. WEL enables write to DQ1–DQ8 and DQP1. $\overline{WEH}$ enables write to DQ9–DQ16 and DQP2.
4. All inputs except $\overline{OE}$ must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. ADSP LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting $\overline{WRITE}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

Partial Truth Table for Read/Write

FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{WEH}$	$\overline{WEL}$
READ	H	H	X	X
READ	H	L	H	H
WRITE one byte	H	L	L	H
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS}.....–0.5V to +4.6V

V_{IN} .....–0.5V to +V_{CC}+0.5V

Storage Temperature (plastic) ..... –55°C to +125°C

Junction Temperature ..... +125°C

Power Dissipation..... 1.4W

Short Circuit Output Current 100mA

Operating Range

Range	Ambient Temperature[9]	V_{CC}[10,11]
Com'l	0°C to +70°C	3.3V –5%/+10%

Electrical Characteristics Over the Operating Range[12]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage[13, 14]	Data Inputs (DQxx)	1.7	V_{CC}+0.3	
V_{IH}		All other	1.7	4.6	V
V_{II}	Input Low (Logic 0) Voltage[13, 14]		–0.3	0.7	V
IL_I	Input Leakage Current[15]	$0V \le V_{IN} \le V_{CC}$	–2	2	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	–2	2	µA
V_{OH}	Output High Voltage[13, 16]	I_{OH} = –2.0 mA	1.7		V
V_{OL}	Output Low Voltage[13, 16]	I_{OL} = 2.0 mA		0.7	V
V_{CC}	Supply Voltage[13]		3.135	3.6	V
V_{CCQ}	I/O Supply		2.375	V_{CC}	V

Parameter	Description	Conditions	Typ.	-7 117 MHz	-8 100 MHz	Unit
I_{CC}	Power Supply Current: Operating[17, 18, 20]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ Min.; V_{CC} = Max.; outputs open	150	370	320	mA
I_{SB2}	CMOS Standby[18, 20]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	5	10	10	mA
I_{SB3}	TTL Standby[18, 20]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	10	20	20	mA
I_{SB4}	Clock Running[18, 20]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = Max.; CLK cycle time $\ge t_{KC}$ Min.	40	80	70	mA

Notes:

9. T_A is the case temperature.
10. Please refer to waveform (c)
11. Power supply ramp up should be monotonic.
12. Values in table are associated with the operating frequencies listed.
13. All voltages referenced to V_{SS} (GND).
14. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$.
    Undershoot:$V_{IL} \le -2.0V$ for $t \le t_{KC}/2$.
15. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
16. AC I/O curves are available upon request.
17. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
18. "Device Deselected" means the device is in Power-down mode as defined in the truth table. "Device Selected" means the device is active.
19. Overshoot: VIH(AC) < VDD + 1.5V for t < tTCYC/2; undershoot: VIL(AC) < 0.5V for t < tTCYC/2; power-up: VIH < 2.6V and VDD < 2.4V and VDDQ < 1.4V for t < 200 ms.
20. Typical values are measured at 3.3V, 25°C and 20-ns cycle time.

Thermal Consideration

Parameter	Description	Conditions	TQFP Typ.	Unit
Θ_{JA}	Thermal Resistance–Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch four-layer PCB	25	°C/W
Θ_{JC}	Thermal Resistance–Junction to Case		9	°C/W

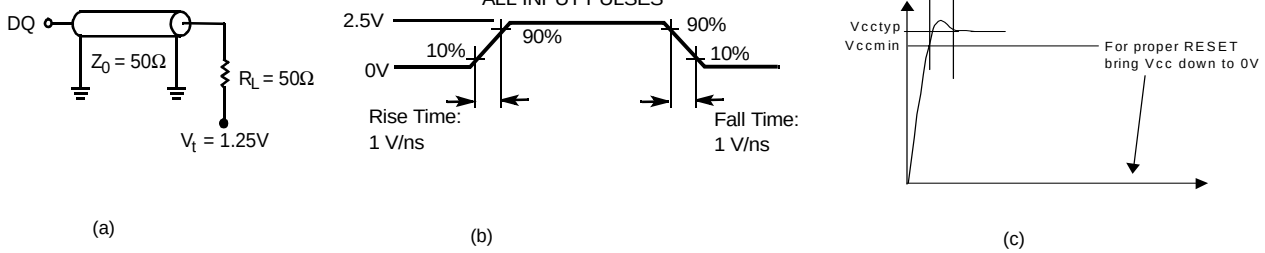
Capacitance

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance[2]	T_A = 25°C, f = 1 MHz, V_{CC}= 3.3V	4	5	pF
C_O	Input/Output Capacitance (DQ)[2]		7	8	pF

Typical Output Buffer Characteristics

Output High Voltage	Pull-up Current		Output Low Voltage	Pull-down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.	V_{OL} (V)	I_{OL} (mA) Min.	I_{OL} (mA) Max.
–0.5	–38	–105	–0.5	0	0
0	–38	–105	0	0	0
0.8	–38	–105	0.4	10	20
1.25	–26	–83	0.8	20	40
1.5	–20	–70	1.25	31	63
2.3	0	–30	1.6	40	80
2.7	0	–10	2.8	40	80
2.9	0	0	3.2	40	80
3.4	0	0	3.4	40	80

AC Test Loads and Waveforms[19]



(a) (b) (c)

Switching Characteristics Over the Operating Range [3]

Parameter	Description	-117		-100		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	8.5		10		ns
t_{CH}	Clock HIGH	3.0		4.0		ns
t_{CL}	Clock LOW	3.0		4.0		ns
t_{AS}	Address Set-up Before CLK Rise	1.5		2.0		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t_{CDV}	Data Output Valid After CLK Rise		7.5		8.0	ns
t_{DOH}	Data Output Hold After CLK Rise	2.0		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-up Before CLK Rise	1.5		2.0		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		ns
t_{WES}	$\overline{BWS}_{[1:0]}$, $\overline{GW}$,$\overline{BWE}$ Set-up Before CLK Rise	1.5		2.0		ns
t_{WEH}	$\overline{BWS}_{[1:0]}$, $\overline{GW}$,$\overline{BWE}$ Hold After CLK Rise	0.5		0.5		ns

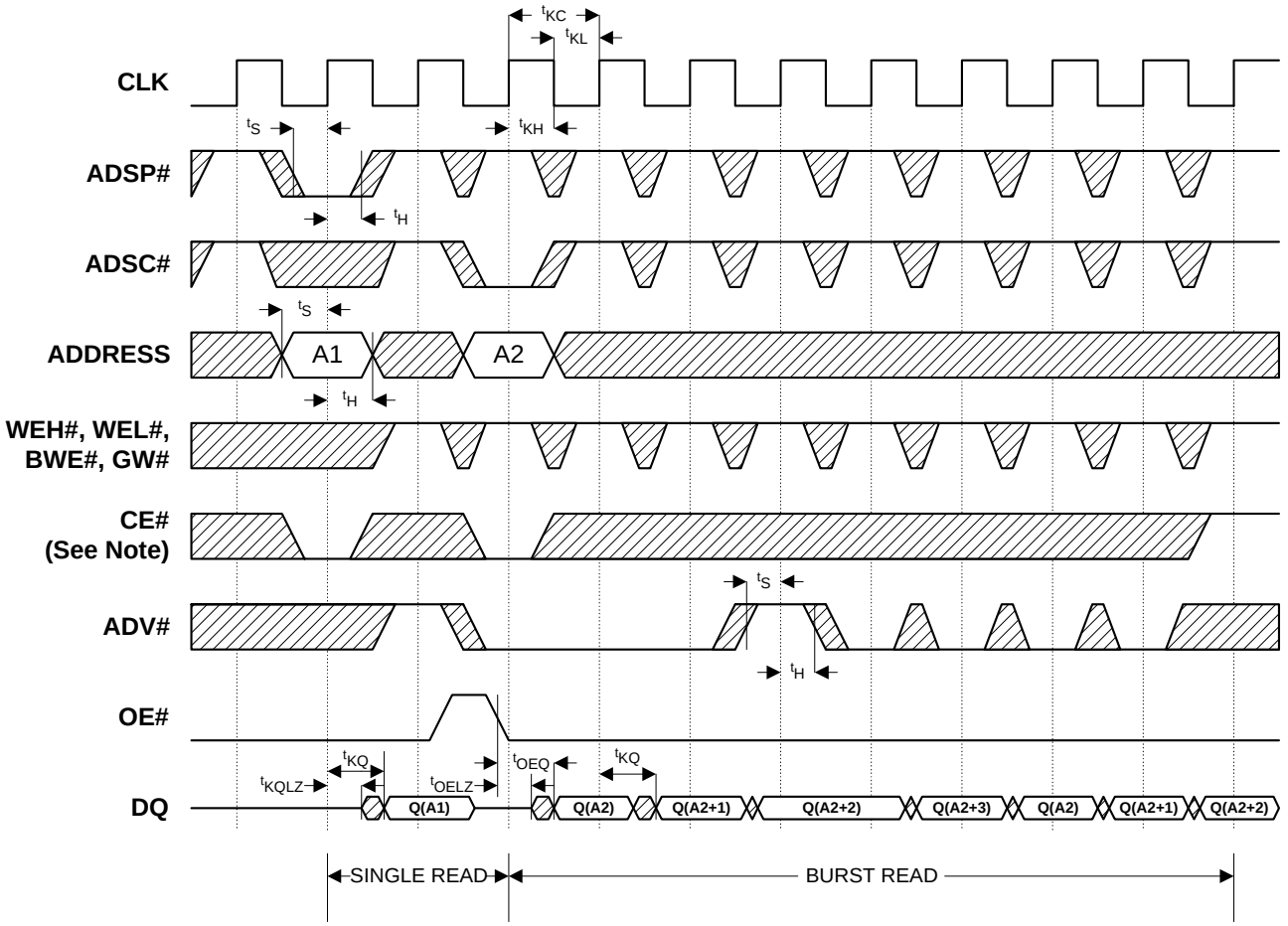
Switching Characteristics Over the Operating Range (continued)[3]

Parameter	Description	-117		-100		Unit
		Min.	Max.	Min.	Max.	
t_{ADVS}	$\overline{ADV}$ Set-up Before CLK Rise	1.5		2.0		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		ns
t_{DS}	Data Input Set-up Before CLK Rise	1.5		2.0		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t_{CES}	Chip Enable Set-up	1.5		2.0		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		ns
t_{CHZ}	Clock to High-Z[4,5]	2	3.5	2	3.5	ns
t_{CLZ}	Clock to Low-Z[4,5]	0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[4,6]		3.5		3.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[4,6]	0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		4.0		4.0	ns

Notes:
2. This parameter is sampled.

Timing Diagrams

Read Timing[7]

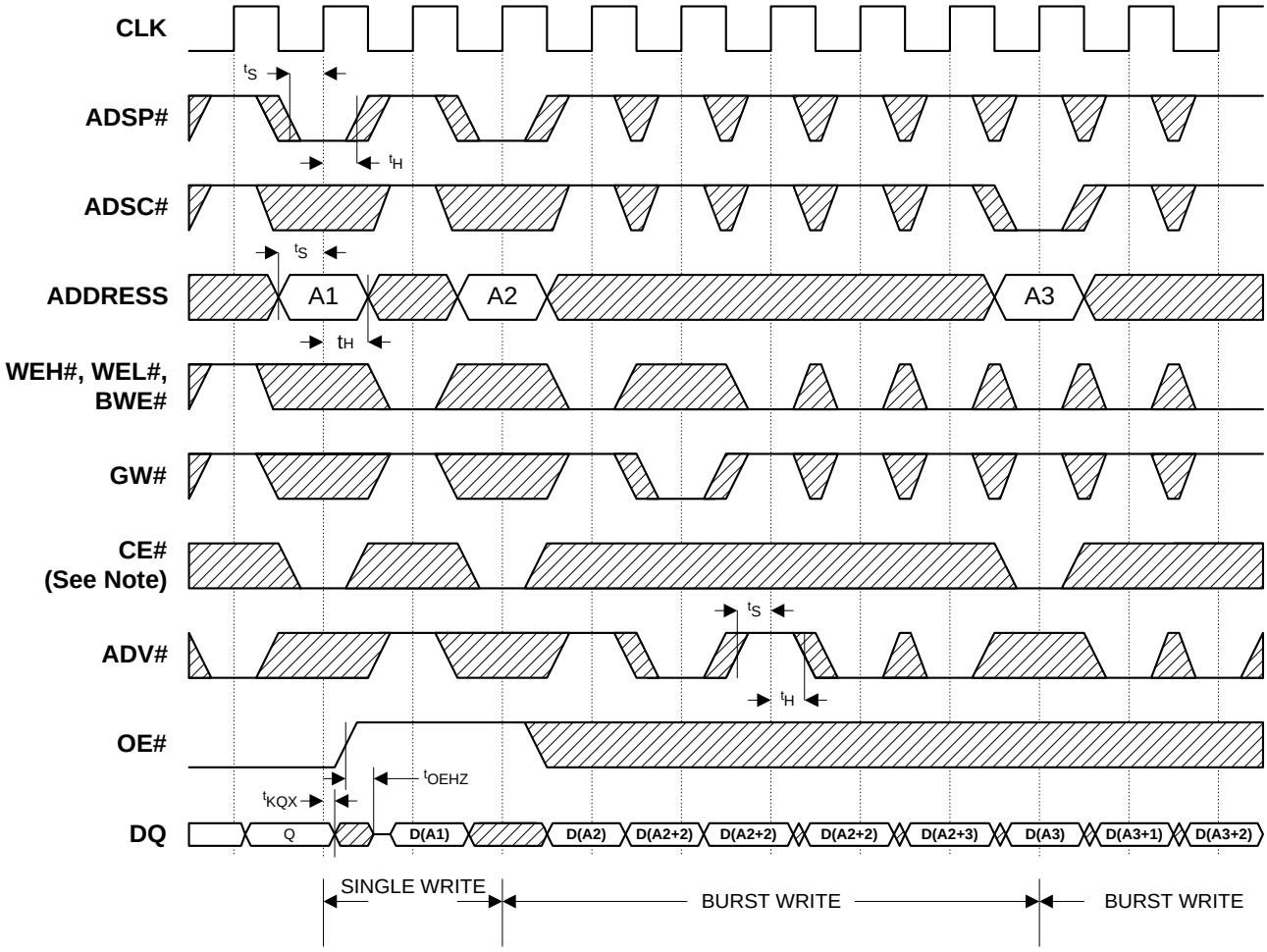


Timing Diagrams(continued)

Notes:

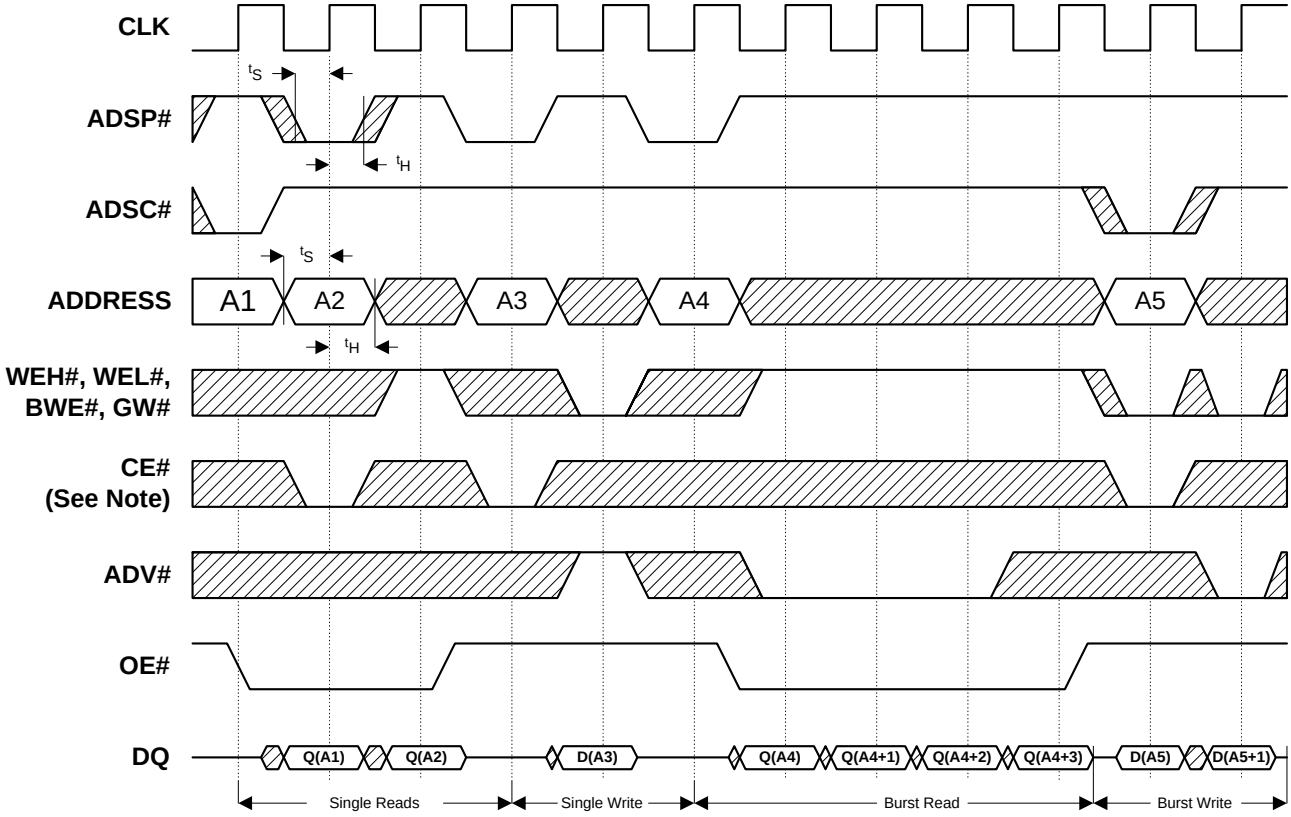
3. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0 to 2.5V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
4. t_{CHZ}, t_{CLZ}, t_{EOHZ}, and t_{EOLZ} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
5. At any given voltage and temperature, t_{CHZ} (max.) is less than t_{CLZ} (min.).
6. This parameter is sampled and not 100% tested.
7. CE active in this timing diagram means that all Chip Enables $\overline{CE}$, $\overline{CE2}$, and CE2 are active.

Write Timing[7]



Timing Diagrams(continued)

Read/Write Timing[7]

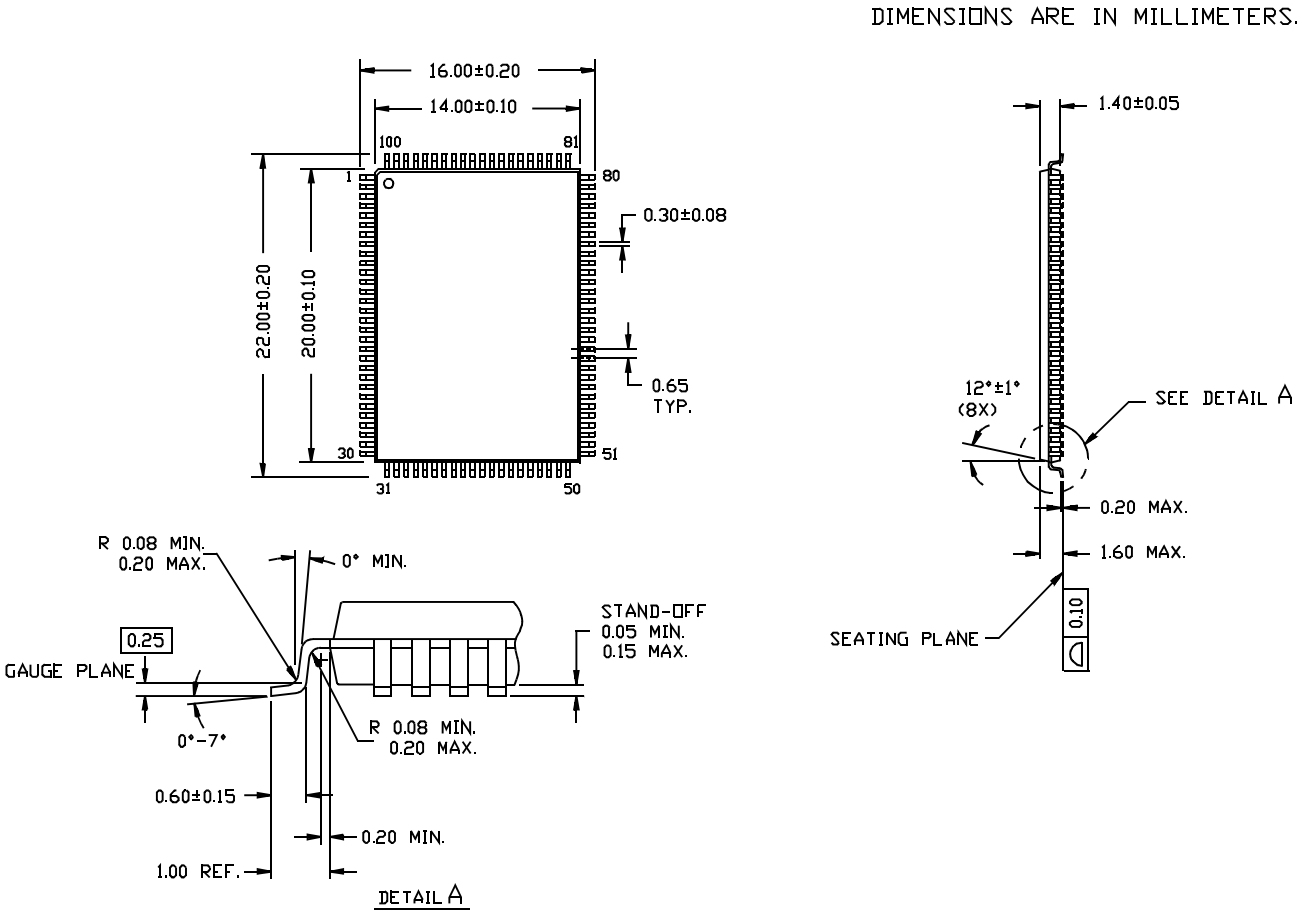


Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
117	CY7C1324A-117AC	A101	100-lead Thin Quad Flat Pack	Commercial
100	CY7C1324A-100AC	A101	100-lead Thin Quad Flat Pack	Commercial

Package Diagrams

100-lead Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



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Document History Page

Document Title: CY7C1324A 128K x 18 Synchronous Flow-thru Burst SRAM Document Number: 38-05325				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118253	10/14/02	HGK	New Data Sheet
*A	123142	01/18/03	RBI	Add Power up Requirements to Operating Conditions Information