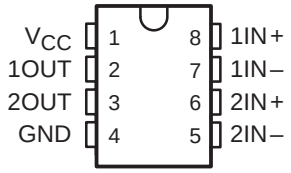
SLLS015B – FEBRUARY 1986 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and -423-B**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28 With External Components**
- **Meets Federal Standards 1020 and 1030**
- **Built-in 5-MHz Low-Pass Filter**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **8-Pin Dual-in-Line Package**
- **Pinout Compatible With the μA9637 and μA9639**

D OR P PACKAGE
(TOP VIEW)



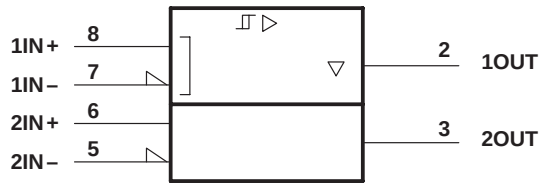
THE SN75146 IS NOT RECOMMENDED FOR NEW DESIGNS.

description

The SN75146 is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and -423-B. The receiver is designed to have a constant impedance with input voltages of ±3 V to ±25 V allowing it to meet the requirements of EIA/TIA-232-E and ITU recommendation V.28 with the addition of an external bias resistor. This receiver is designed for low-speed operation below 355 kHz and has a built-in 5-MHz low-pass filter to attenuate high-frequency noise. The inputs are compatible with either a single-ended or a differential line system and the outputs are TTL compatible. This device operates from a single 5-V power supply and is supplied in both the 8-pin dual-in-line and small-outline packages.

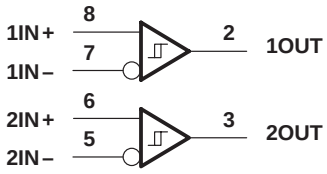
The SN75146 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



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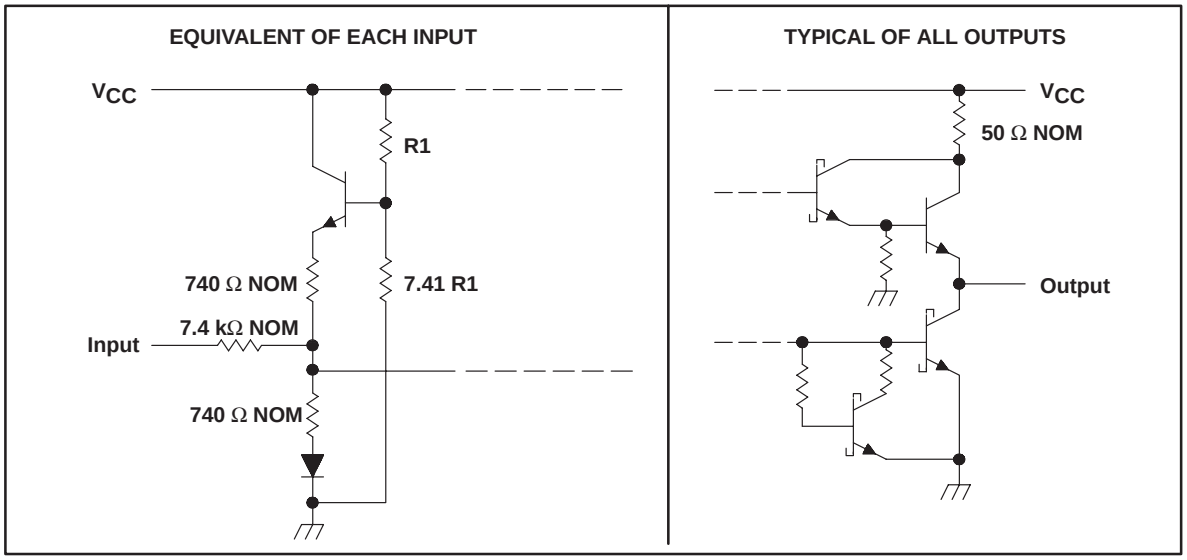
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage, V_I . . . . . ±25 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±25 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to 5.5 V
Low-level output current, I_{OL} . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

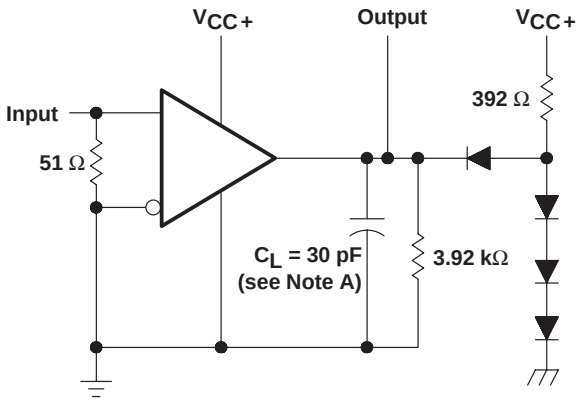
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT}	Threshold input voltage (V_{IT+} and V_{IT-})			−0.2‡		0.2	V
		See Note 3		−0.4‡		0.4	
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)			70			mV
V_{IB}	Input bias voltage	I_I = 0		2		2.4	V
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
r_i	Input resistance	V_I = 3 V to 25 V or V_I = −3 V to −25 V, See Note 4		6	7.8	10.5	kΩ
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 5	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. r_i is defined by $\Delta V_I/\Delta I_I$.
5. The input not under test is grounded.

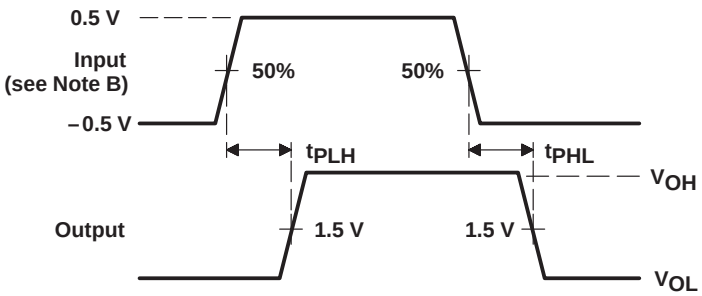
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	See Figure 1	100	150	300	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	150	300	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 300 kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

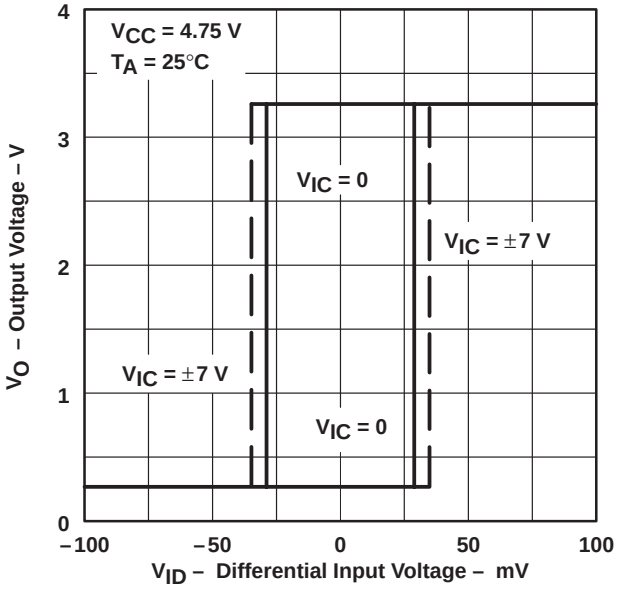


Figure 2

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

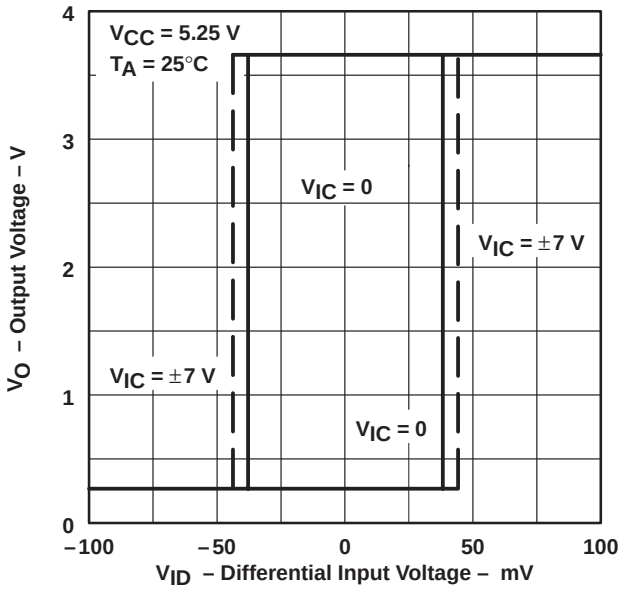
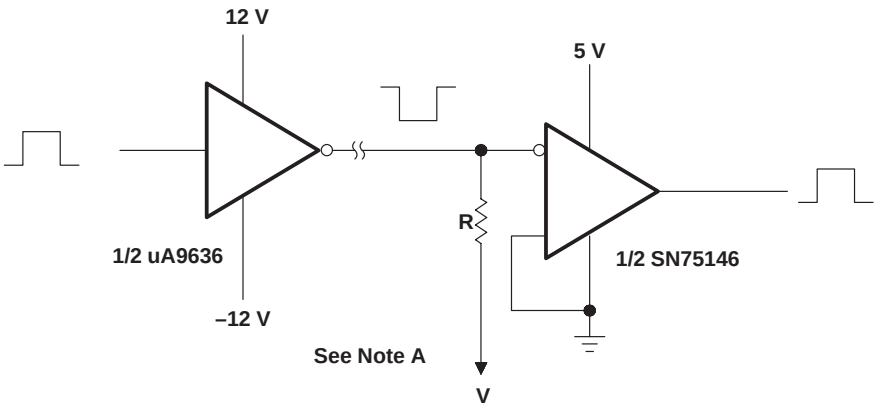


Figure 3

APPLICATION INFORMATION



NOTE A: In order to meet the input-impedance and open-circuit-input voltage requirements of ANSI Standard EIA/TIA-232-E and ITU recommendation V.28 and ensure open-circuit-input fail-safe operation, R and V are selected to satisfy the following equations:

$$V = -1.1 - 3.3\,\frac{R}{r_i}\ \text{volts}$$

$$3\ \text{k}\Omega \le \frac{R\left(r_i\right)}{R + r_i} \le 7\ \text{k}\Omega$$

Figure 4. EIA/TIA-232-E System Applications

APPLICATION INFORMATION

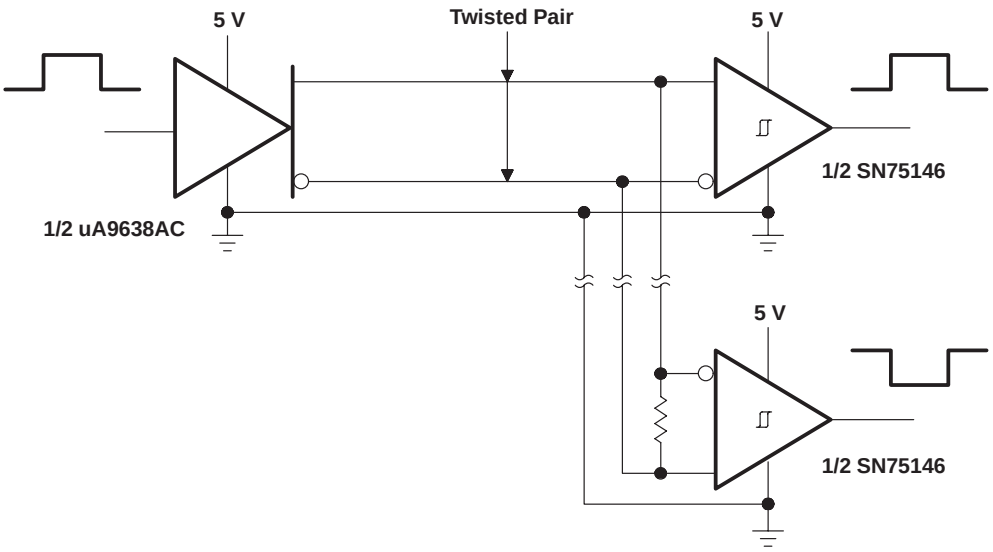


Figure 5. EIA/TIA-422-B System Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75146D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	75146	
SN75146P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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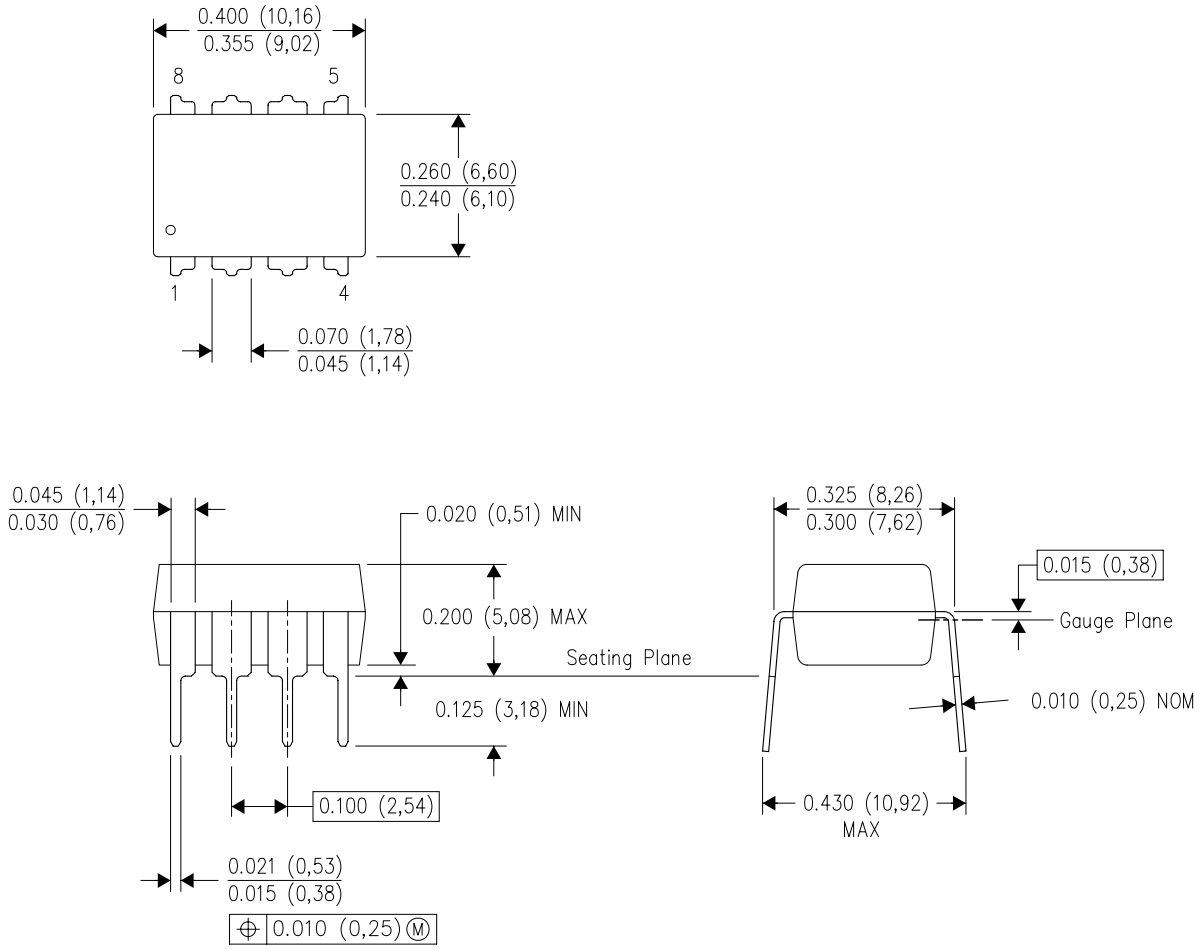
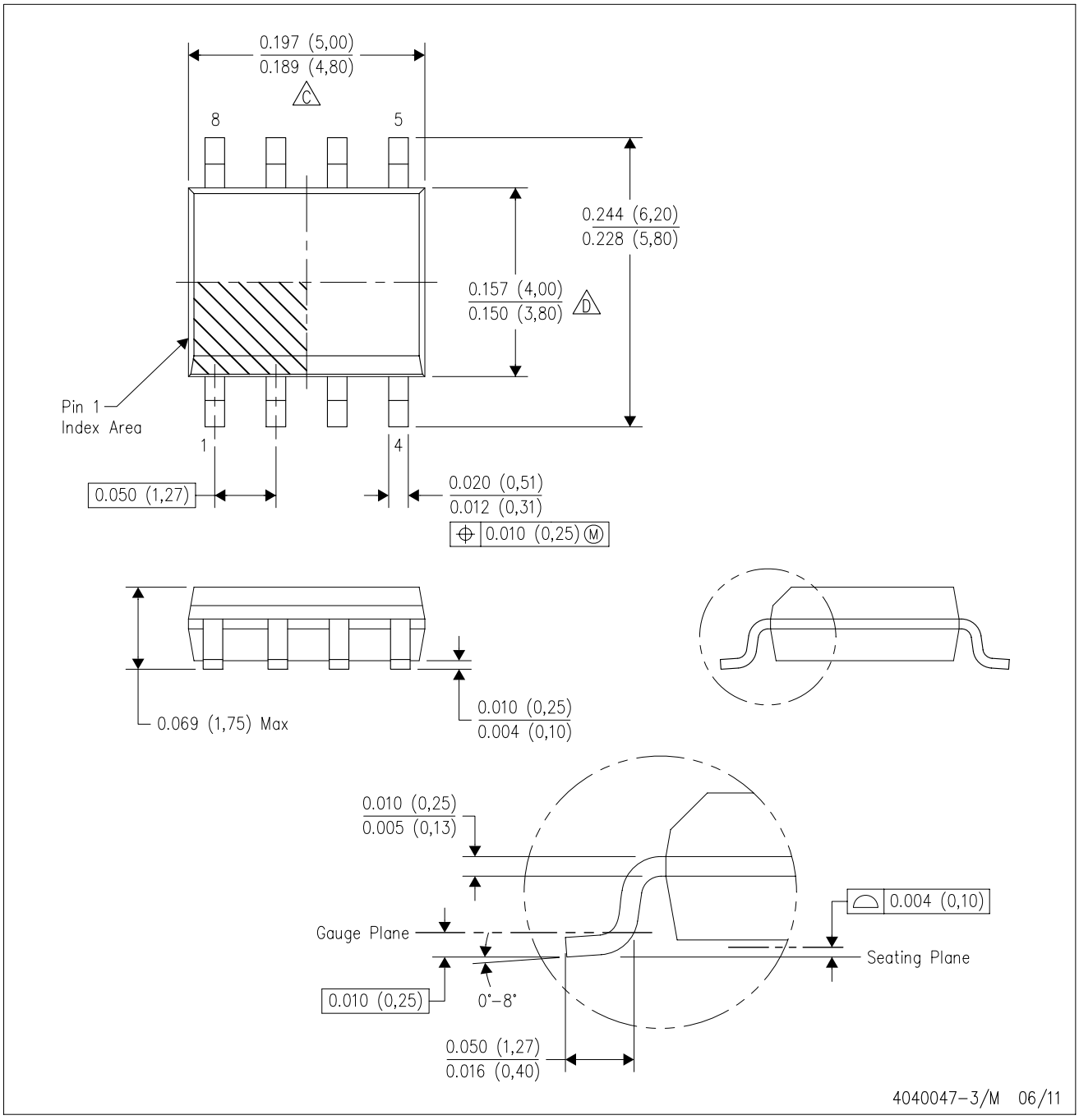
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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