



Current-Mode PWM Controllers for Isolated Power Supplies

General Description

The MAX5021/MAX5022 current-mode PWM controllers contain all the control circuitry required for the design of wide input voltage range isolated power supplies. These devices are well suited for use in universal input (85VAC to 265VAC) off-line or telecom (-36VDC to -72VDC) power supplies.

An undervoltage lockout (UVLO) circuit with large hysteresis coupled with low startup and operating current reduce power dissipation in the startup resistor and allow use of ceramic bypass capacitors. The 262kHz switching frequency is internally trimmed to $\pm 12\%$ accuracy; this allows the optimization of the magnetic and filter components resulting in compact, cost-effective power supplies. The MAX5021 with 50% maximum duty cycle and MAX5022 with 75% maximum duty cycle are recommended for forward converters and fly-back converters, respectively. The MAX5021/MAX5022 are available in 6-pin SOT23, 8-pin μ MAX, and 8-pin DIP packages and are rated for operation over the -40°C to $+85^{\circ}\text{C}$ temperature range.

Applications

Universal Off-Line Power Supplies
Standby Power Supplies
Isolated Power Supplies
Isolated Telecom Power Supplies
Mobile Phone Chargers

Features

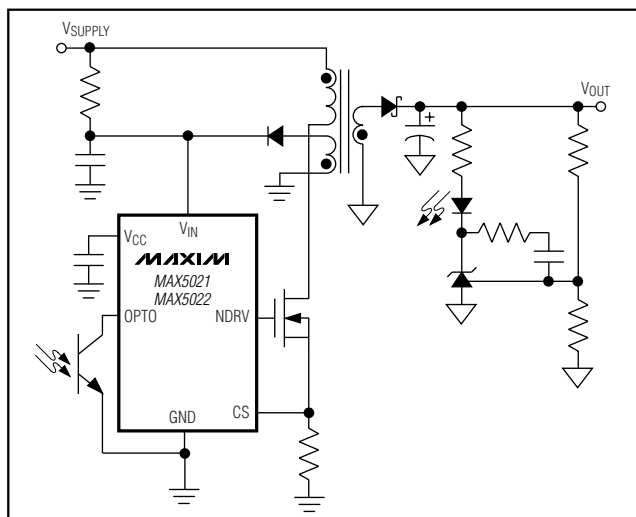
- ◆ Available in a Tiny 6-Pin SOT23 Package
- ◆ 50 μA Typical Startup Current
- ◆ 1.2mA Typical Operating Current
- ◆ Large UVLO Hysteresis of 14V
- ◆ Fixed Switching Frequency of 262kHz $\pm 12\%$
- ◆ 50% Maximum Duty Cycle Limit (MAX5021)
- ◆ 75% Maximum Duty Cycle Limit (MAX5022)
- ◆ 60ns Cycle-by-Cycle Current-Limit Response Time

Ordering Information

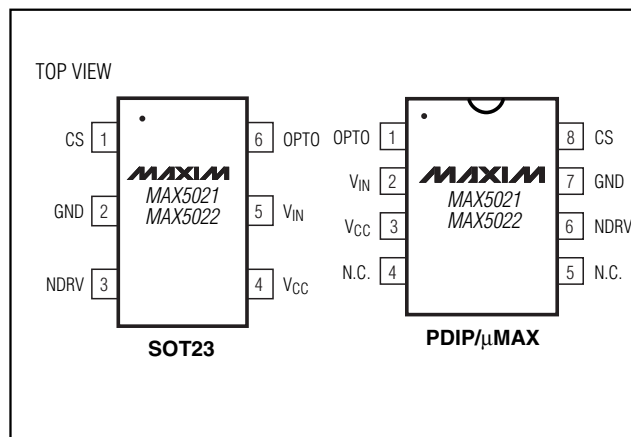
PART	MAX DUTY CYCLE	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX5021EUT	50%	-40°C to $+85^{\circ}\text{C}$	6 SOT23-6	AASQ
MAX5021EUA	50%	-40°C to $+85^{\circ}\text{C}$	8 μ MAX	—
MAX5021EPA	50%	-40°C to $+85^{\circ}\text{C}$	8 PDIP	—
MAX5022EUT	75%	-40°C to $+85^{\circ}\text{C}$	6 SOT23-6	AASR
MAX5022EUA	75%	-40°C to $+85^{\circ}\text{C}$	8 μ MAX	—
MAX5022EPA	75%	-40°C to $+85^{\circ}\text{C}$	8 PDIP	—

WARNING: The MAX5021/MAX5022 are designed to work with high voltages. Exercise caution!

Typical Operating Circuit



Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND-0.3V to +30V
 V_{CC} to GND-0.3V to +13V
NDRV to GND-0.3V to ($V_{CC} + 0.3V$)
CS, OPTO to GND-0.3V to +6V
NDRV Short-Circuit to GNDContinuous
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
6-Pin SOT23 (derate 8.7mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)696mW

8-Pin μMAX (derate 4.5mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)362mW
8-Pin PDIP (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$)727mW
Operating Temperature Range-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Storage Temperature Range-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering 10s)+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = +11V$ to +28V, $V_{CS} = 0$, OPTO is unconnected, 10nF bypass capacitors at V_{IN} and V_{CC} , NDRV unconnected, $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{IN} = +12V$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT/STARTUP						
Undervoltage Lockout Wakeup Level	V _{UVR}	V _{IN} rising	22	24	26	V
Undervoltage Lockout Shutdown Level	V _{UVF}	V _{IN} falling	9.3	10	10.9	V
V _{IN} Supply Current at Startup	I _{START}	V _{IN} = +22V		50	85	μA
V _{IN} Range	V _{IN}		11		28	V
Undervoltage Lockout Propagation Delay	T _{UVR}	V _{IN} steps up from +9V to +26V		5		μs
	T _{UVF}	V _{IN} steps down from +26V to +9V		1		
INTERNAL SUPPLY						
V _{CC} Regulator Set Point	V _{CCSP}	V _{IN} = +11V to +28V, sourcing 1μA to 5mA from V _{CC}	7.0		10.5	V
V _{IN} Supply Current after Startup	I _{IN}	V _{IN} = +28V, OPTO connected to GND	0.9		2.43	mA
		V _{IN} = +28V, OPTO unconnected (Note 2)	0.4			
GATE DRIVER						
Driver Output Impedance	R _{ON(LOW)}	Measured at NDRV sinking 5mA		10	20	Ω
	R _{ON(HIGH)}	Measured at NDRV sourcing 5mA		20	40	
Driver Peak Sink Current	I _{SINK}			250		mA
Driver Peak Source Current	I _{SOURCE}			150		mA
PWM COMPARATOR						
Comparator Offset Voltage	V _{OPWM}	V _{OPTO} - V _{CS}	600	750	900	mV
CS Input Bias Current	I _{CS}		-2		+2	μA
Propagation Delay from Comparator Input to NDRV	T _{PWM}	25mV overdrive		60		ns
Minimum On-Time	T _{ON(MIN)}			150		ns
CURRENT-LIMIT COMPARATOR						
Current-Limit Trip Threshold	V _{CS}		540	600	660	mV
Current-Limit Propagation Delay from Comparator Input to NDRV	T _{CL}	25mV overdrive		60		ns

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MAX5021/MAX5022

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = +11V$ to $+28V$, $V_{CS} = 0$, OPTO is unconnected, 10nF bypass capacitors at V_{IN} and V_{CC} , NDRV unconnected, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{IN} = +12V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

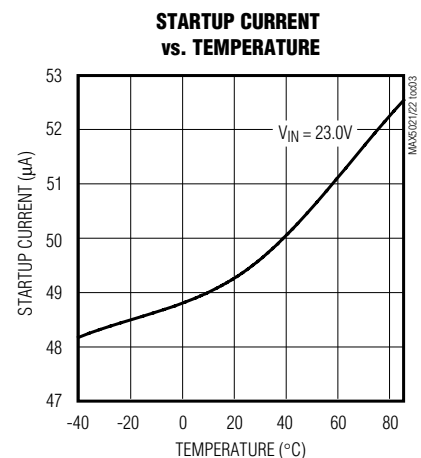
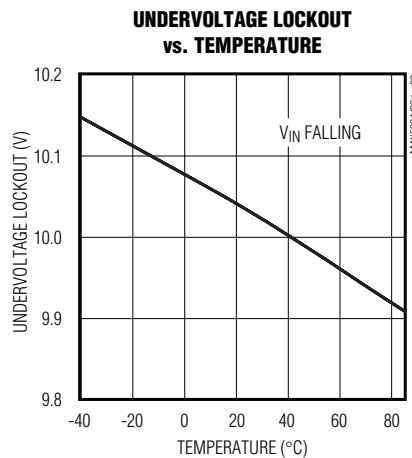
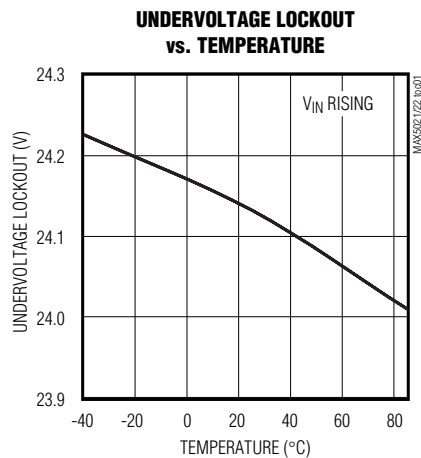
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Switching Frequency	fsw		230	262	290	kHz
Maximum Duty Cycle	DMAX	MAX5021		50	51	%
		MAX5022		75	76	
OPTO INPUT						
OPTO Pullup Voltage	VOPTO	OPTO sourcing 10μA			5.5	V
OPTO Pullup Resistance	ROPTO		4.5	6.2	7.9	kΩ

Note 1: All devices are 100% tested at $T_A = +25^\circ C$. All limits over temperature are guaranteed by characterization.

Note 2: This minimum current after startup is a safeguard that prevents the V_{IN} pin voltage from rising in the event that OPTO and NDRV become unconnected.

Typical Operating Characteristics

($V_{IN} = 15V$, $T_A = +25^\circ C$, unless otherwise noted.)

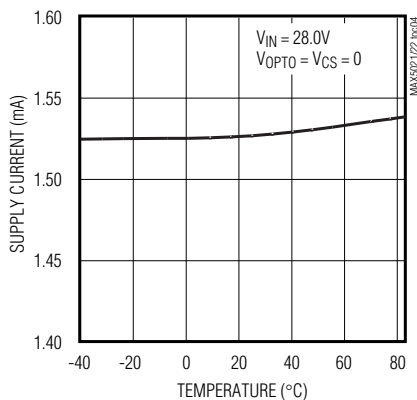


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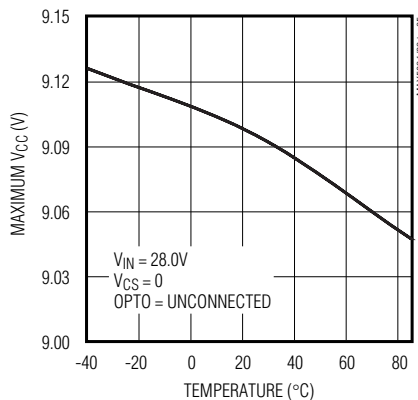
Typical Operating Characteristics (continued)

($V_{IN} = 15V$, $T_A = +25^\circ C$, unless otherwise noted.)

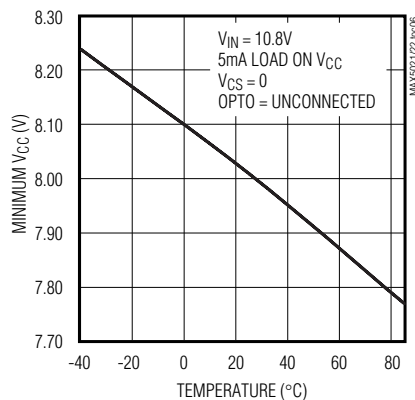
**SUPPLY CURRENT
vs. TEMPERATURE**



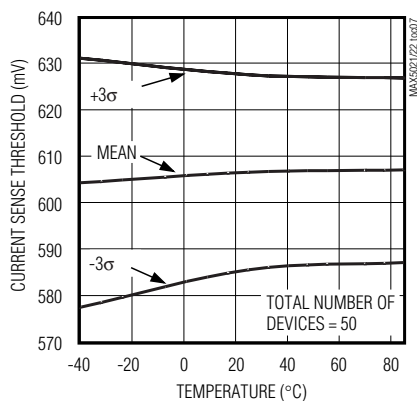
**MAXIMUM V_{CC}
vs. TEMPERATURE**



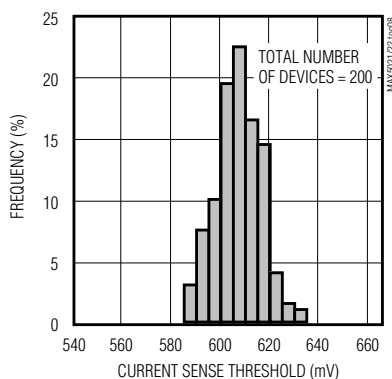
**MINIMUM V_{CC}
vs. TEMPERATURE**



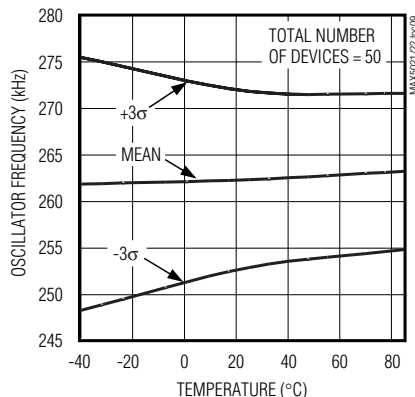
**CURRENT SENSE THRESHOLD
vs. TEMPERATURE**



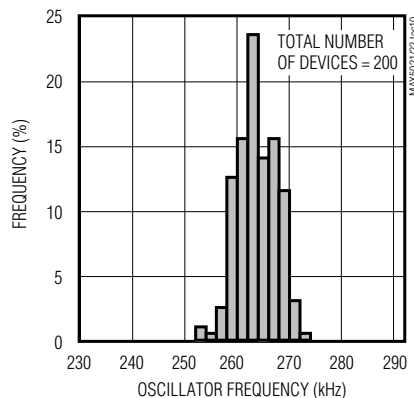
**CURRENT SENSE
THRESHOLD**



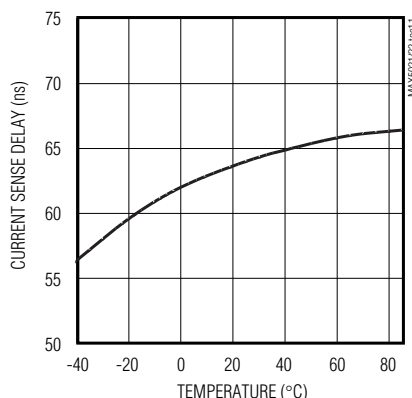
**OSCILLATOR FREQUENCY
vs. TEMPERATURE**



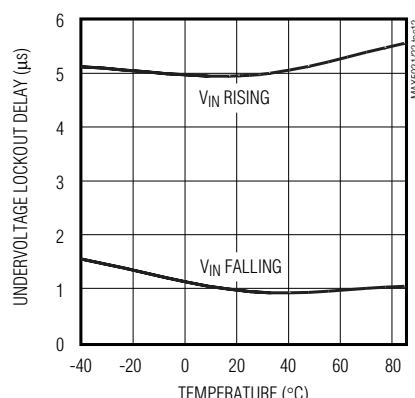
OSCILLATOR FREQUENCY



**CURRENT SENSE DELAY
vs. TEMPERATURE**



**UNDERVOLTAGE LOCKOUT
DELAY vs. TEMPERATURE**



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Pin Description

PIN		NAME	FUNCTION
SOT23	PDIP μMAX		
1	8	CS	Current Sense Connection for PWM Regulation and Overcurrent Protection. The current-limit comparator threshold is internally set to 0.6V.
2	7	GND	Power-Supply Ground
3	6	NDRV	External N-Channel MOSFET Gate Connection
4	3	V _{CC}	Gate Drive Supply. Internally regulated down from V _{IN} . Decouple with a 10nF or larger capacitor to GND.
5	2	V _{IN}	IC Supply. Decouple with a 10nF or larger capacitor to GND. Connect a startup resistor (R _S) from the input supply line to V _{IN} . Connect to bias winding through diode rectifier. See <i>Typical Operating Circuit</i> .
6	1	OPTO	Optocoupler Transistor Collector Connection. Connect emitter of optocoupler to GND. The OPTO has an internal pullup resistor with a typical value of 6.2kΩ.
—	4, 5	N.C.	No Connection. Do not make connections to these pins.

Detailed Description

The MAX5021/MAX5022 are current-mode PWM controllers that have been specifically designed for use in isolated power supplies. An undervoltage lockout circuit (UVLO) with a large hysteresis (14V) along with very low startup and operating current result in high-efficiency, universal input power supplies. Both devices can be used in power supplies capable of operating from a universal 85VAC to 265VAC line or the telecom voltage range of -36VDC to -72VDC.

Power supplies designed with these devices use a high-value startup resistor, R_S, (series combination of R₁ and R₂) that charges a reservoir capacitor, C₂ (see Figure 1). During this initial period while the voltage is less than the UVLO start threshold, the IC typically consumes only 50μA of quiescent current. This low startup current and the large UVLO hysteresis combined with the use of a ceramic capacitor C₂ keeps the power dissipation in R_S to less than 1/4W even at the high end of the universal AC input voltage (265VAC).

The MAX5021/MAX5022 include a cycle-by-cycle current limit which turns off the gate drive to the external MOSFET during an overcurrent condition. If the output on the secondary side of transformer T₁ is shorted, the tertiary winding voltage will drop below the 10V threshold causing the UVLO circuit to turn off the gate drive to the external power MOSFET, thus re-initiating the startup sequence.

Startup

Figure 2 shows the voltages on V_{IN} and V_{CC} during startup. Initially, both V_{IN} and V_{CC} are 0V. After the line voltage is applied, C₂ charges through the startup resistor, R_S, to an intermediate voltage at which point the internal reference and regulator begin charging C₃ (see Figure 1). The bias current consumed by the device during this period is only 50μA; the remaining input current charges C₂ and C₃. Charging of C₃ stops when the V_{CC} voltage reaches approximately 9.5V, while the voltage across C₂ continues rising until it reaches the wakeup level of 24V. Once V_{IN} exceeds the UVLO threshold, NDRV begins switching the MOSFET, transferring energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 10V (UVLO lower threshold), then startup has been accomplished and sustained operation will commence.

If V_{IN} drops below 10V before startup is complete, then the IC goes back into UVLO. In this case, increase the value of C₂ and/or use a MOSFET with a lower gate-charge requirement.

Startup Time Considerations

The V_{IN} bypass capacitor C₂ supplies current immediately after wakeup. The size of C₂ will determine the number of cycles available for startup. Large values for C₂ will increase the startup time, but will also supply more gate charge, allowing for more cycles after wakeup. If the value of C₂ is too small, V_{IN} will drop below 10V because

MAX5021/MAX5022



As a rule of thumb, off-line power supplies keep typical startup times to less than 500ms even in low-line conditions (85VAC input). Size the startup resistor, R_S , to supply the maximum startup bias of the IC (85 μ A) plus the additional current required for charging the capacitors C2 and C3 in less than 500ms. This resistor dissipates continuous power in normal operation, despite the fact that it is only used during the startup sequence. Therefore it must be chosen to provide enough current for the low-line condition as well as have an appropriate power rating for the high-line condition (265VAC). In most cases, split the value into two resistors connected in series for the required voltage of approximately 400VDC.

The diagram shows two voltage signals over a 200 ms period. The V_{IN} signal (top trace) starts at 0V, rises to approximately 4V at 10ms, then continues a linear ramp to 25V at 180ms. At 180ms, it drops sharply to about 10V and then exhibits small oscillations. The V_{CC} signal (bottom trace) starts at 0V, rises to about 1V at 10ms, then continues a linear ramp to 9V at 100ms. At 100ms, it levels off at 9V until 150ms, where it drops slightly to about 8.5V and then exhibits small oscillations. Annotations include: 'IC COMES OUT OF UVLO (WAKEUP)' at 10ms, 'VIN SUPPLIED BY C2' at 150ms, 'VIN SUPPLIED BY TERTIARY WINDING (NORMAL OPERATION)' at 180ms, 'VCC BYPASS CAPACITOR FULLY CHARGED' at 100ms, and 'VCC DROPS SLIGHTLY WHEN NDRV BEGINS SWITCHING' at 150ms.

to 24V all within the desired time period of 500ms, for an overall average charging current of 15 μ A. Hence, the startup resistor must provide a total of at least 100 μ A. Developing 100 μ A from an input voltage of

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85VAC (corresponding to 120VDC) to the 24V wakeup level results in a resistor value of about 1MΩ. If we assume R_S values between 750kΩ and 1MΩ, then at the high-line voltage of 265VAC (corresponding to 374VDC) power dissipation will be between 140mW to 190mW. A single 1/4W resistor or a series combination of two 1/4W resistors is adequate.

Undervoltage Lockout (UVLO)

The device will attempt to start when V_{IN} exceeds the UVLO threshold of 24V. During startup, the UVLO circuit keeps the CPWM comparator, ILIM comparator, oscillator, and output driver shut down to reduce current consumption (*Functional Diagram*). Once V_{IN} reaches 24V, the UVLO circuit turns on both the CPWM and ILIM comparators, as well as the oscillator, and allows the output driver to switch. If V_{IN} drops below 10V, the UVLO circuit will shut down the CPWM comparator, ILIM comparator, oscillator, and output driver returning the MAX5021/MAX5022 to the startup mode.

N-Channel MOSFET Switch Driver

The NDRV pin drives an external N-channel MOSFET. The NDRV output is supplied by the internal regulator (V_{CC}), which is internally set to approximately 9V. For the universal input voltage range, the MOSFET used must be able to withstand the DC level of the high-line input voltage plus the reflected voltage at the primary of the transformer. For most applications that use the discontinuous flyback topology, this requires a MOSFET rated at 600V. NDRV can source/sink 150mA/250mA peak current, thus select a MOSFET that will yield acceptable conduction and switching losses.

Internal Oscillator

The internal oscillator switches at 1.048MHz and is divided down to 262kHz by two D flip-flops. The MAX5021 inverts the Q output of the last D flip-flop to provide a duty cycle of 50% (Figure 3). The MAX5022 performs a logic NAND operation on the Q outputs of both D flip-flops to provide a duty cycle of 75%.

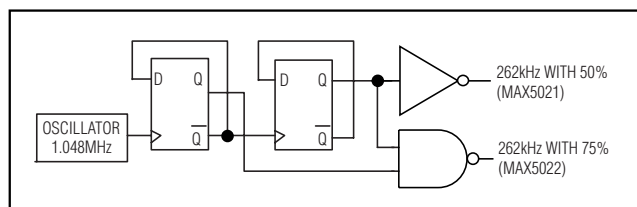


Figure 3. Internal Oscillator

Optocoupler Feedback

The MAX5021/MAX5022 do not include an internal error amplifier and are recommended for use in optocoupler feedback power supplies. Isolated voltage feedback is achieved by using an optocoupler and a shunt regulator as shown in the *Typical Operating Circuit*. The output voltage set point accuracy is a function of the accuracy of the shunt regulator and resistor divider.

When a TLV431 shunt regulator is used for output voltage regulation, the output voltage is set by the ratio of R₄ and R₅ (Figure 1). Output voltage is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_4}{R_5} \right)$$

where V_{REF} = 1.24V for the TLV431.

During normal operation, the optocoupler feedback pin (OPTO) is pulled up through a 6.2kΩ resistor to the internal supply voltage of 5.25V. When the device is in UVLO, OPTO is disconnected from the 5.25V regulator and connected to ground (*Functional Diagram*). This helps initial startup by reducing the current consumption of the device.

Current Limit

The current limit is set by a current sense resistor, R_{CS}, connected between the source of the MOSFET and ground. The CS input has a voltage trip level (V_{CS}) of 600mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{V_{CS}}{I_{PRI}}$$

where I_{PRI} is the peak current in the primary that flows through the MOSFET. When the voltage produced by this current through the current sense resistor exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) will quickly terminate the current ON-cycle, typically within 60ns. In most cases a small RC filter will be required to filter out the leading-edge spike on the sense waveform. Set the corner frequency at a few MHz.

Applications Information

Universal Off-Line Power Supply

Figure 1 shows the design of a 5V/1A isolated power supply capable of operating from a line voltage of 85VAC to 265VAC. This circuit is implemented in the MAX5022EVKIT.

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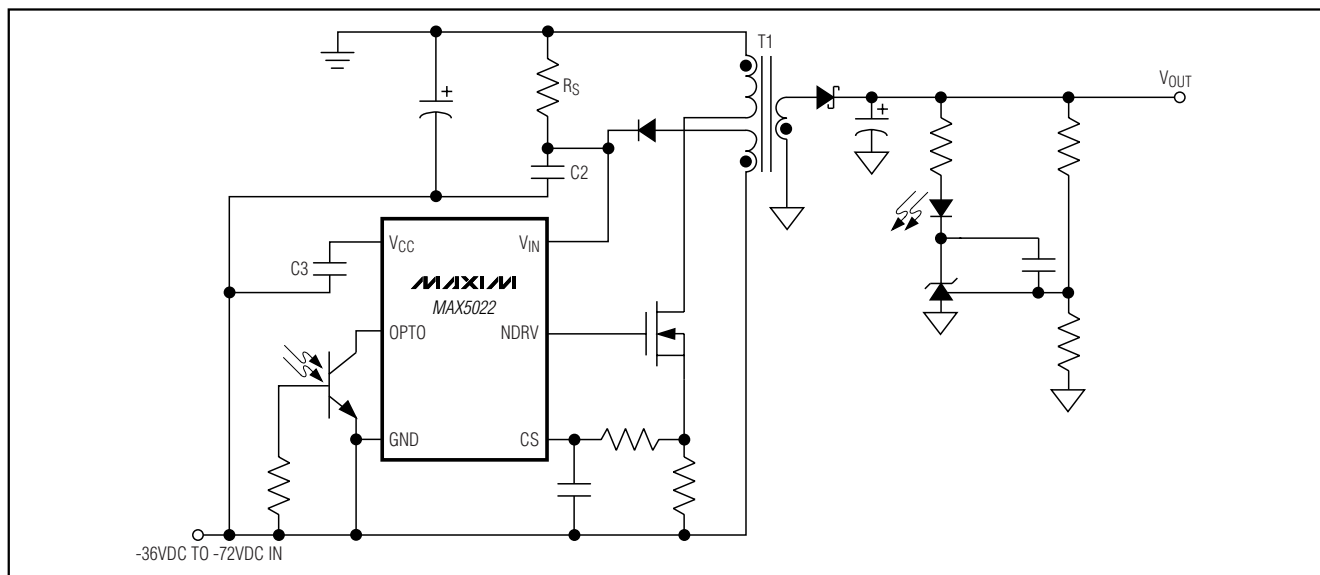


Figure 4. -48VDC Input to +5V Output

WARNING! DANGEROUS AND LETHAL VOLTAGES ARE PRESENT IN OFF-LINE CIRCUITS! USE EXTREME CAUTION IN THE CONSTRUCTION, TESTING, AND USE OF OFF-LINE CIRCUITS.

Isolated Telecom Power Supply

Figure 4 shows a -48VDC telecom power supply capable of generating an isolated +5V output.

Layout Recommendations

All printed circuit board traces carrying switching currents must be kept as short as possible, and the current loops they form must be minimized. The pins of the SOT23 package have been placed to allow simple interfacing to the external MOSFET. The order of these pins directly corresponds to the order of a TO-220 or similar package MOSFET.

For universal AC input design all applicable safety regulations must be followed. Off-line power supplies may require UL, VDE, and other similar agency approvals. These agencies can be contacted for the latest layout and component rules.

Typically there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly the heatsink of the MOSFET presents a dv/dt source, thus the surface area of the heatsink must be minimized as much as possible.

To achieve best performance, a star ground connection is recommended to avoid ground loops. For example, the ground returns for the power-line input filter, power MOSFET switch, and sense resistor should be routed separately through wide copper traces to meet at a single system ground connection.

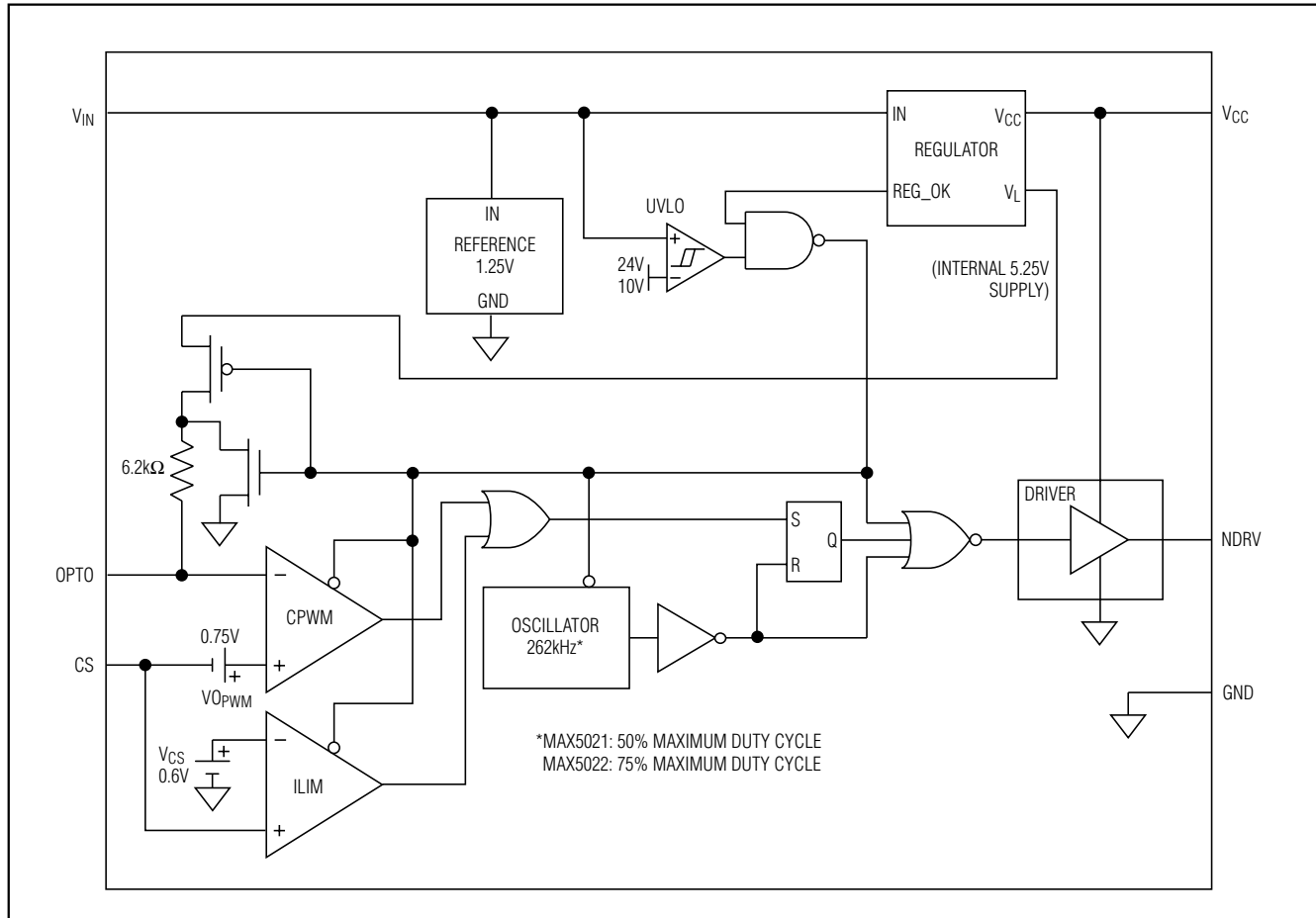
Chip Information

TRANSISTOR COUNT: 519

PROCESS: BiCMOS

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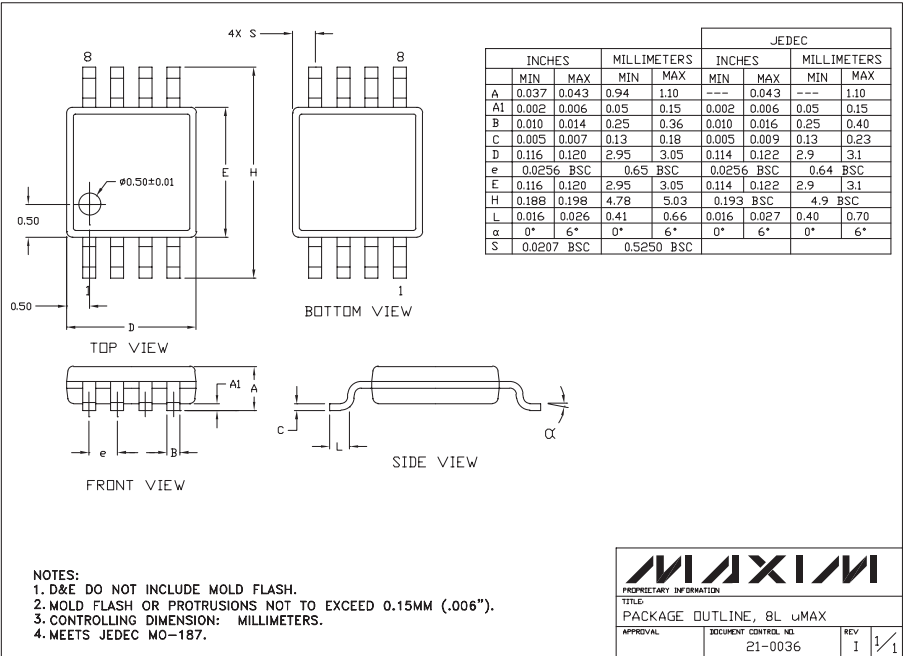
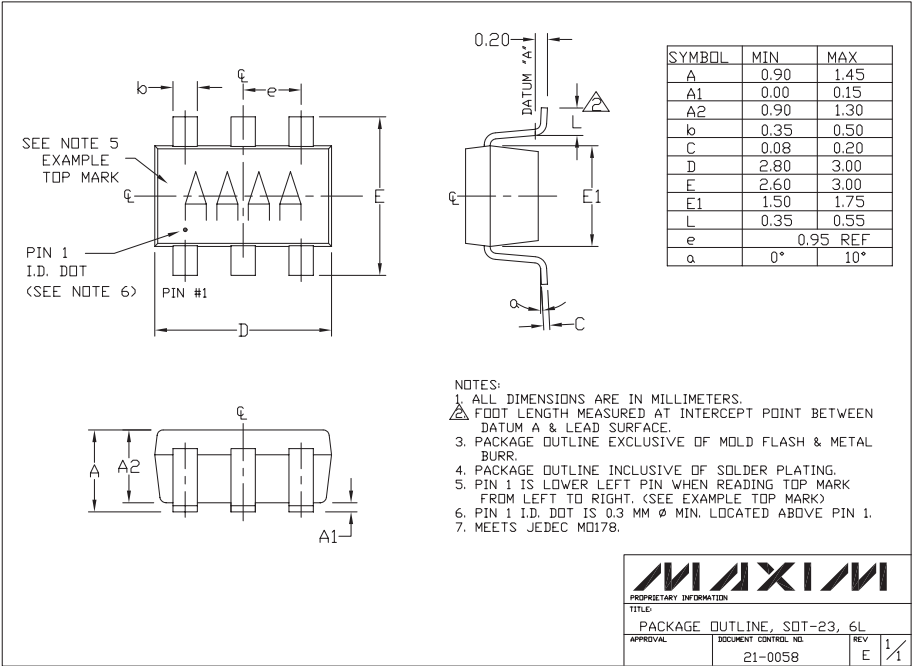
Functional Diagram



MAX5021/MAX5022

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Package Information



Package Information (continued)

Technical drawing of a PDIP package showing top, side, and end views with dimension callouts.

Top View Dimensions:

- D1:** Pin diameter
- N:** Number of pins
- D:** Package body width
- A:** Total height
- A2:** Height to top of mold flash
- A1:** Height to base of pins
- L:** Pin length
- e:** Pin pitch
- B1:** Pin thickness
- B:** Pin length at base

Side View Dimensions:

- E:** Total width
- E1:** Width to top of mold flash
- 0°-15°:** Lead angle
- C:** Width to base of pins
- eA:** Pin thickness at base
- eB:** Pin thickness at base

End View Dimensions:

- N:** Number of pins
- MS001:** JEDEC standard reference

Dimension Tables:

INCHES		MILLIMETERS	
MIN	MAX	MIN	MAX
A	---	0.180	4.572
A1	0.020	---	0.508
A2	0.125	0.175	3.18
A3	0.055	0.080	1.40
B	0.015	0.021	0.381
B1	0.045	0.060	1.14
C	0.009	0.014	0.229
D1	0.005	0.080	0.13
E	0.300	0.325	7.62
E1	0.275	0.295	6.985
e	0.100	---	2.54
eA	0.300	---	7.62
eB	---	0.400	---
L	0.115	0.150	2.921

INCHES		MILLIMETERS	
MIN	MAX	MIN	MAX
D	0.348	0.390	8.84
D	0.735	0.765	18.67
D	0.745	0.765	18.92
D	0.885	0.915	22.48
D	1.015	1.045	25.78
D	1.14	1.265	28.96
D	1.360	1.380	34.54

Notes:

- D&E DO NOT INCLUDE MOLD FLASH
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
- CONTROLLING DIMENSION: MILLIMETER
- MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
- SIMILAR TO JEDEC MS-095-AH
- N = NUMBER OF PINS

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