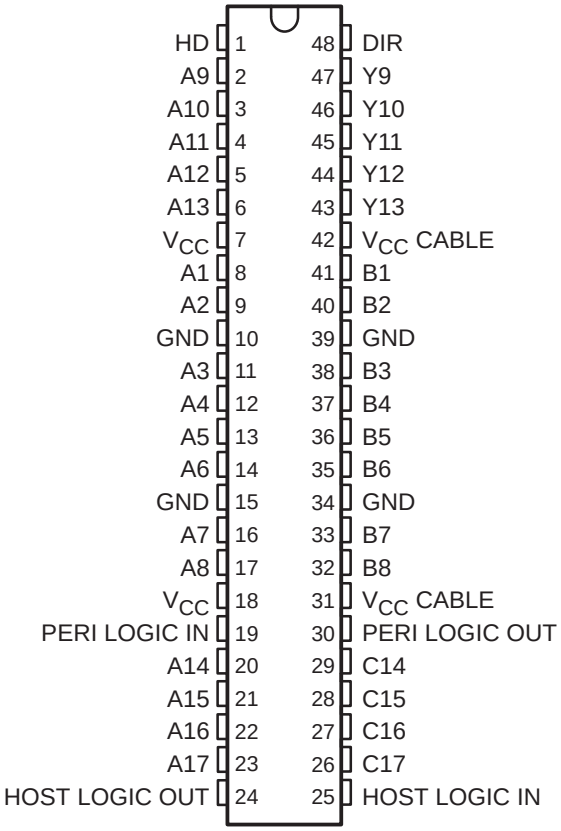
- **1.4-kΩ Pullup Resistors Integrated on All Open-Drain Outputs Eliminate the Need for Discrete Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Designed for the IEEE Std 1284-I (Level 1 Type) and IEEE Std 1284-II (Level 2 Type) Electrical Specifications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin-Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The SN74LVC161284 is designed for 3-V to 3.6-V $V_{CC}$ operation. This device provides asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device has eight bidirectional bits; data can flow in the A-to-B direction when DIR is high, and in the B-to-A direction when DIR is low. This device also has five drivers, which drive the cable side, and four receivers. The SN74LVC161284 has one receiver dedicated to the HOST LOGIC line and a driver to drive the PERI LOGIC line.

The output drive mode is determined by the high-drive (HD) control pin. When HD is high, the outputs are in a totem-pole configuration, and in an open-drain configuration when HD is low. This meets the drive requirements as specified in the IEEE Std 1284-I (level 1 type) and IEEE Std 1284-II (level 2 type) parallel peripheral-interface specifications. Except for HOST LOGIC IN and PERI LOGIC OUT, all cable-side pins have a 1.4-kΩ integrated pullup resistor. The pullup resistor is switched off if the associated output driver is in the low state or if the output voltage is above $V_{CC}$ CABLE. If $V_{CC}$ CABLE is off, PERI LOGIC OUT is set to low.

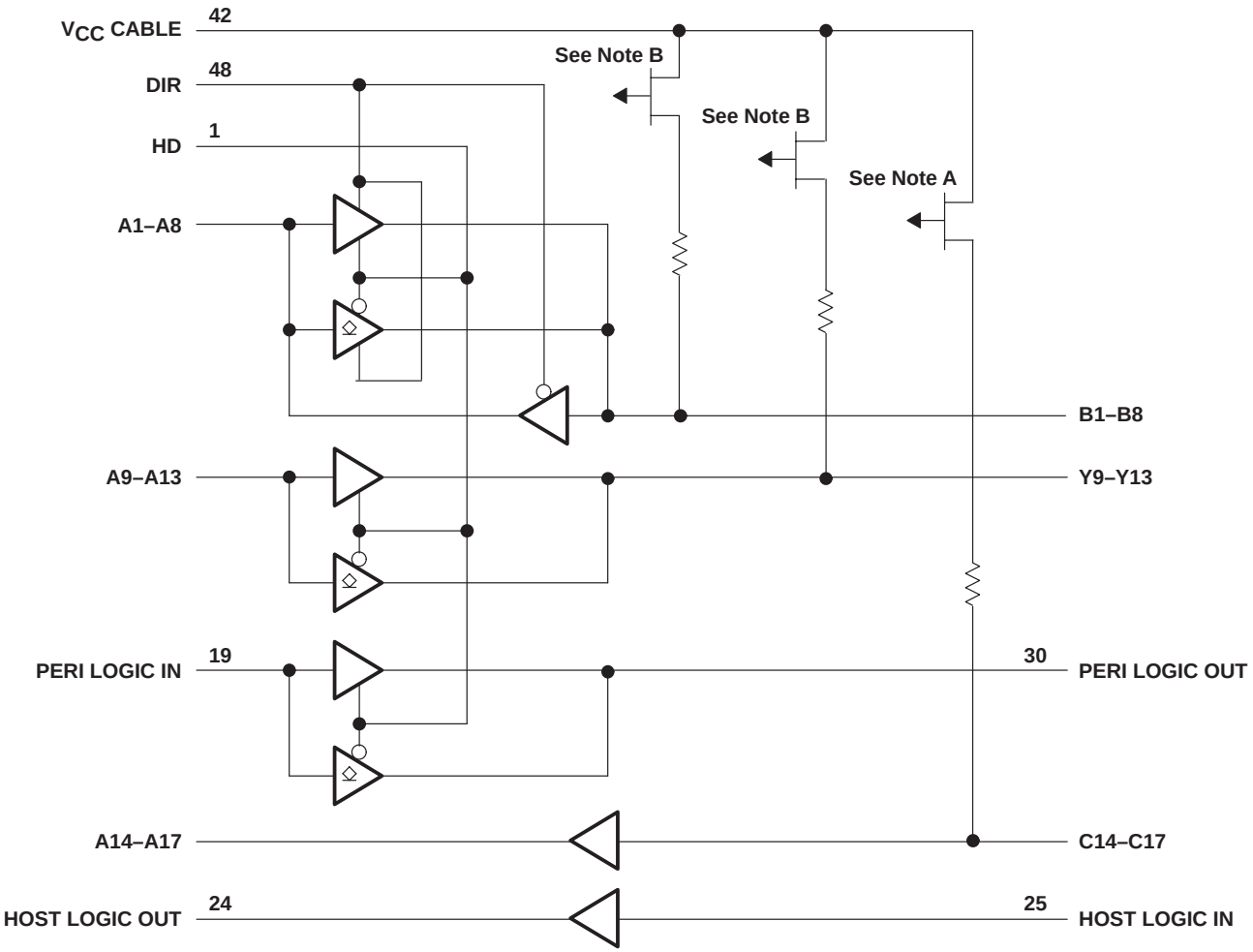
The device has two supply voltages. $V_{CC}$ is designed for 3-V to 3.6-V operation. $V_{CC}$ CABLE supplies the inputs and output buffers of the cable side only and is designed for 3-V to 3.6-V and for 4.7-V to 5.5-V operation. Even when $V_{CC}$ CABLE is 3 V to 3.6 V, the cable-side I/O pins are 5-V tolerant.

The SN74LVC161284 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | OUTPUT | MODE |
|---|---|---|---|
| DIR | HD | | |
| L | L | Open drain | A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT |
| | | Totem pole | B1–B8 to A1–A8 and C14–C17 to A14–A17 |
| L | H | Totem pole | B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17 |
| H | L | Open drain | A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT |
| | | Totem pole | C14–C17 to A14–A17 |
| H | H | Totem pole | A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT |

## logic diagram




NOTES: A. The PMOS transistor prevents backdriving current from the signal pins to $V_{CC}$ CABLE when $V_{CC}$ CABLE is open or at GND.
B. The PMOS transistors prevent backdriving current from the signal pins to $V_{CC}$ CABLE when $V_{CC}$ CABLE is open or at GND. The PMOS transistor is turned off when the associated driver is in the low state.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: $V_{CC}$ CABLE . . . . . –0.5 V to 7 V
$V_{CC}$ . . . . . –0.5 V to 4.6 V
Input and output voltage range, $V_I$ and $V_O$: Cable side (see Notes 1 and 2) . . . . . –2 V to 7 V
Peripheral side (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$: Except PERI LOGIC OUT . . . . . ±50 mA
PERI LOGIC OUT . . . . . ±100 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±200 mA
Output high sink current, $I_{SK}$ ($V_O$ = 5.5 V and $V_{CC}$ CABLE = 3 V) . . . . . 65 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The ac input voltage pulse duration is limited to 40 ns if the amplitude is greater than –0.5 V.
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ CABLE | Supply voltage for the cable side, $V_{CC}$ CABLE ≥ $V_{CC}$ | | 3 | 5.5 | V |
| $V_{CC}$ | Supply voltage | | 3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | A, B, DIR, and HD | 2 | | V |
| | | C14–C17 | 2.3 | | |
| | | HOST LOGIC IN | 2.6 | | |
| | | PERI LOGIC IN | 2 | | |
| $V_{IL}$ | Low-level input voltage | A, B, DIR, and HD | | 0.8 | V |
| | | C14–C17 | | 0.8 | |
| | | HOST LOGIC IN | | 1.6 | |
| | | PERI LOGIC IN | | 0.8 | |
| $V_I$ | Input voltage | Peripheral side | 0 | $V_{CC}$ | V |
| | | Cable side | 0 | 5.5 | |
| $V_O$ | Open-drain output voltage | HD low | 0 | 5.5 | V |
| $I_{OH}$ | High-level output current | HD high, B and Y outputs | | –14 | mA |
| | | A outputs and HOST LOGIC OUT | | –4 | |
| | | PERI LOGIC OUT | | –0.5 | |
| $I_{OL}$ | Low-level output current | B and Y outputs | | 14 | mA |
| | | A outputs and HOST LOGIC OUT | | 4 | |
| | | PERI LOGIC OUT | | 84 | |
| $T_A$ | Operating free-air temperature | | 0 | 70 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ CABLE = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta V_t$ | Input hysteresis | $V_{thH} - V_{thL}$ for all inputs except the C inputs and HOST LOGIC IN | 3.3 V | 0.4 | | | V |
| | | $V_{thH} - V_{thL}$ for the HOST LOGIC IN | 3.3 V | 0.2 | | | |
| | | $V_{thH} - V_{thL}$ for the C inputs | 3.3 V | 0.8 | | | |
| $V_{OH}$ | HD high, B and Y outputs | $I_{OH}$ = –14 mA | 3 V | 2.23 | | | V |
| | | | 3.3 V‡ | 2.4 | | | |
| | HD high, A outputs, and HOST LOGIC OUT | $I_{OH}$ = –4 mA | 3 V | 2.4 | | | |
| | | $I_{OH}$ = –50 µA | 3 V | 2.8 | | | |
| | PERI LOGIC OUT | $I_{OH}$ = –0.5 mA | 3.15 V | 3.1 | | | |
| | | | 3.3 V‡ | 4.5 | | | |
| $V_{OL}$ | B and Y outputs | $I_{OL}$ = 14 mA | 3 V | | | 0.77 | V |
| | A outputs and HOST LOGIC OUT | $I_{OL}$ = 50 µA | 3 V | | | 0.2 | |
| | | $I_{OL}$ = 4 mA | 3 V | | | 0 4 | |
| | PERI LOGIC OUT | $I_{OL}$ = 84 mA | 3 V | | | 0.8 | |
| $I_I$ | C inputs | $V_I = V_{CC}$ | 3.6 V§ | | | 50 | µA |
| | | $V_I$ = GND (pullup resistors) | 3.6 V§ | | | –3.5 | mA |
| | All inputs except the B or C inputs | $V_I = V_{CC}$ or GND | 3.6 V | | | ±1 | µA |
| $I_{OZ}$ | B outputs | $V_O = V_{CC}$ | 3.6 V | | | 20 | µA |
| | | $V_O$ = GND (pullup resistors) | 3.6 V§ | | | –3.5 | mA |
| | A1–A8 | $V_O = V_{CC}$ or GND | 3.6 V | | | ±20 | µA |
| | Open-drain Y outputs | $V_O$ = GND (pullup resistors) | 3.6 V§ | | | –3.5 | mA |
| $I_{off}$ | Leakage to GND, B and Y outputs | $V_I$ or $V_O$ = 0 to 7 V | 0 V | | | 100 | µA |
| | Leakage to $V_{CC}$, B and Y outputs | | | | | 10 | |
| $I_{CC}$¶ | | $V_I = V_{CC}$, $I_O$ = 0 | 3.6 V | | | 0.8 | mA |
| | | $V_I$ = GND (12 × pullup) | 3.6 V | | | 45 | |
| $C_i$ | Control inputs | $V_I = V_{CC}$ or GND | 3.3 V | | 3 | 4 | pF |
| $C_{io}$ | All inputs | $V_O = V_{CC}$ or GND | 3.3 V | | 7 | 15 | pF |
| $Z_O$ | Cable side | $I_{OH}$ = –35 mA | 3.3 V | | 45 | | Ω |
| R pullup | Cable side | $V_O$ = 0 V (in Hi Z) | 3.3 V | 1.15 | | 1.65 | kΩ |

† Typical values are measured at $V_{CC}$ = 3.3 V, $V_{CC}$ CABLE = 5 V, and $T_A$ = 25°C.
‡ $V_{CC}$ CABLE = 4.7 V
§ $V_{CC}$ CABLE = 3.6 V
¶ A maximum current of 170 µA per pin is added to $I_{CC}$ if the pullup resistor pin is above $V_{CC}$.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

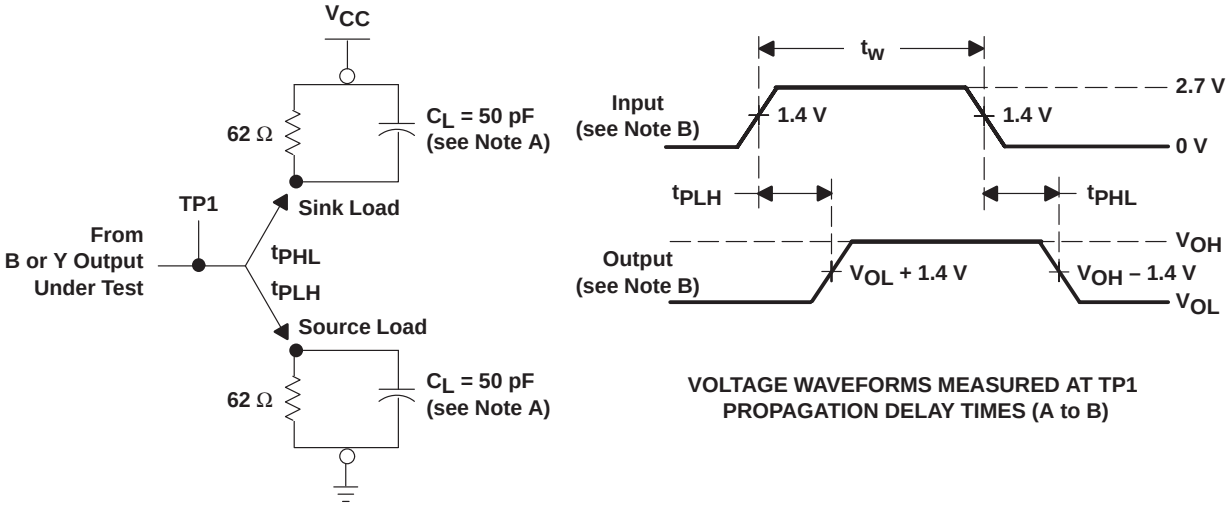
| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Totem pole | A or B | B or A | 1 | | 40 | ns |
| $t_{PHL}$ | | | | 1 | | 40 | |
| $t_{slew}$ | Totem pole | Cable-side outputs | | 0.05 | | 0.4 | V/ns |
| $t_{en}$ | Totem pole | HD | B, Y, and PERI LOGIC OUT | 1 | | 25 | ns |
| $t_{dis}$ | Totem pole | HD | B, Y, and PERI LOGIC OUT | 1 | | 25 | ns |
| $t_{en}$–$t_{dis}$ | | | | 1 | | 10 | ns |
| $t_{en}$ | | DIR | A | 1 | | 50 | ns |
| $t_{dis}$ | | DIR | A | 1 | | 15 | ns |
| | | | B | 1 | | 50 | |
| $t_r$, $t_f$ | Open drain | A | B or Y | | | 120 | ns |
| $t_{sk(o)}$‡ | | A or B | B or A | | 2.5 | 10 | ns |

† Typical values are measured at $V_{CC}$ = 3.3 V, $V_{CC}$ CABLE = 5 V, and $T_A$ = 25°C.
‡ Skew is measured at 1/2 ($V_{OH}$ + $V_{OL}$) for signals switching in the same direction.

## operating characteristics, $V_{CC}$ = 3.3 V, $T_A$ = 25°C

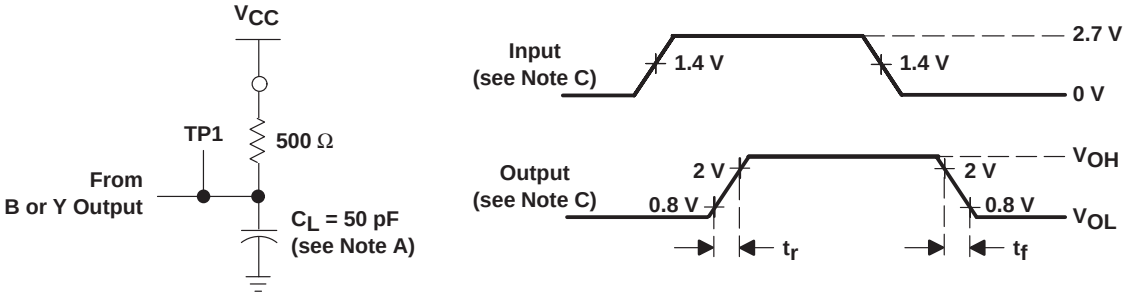
| PARAMETER | | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 0, | f = 10 MHz | 45 | pF |

## PARAMETER MEASUREMENT INFORMATION




VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)

SLEW RATE A-TO-B OR A-TO-Y LOAD (Totem Pole)



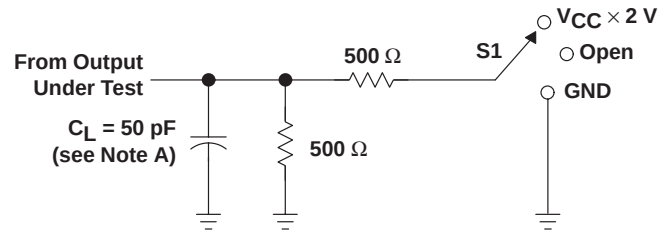

VOLTAGE WAVEFORMS MEASURED AT TP1, B SIDE

A-TO-B LOAD OR A-TO-Y LOAD (Open Drain)

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input rise and fall times are 3 ns, 150 ns < pulse duration < 10 µs for both low-to-high and high-to-low transitions. Slew rate is measured between 0.4 V and 0.9 V for the rising edge and between 2.4 V and 1.9 V for the falling edge.
C. Input rise and fall times are 3 ns. Rise and fall times (open drain) < 120 ns.
D. The outputs are measured one at a time with one transition per measurement.

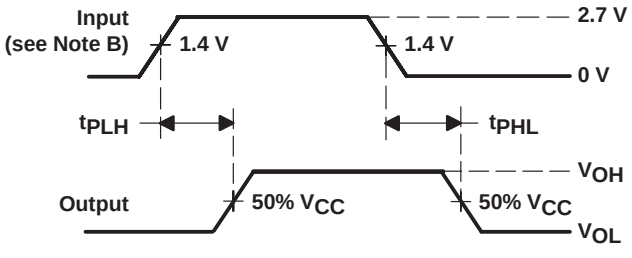
**Figure 1. Load Circuits and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION

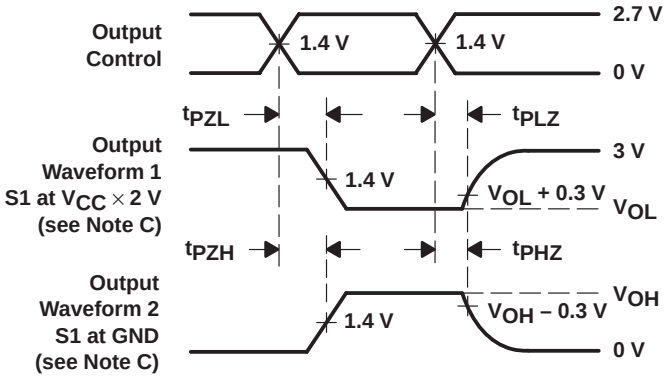



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC} \times 2$ V |
| $t_{PHZ}/t_{PZH}$ | GND |

LOAD CIRCUIT

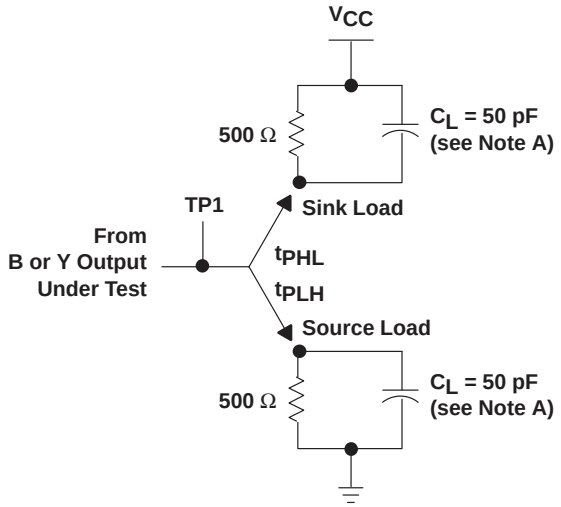


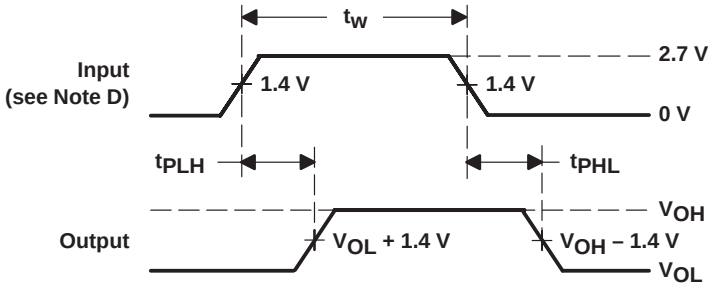

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B to A)




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

B-TO-A LOAD (Totem Pole)




VOLTAGE WAVEFORMS MEASURED AT TP1
PROPAGATION DELAY TIMES (A to B)

A-TO-B LOAD OR A-TO-Y LOAD (Totem Pole)

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input rise and fall times are 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. Input rise and fall times are 3 ns. Pulse duration is 150 ns < $t_w$ < 10 µs.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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