- **Versatile Multiplexing Interface Allows Lower Pixel Bus Rate**
- **High Level of Integration Provides Lower System Cost and Complexity**
- **Versatile Pixel Bus Interface Supports Little- and Big-Endian Data Formats**
- **Directly Interfaces to TMS34010/TMS34020 and Other Graphics Processors**
- **Single 8-Bit D/A Converters**
- **Low Cost Monochrome and Gray-Scale System**
- **Pin Compatible With TLC34075 and TLC34076**
- **135-, 170-, and 200-MHz Versions**
- **On-Chip Voltage Reference**
- **RS-343A-Compatible Outputs**
- **TTL-Compatible Inputs**
- **Standard MPU Interface**
- **On-Chip Clock Selection**
- **Directly Interfaces to Video RAM**
- **Supports Split Shift-Register Transfers**
- **TIGA™ Software-Standard Compatible**
- **CMOS Technology**
- **Data Manual Available†**

description

The TLC34074 video interface DAC (VID) is designed for monochrome and gray-scale graphics systems, providing lower system cost with a higher level of integration by incorporating all the high-speed timing, synchronizing, and multiplexing logic usually associated with graphics systems into one device, thus greatly reducing chip count. Since all high-speed signals (excluding the clock source) are contained on-chip, RF noise considerations are simplified. Maximum flexibility is provided through the pixel multiplexing scheme, which allows for 32-, 16-, 8-, and 4-bit pixel buses to be accommodated without any circuit modification. This enables the system to be easily reconfigured for varying amounts of available video RAM. Additionally, data can be split into 1, 2, 4, or 8-bit gray-scale.

The TLC34074 is also designed to be terminal compatible with the TLC34075 and TLC34076 video interface palettes. Therefore, a single graphics design can be configured into a color or black-and-white system by using either the TLC34075/076 or the TLC34074 to reduce the system cost and increase the resolution. Like the TLC34076, the TLC34074 can be programmed for little or big-endian data format for the pixel bus frame buffer interface.

The TLC34074 has an 8-bit video digital-to-analog converter (DAC) capable of directly driving a doubly terminated 75-Ω line. Sync generation can be incorporated onto the output channel when so enabled. Hsync and Vsync are fed through the device and optionally inverted to indicate screen resolution to the monitor. Bit stuffing logic repeats the intended gray-scale pattern to the least significant bits when the gray-scale is not 8 bits wide. This allows the 8-bit DAC to achieve full RS-343A output levels while maintaining uniform linearity for all codes.

AVAILABLE OPTIONS

T_A	SPEED	DAC RESOLUTION	PACKAGE
			PLASTIC CHIP CARRIER (FN)
0°C to 70°C	135 MHz	8 Bits	TLC34074-135FN
	170 MHz	8 Bits	TLC34074-170FN
	200 MHz	8 Bits	TLC34074-200FN

† For the complete data manual, refer to the Graphics and Imaging Data Book (SLAD002).

TIGA is a trademark of Texas Instruments Incorporated.

description (continued)

Clocking is provided through one of four inputs (3 TTL- and 1 ECL/TTL-compatible) and is software selectable. The video and shift-clock outputs provide a software-selected divide ratio of the chosen clock input.

The TLC34074 can be connected directly to the serial port of VRAM devices, eliminating the need for any discrete logic. Support for split shift-register transfers is also provided.

functional block diagram

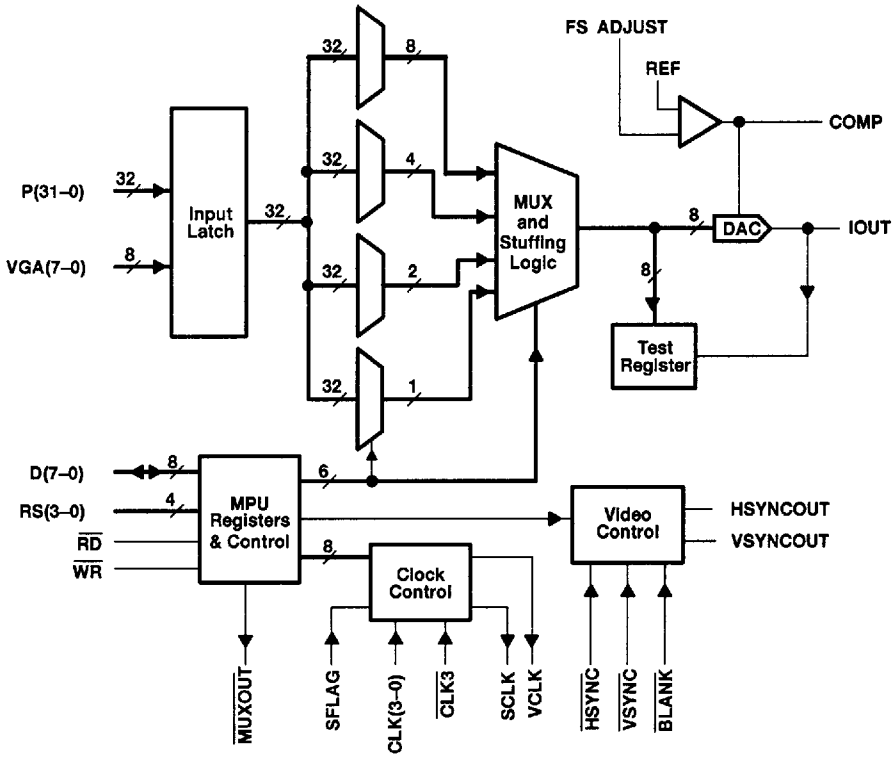

Figure 1. Functional Block Diagram