REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 01295 to case outlines R and 2. Add vendor CAGE 27014 to case outline 2.	1987 SEPT 23	M.A. Frye
B	Change vendor CAGE code to 67268. Add case outline S to drawing. Add vendor CAGE 01295 to case outline S. Remove vendor CAGE 04713 from drawing. Editorial changes to table I. Editorial changes throughout.	1989 JUL 24	M.A. Frye

CURRENT CAGE CODE 67268

REV																								
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SHEET																								
REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16							

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: James E. Nicholas

CHECKED BY: Ray Monnin

APPROVED BY: M.A. Frye

DRAWING APPROVAL DATE: 17 JULY 1986

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HIGH SPEED, CMOS, OCTAL, D-TYPE LATCH, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-86062

SHEET 1 OF 16

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1253

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86062	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC563	Octal, 3-state, inverting D-type, transparent latch

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20 lead, .540" x .300" x .100") flat package
2	C-2 (20-terminal .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	±20 mA
DC output current (per pin)	±35 mA
DC V_{CC} or GND current (per pin)	±70 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases R, S, and 2	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.

1.4 Recommended operating conditions.

Supply voltage range	+2.0 V dc to +6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time:	
V_{CC} = 2.0 V	0 to 1,000 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns
Minimum setup time (t_s):	
T_C = +25°C:	
V_{CC} = 2.0 V	75 ns
V_{CC} = 4.5 V	15 ns
V_{CC} = 6.0 V	13 ns
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	110 ns
V_{CC} = 4.5 V	22 ns
V_{CC} = 6.0 V	19 ns
Minimum hold time (t_h):	
T_C = +25°C:	
V_{CC} = 2.0 V	50 ns
V_{CC} = 4.5 V	10 ns
V_{CC} = 6.0 V	9 ns
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	75 ns
V_{CC} = 4.5 V	15 ns
V_{CC} = 6.0 V	13 ns
Minimum pluse width (t_w):	
T_C = +25°C:	
V_{CC} = 2.0 V	80 ns
V_{CC} = 4.5 V	16 ns
V_{CC} = 6.0 V	14 ns
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	120 ns
V_{CC} = 4.5 V	24 ns
V_{CC} = 6.0 V	20 ns

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	$V_{IN} = V_{IH}(min)$ or $V_{IL}(max)$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
		$\lvert I_O \rvert \le 20$ µA	$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}(min)$ or $V_{IL}(max)$ $\lvert I_O \rvert \le 6.0$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}(min)$ or $V_{IL}(max)$ $\lvert I_O \rvert \le 7.8$ mA	$V_{CC} = 6.0$ V		5.2		
Low level output voltage	V_{OL}	$V_{IN} = V_{IH}(min)$ or $V_{IL}(max)$	$V_{CC} = 2.0$ V	1, 2, 3		0.1	
		$\lvert I_O \rvert \le 20$ µA	$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}(min)$ or $V_{IL}(max)$ $\lvert I_O \rvert \le 6.0$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}(min)$ or $V_{IL}(max)$ $\lvert I_O \rvert \le 7.8$ mA	$V_{CC} = 6.0$ V			0.4	
High level input voltage 2/	V_{IH}		$V_{CC} = 2.0$ V	1, 2, 3	1.5		
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/		Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage 2/	V_{IL}		V_{CC} = 2.0 V	1, 2, 3		0.3	V
			V_{CC} = 4.5 V			0.9	
			V_{CC} = 6.0 V			1.2	
Input capacitance	C_{IN}	V_{IN} = 0 V, T_C = +25°C see 4.3.1c		4		10	pF
Quiescent current	I_{CC}	V_{CC} = 6.0 V V_{IN} = V_{CC} or GND		1, 2, 3		160	µA
Input leakage current	I_{IN}	V_{CC} = 6.0 V V_{IN} = V_{CC} or GND		1, 2, 3		±1	
Three-state output leakage current	I_{OZ}	V_O = V_{CC} or GND V_I = V_{IH} or V_{IL}		1, 2, 3		±10	µA
Output capacitance	C_{OUT}	See 4.3.1c		4		20	pF
Functional tests		See 4.3.1d		7			
Propagation delay time, data to Q output (see fig. 4) 3/	t_{PHL1} t_{PLH1}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		175	ns
			V_{CC} = 4.5 V			35	
			V_{CC} = 6.0 V			30	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		265	
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified 1/		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, latch enable to any output (see fig. 4) 3/	t_{PHL2} t_{PLH2}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		175	ns
			V_{CC} = 4.5 V			35	
			V_{CC} = 6.0 V			30	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		265	
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	
Propagation delay time, output enable to any output (see fig. 4) 3/	t_{PZH} t_{PZL}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		175	ns
			V_{CC} = 4.5 V			35	
			V_{CC} = 6.0 V			30	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		265	
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, output disable to any output (see fig. 4) 3/	t_{PHZ} t_{PLZ}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		150	ns
			V_{CC} = 4.5 V			30	
			V_{CC} = 6.0 V			26	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		225	
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			38	
Transition time, output rise and fall (see fig. 4) 4/	t_{THL} t_{TLH}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		60	ns
			V_{CC} = 4.5 V			12	
			V_{CC} = 6.0 V			10	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		90	
			V_{CC} = 4.5 V			18	
			V_{CC} = 6.0 V			15	

1/ For a power supply of 5 V ±10%, the worst case output voltages (V_{OH} and V_{OL}) occur for V_{CC} at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst cases V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V, respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage currents (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage, so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 50 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ V_{IL} and V_{IH} tests not required. Apply as forcing function for V_{OH} and V_{OL}.

3/ AC testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed if not tested to the specified parameters.

4/ Transition times, if not tested, shall be guaranteed to the specified parameters.

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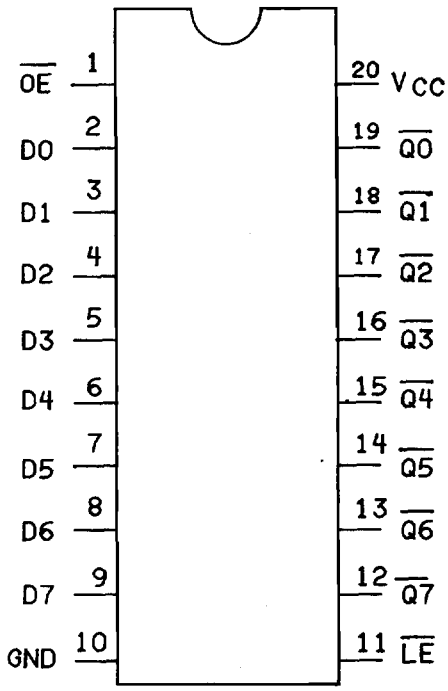
Cases R and S



Case 2

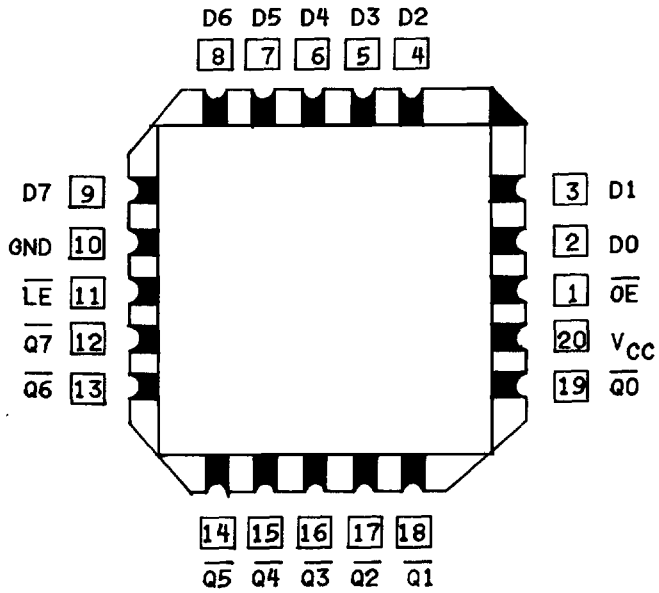


FIGURE 1. Terminal connections (top view).

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$\overline{\text{Output Enable}}$	$\overline{\text{Latch Enable}}$	Data	$\overline{Q}$ Output
L	H	H	L
L	H	L	H
L	L	l	H
L	L	h	L
H	X	X	Z

NOTE
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition
X = Don't care
Z = High impedance state

FIGURE 2. Truth table.

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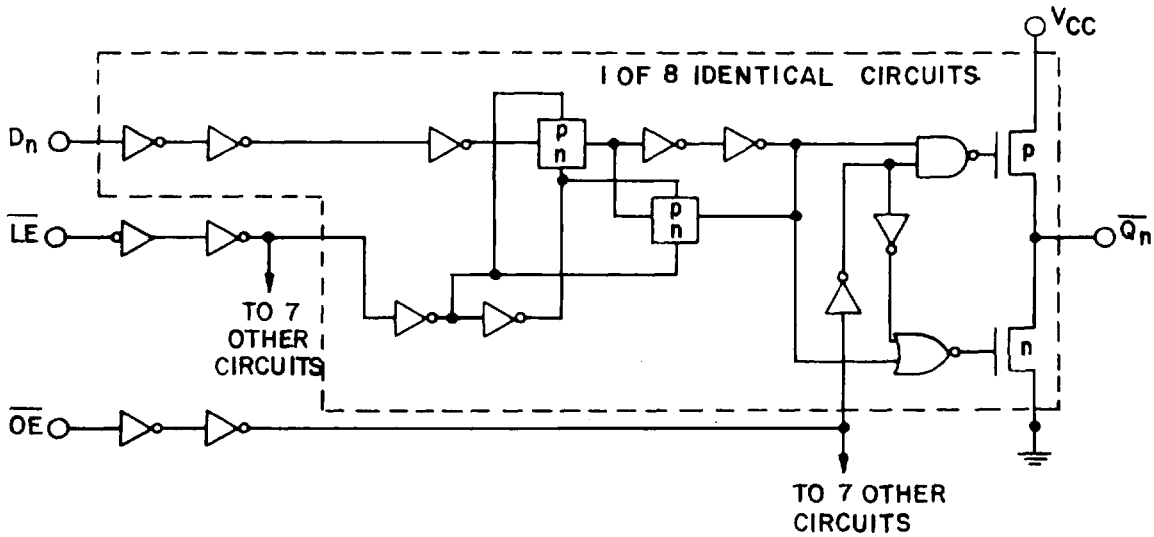

FIGURE 3. Logic diagram

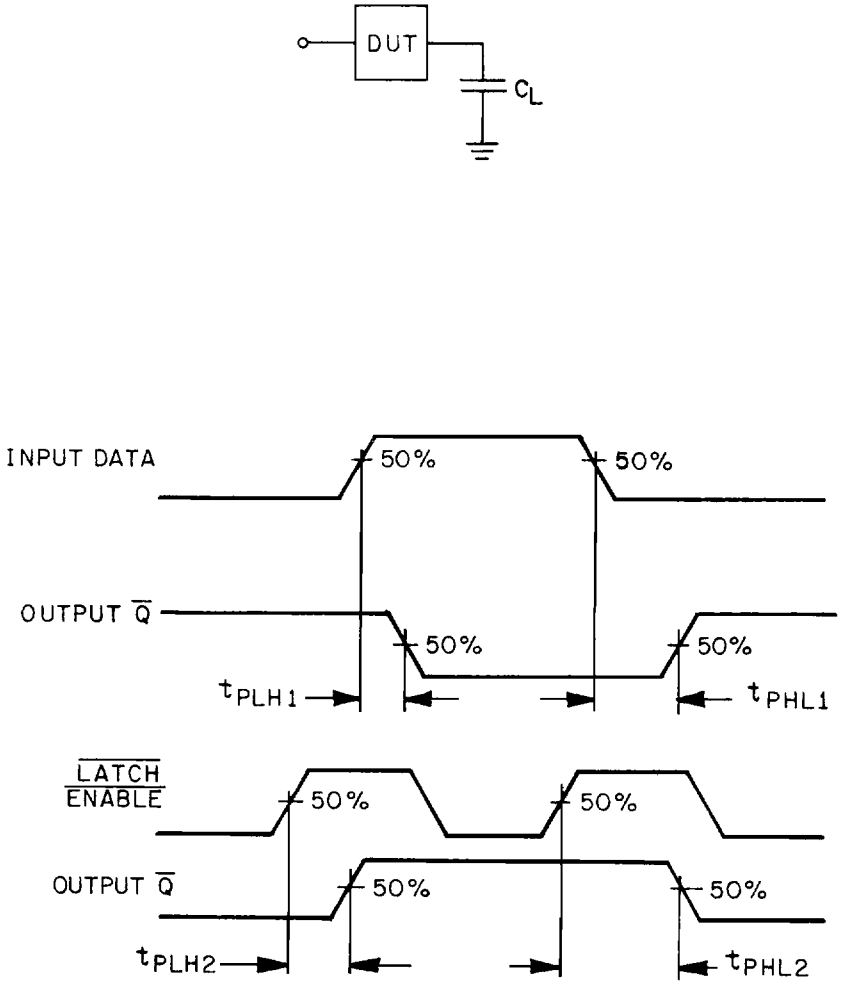

FIGURE 4. Test circuits and switching waveforms.

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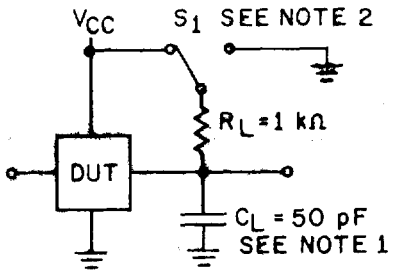

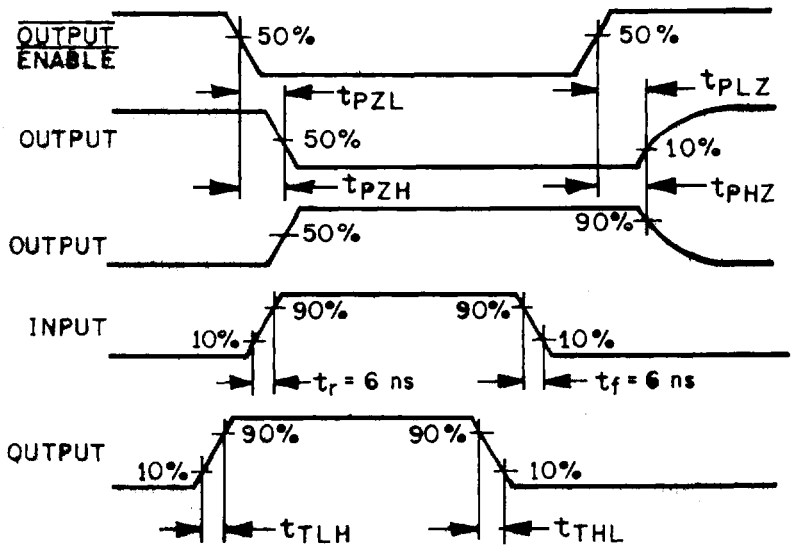

NOTES:
1. C_L includes load and test jig.
2. S_1 = V_{CC} for t_{PZL} and t_{PLZ}.
   S_1 = GND for t_{PZH} and t_{PHZ}.

FIGURE 4. Test circuits and switching waveforms - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with 0 failures.

d. Subgroup 7 tests sufficiently to verify the truth table.

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4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,9
Group A test requirements (method 5005)	1,2,3,4,7,9, 10**,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/65405B--.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8606201RX	27014 18714 01295	MM54HC563J/883 CD54HC563F/3A SNJ54HC563J	M38510/65405BRX
5962-8606201SX	01295	SNJ54HC563W	M38510/65405BSX
5962-86062012X	01295 27014	SNJ54HC563FK MM54HC563E/883	M38510/65405B2X

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8090
18714	RCA Corporation Solid State Division Route 202 Somerville, NJ 08876
01295	Texas Instruments, Incorporated P. O. Box 6448 Midland, TX 79701

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