Rochester Electronics

Datasheet

PART NUMBER

93425DMB-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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National Semiconductor

93425/93L425
1024 x 1-Bit Static Random Access Memory

General Description

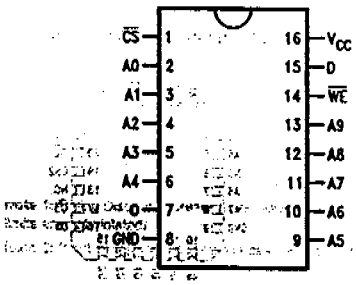
The 93425 is a 1024-bit read write Random Access Memory (RAM), organized 1024 words by one bit. It is designed for high speed cache control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output as well as an active LOW Chip Select line.

Features

- Commercial address access time 953425—20 to 60 ns max
- Military address access time 93425—30 to 70 ns max
- Low power version also available (93L425)
- Features TRI-STATE® output
- Power dissipation decreases with increasing temperature
- Standard processing includes burn-in

Connection Diagram

16-Pin DIP



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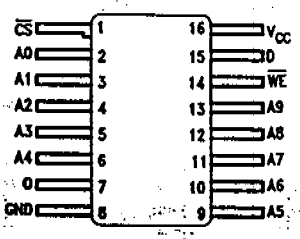
Top View

Order Number 93425DC, 93425ADC, 93425DC25, 93425DMQB, 93425DMQB40, 93425DMQB50, 93425PC, 93425APC, 93425PC25, 93L425DC, 93L425ADC, 93L425DC25, 93L425DMQB, 93L425DMQB40, 93L425DMQB50, 93L425PC, 93L425APC or 93L425PC25
See NS Package Number J16A* or N16E*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Flatpak



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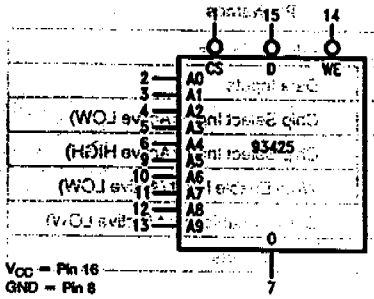
Top View

Order Number 93425FMQB, 93425AFMQB, 93L425FMQB40, 93L425FMQB, 93L425AFMQB or 93L425FMQB50
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Logic Symbol



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Pin Names

$\overline{CS}$	Chip Select (Active LOW)
A_0–A_9	Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
D	Data Input
O	Data Output

TABLE 5

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA
Input Current (DC)	−12 mA to +5.0 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	
Commercial	5.0V ±5%
Military	5.0V ±10%
Case Temperature (T_C)	
Commercial	0°C to +75°C
Military	−55°C to +125°C

DC Electrical Characteristics Over operating temperature ranges (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1			V	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Max, I_{OH} = −5.2 mA
I_{IL}	Input LOW Current		−180	−300	μA	V_{CC} = Max, V_{IN} = 0.4V
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = Max, V_{IN} = 4.5V
I_{IHB}	Input Breakdown Current			1.0	mA	V_{CC} = Max, V_{IN} = V_{CC}
V_{IC}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, V_{IN} = −10 mA
I_{OZH} I_{OZL}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4V V_{CC} = Max, V_{OUT} = 0.5V
I_{OS}	Output Current Short Circuit to Ground (Note 7)			−100	mA	V_{CC} = Max, (Note 7)
I_{CC}	Power Supply Current		60	~~65~~ 75 ~~125~~ ~~135~~	~~mA~~ mA ~~mA~~ ~~mA~~	~~93L425 Commercial~~ 93L425 Military ~~93425 Commercial~~ ~~93425 Military~~

Note 1: Either input voltage limit or input current limit is sufficient to protect the inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, T_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} = $V_{OL\ Max}$ (0.45V), V_{IH} = $V_{OH\ Min}$ (2.4V).

Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

TABLE 5

93425/93L425

Commercial

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	93L425-35		93L425-45 93L425A		93L425-60 93L425		Units
			Min	Max	Min	Max	Min	Max	
READ TIMING									
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b)*		25		30		40	ns
t_{ZRCS}	Chip Select to HIGH Z			25		30		40	ns
t_{AA}	Address Access Time (Note 8)			35		45		60	ns
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figures 4a, 4b)*	30		35		45		ns
t_{WSD}	Data Setup Time prior to Write		5		5		5		ns
t_{WHD}	Data Hold Time after Write		5		5		5		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		5		5		10		ns
t_{WHA}	Address Hold Time after Write		5		5		5		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		5		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			20		25		45	ns
t_{WR}	Write Recovery Time			30		35		45	ns

Military

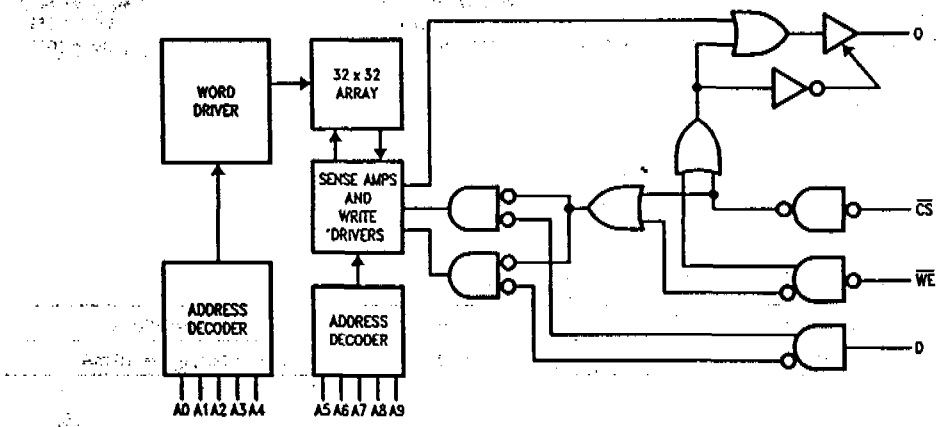
AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±10%, GND = 0V, T_C = −55°C to +125°C

Symbol	Parameter	Conditions	93L425-40		93L425-50 93L425A		93L425-70 93L425		Units
			Min	Max	Min	Max	Min	Max	
READ TIMING									
t_{ACS}	Chip Select Access Time	*(Figures 3a, 3b)*		30		35		45	ns
t_{ZRCS}	Chip Select to HIGH Z			25		30		50	ns
t_{AA}	Address Access Time (Note 8)			40		50		70	ns
WRITE TIMING									
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*(Figures 4a, 4b)*	35		40		50		ns
t_{WSD}	Data Setup Time prior to Write		5		5		10		ns
t_{WHD}	Data Hold Time after Write		5		5		10		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		10		10		10		ns
t_{WHA}	Address Hold Time after Write		5		5		10		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		5		10		ns
t_{WHCS}	Chip Select Hold Time after Write		5		5		5		ns
t_{ZWS}	Write Enable to HIGH Z			25		30		45	ns
t_{WR}	Write Recovery Time			25		40		55	ns

TABLE 5

93425/93L425

Logic Diagram



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Functional Description

The 93425 is a fully decoded 1024-bit read write Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address A0–A9.

One Chip Select input is provided for easy memory array expansion of up to 2048 bits without the need for external decoding. For larger memories the fast chip select access time permits direct address decoding without an increase in overall memory access time.

The read and write functions of the 93425 are controlled by the state of the active LOW Write Enable $\overline{WE}$ input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D is written into the location specified by the binary address present at A0 through A9. Since the write function is level triggered, data must be held stable at the data input for at least $t_{WSD(min)}$ plus $t_{W(min)}$ plus $t_{WHD(min)}$ to insure a valid write. When $\overline{WE}$ is held HIGH and the chip selected, data is read from the addressed location and presented at the output O.

The 93425 has a three-state output which provides active pull-up or pull-down when enabled and a high impedance (HIGH Z) state when disabled. The active pull-up provides drive capability for high capacitive loads while the high impedance state allows optimization of word expansion in bus organized systems.

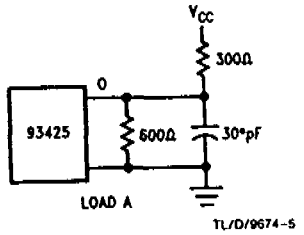
Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D	O	
H	H	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write 0
L	L	H	HIGH Z	Write 1
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level: 2.4V
L = LOW Voltage Level: 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High Impedance State

Logic Symbol

TABLE 5



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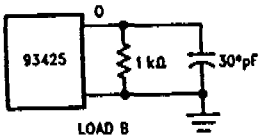

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Note: Load A is used for all production testing.
*Includes jig and probe capacitance

FIGURE 1. AC Test Output Load

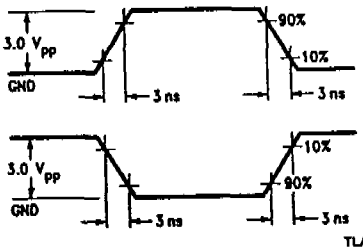

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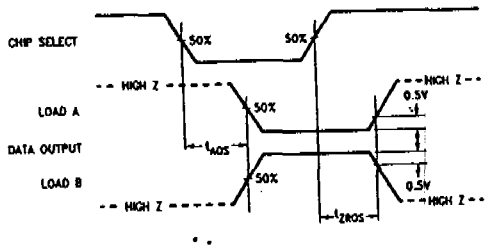
FIGURE 2. AC Test Input Levels



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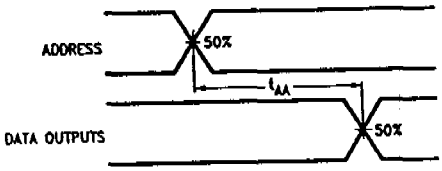
3a. Read Mode Propagation Delay from Chip Select



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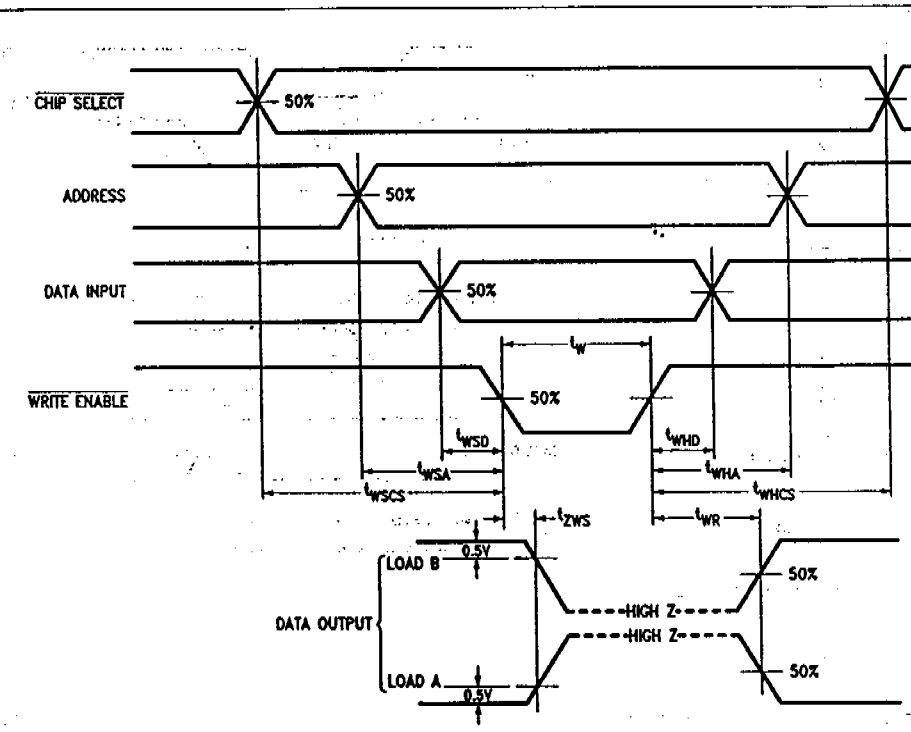
3b. Read Mode Propagation Delay from Address

FIGURE 3. Read Mode Timing

TABLE 5



Note 1: Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0/0.0V.

FIGURE 4. Write Mode Timing