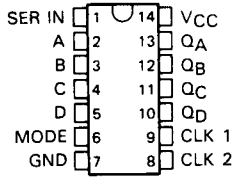
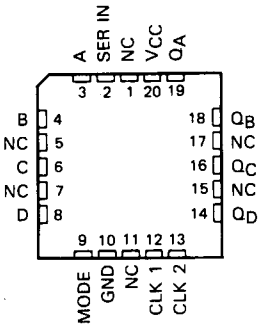
D2661, DECEMBER 1983–REVISED MAY 1986

- **Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **Right or Left Shifts**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS95 . . . J PACKAGE
SN74AS95 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS95 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These four-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the Clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of Clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of Clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.); and serial data is entered at input D. The clock input may be applied commonly to Clock 1 and Clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low. However, conditions described in the last three lines of the function table will also ensure that the register contents are protected.

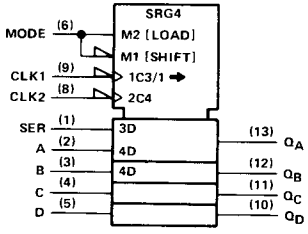
The SN54AS95 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS95 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

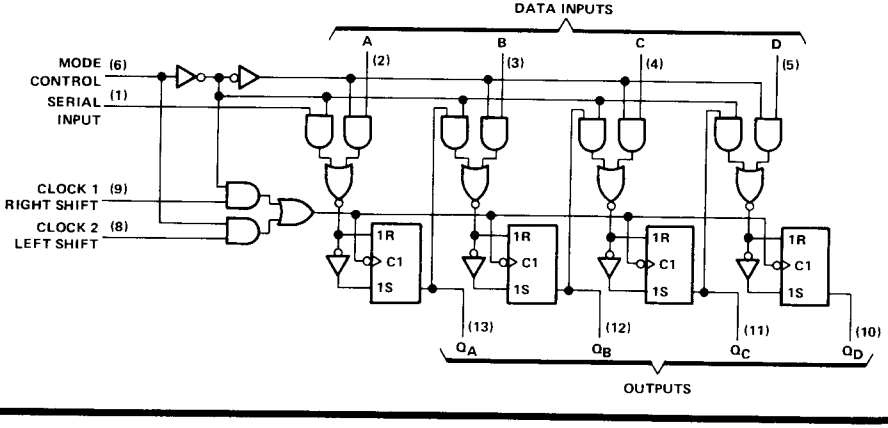
†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions).
↓ = transition from high to low level, ↑ = transition from low to high level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS95 . . . . . −55°C to 125°C
SN74AS95 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS95			SN74AS85			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		80	0		100	MHz
t_w	Pulse duration, CLK high or low		6.5			5			ns
t_{su}	Setup time, data before CLK↓		2.5			2			ns
t_h	Hold time after CLK↓ (see Figure 1)	Data	2.5			2.5			ns
		CLK 1 to Mode	3.5			3			
		CLK 2 to Mode	1			0			
t_{en}	Clock enable time (see Figure 1)	CLK 1	13			12			ns
		CLK 2	13			12			
t_{in}	Clock inhibit time (see Figure 1)	CLK 1	3			2.5			ns
		CLK 2	1			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS95			SN74AS95			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Mode	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.35 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	34		21	34	mA
I_{CCL}		V_{CC} = 5.5 V			26	39		26	39	mA

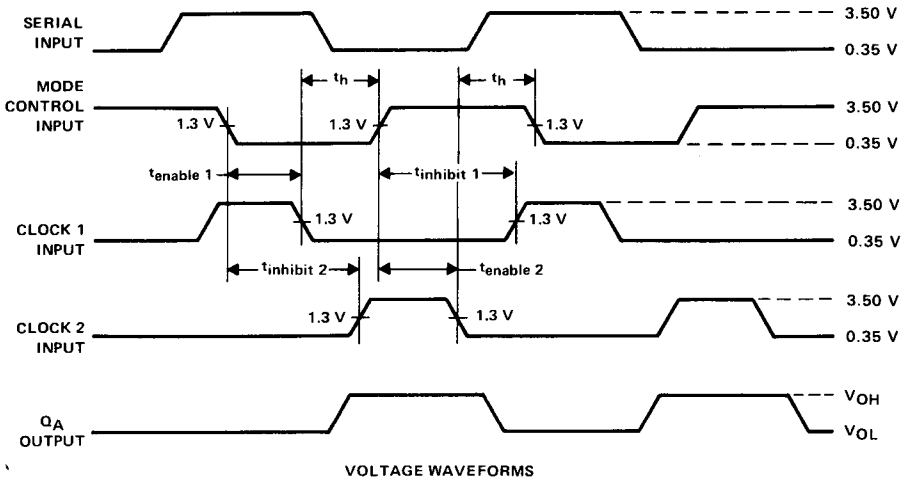
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristice (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS95		SN74AS95		
			MIN	MAX	MIN	MAX	
f_{max}			80		100		MHz
t_{PLH}	CLK	Q	2	11	2	10	ns
t_{PHL}			2	10.5	2	9.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 1–CLOCK ENABLE, INHIBIT, AND HOLD TIMES

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