

DM74S299 3-STATE 8-Bit Universal Shift/Storage Registers

General Description

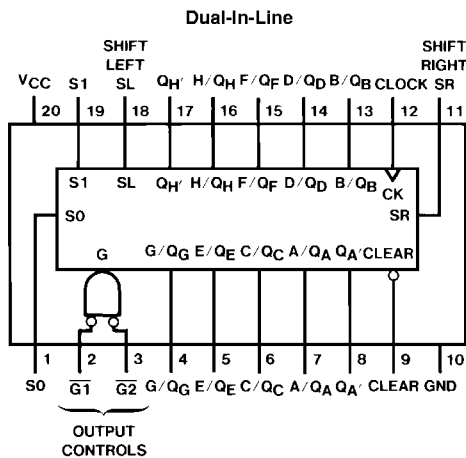
This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the 3-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
 - Hold (Store) Shift Left
 - Shift Right Load Data
- 3-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Operates with outputs enabled or at high Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

Connection Diagram



Order Number DM74S299N
See Package Number N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage
Input Voltage

7V
5.5V

Operating Free Air Temperature Range

DM74S
Storage Temperature Range

0°C to +70°C
-65°C to +150°C

Recommended Operating Conditions

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	DM74S299			Units
		Min	Nom	Max	
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	High Level Input Voltage	2			V
V _{IL}	Low Level Input Voltage			0.8	V
I _{OH}	High Level Output Current (Q _A thru Q _H)			-6.5	mA
	High Level Output Current (Q _A , Q _H)			-0.5	
I _{OL}	Low Level Output Current (Q _A thru Q _H)			20	mA
	High Level Output Current (Q _A , Q _H)			6	
f _{CLK}	Clock Frequency (Note 3)	0	70	50	MHz
f _{CLK}	Clock Frequency (Note 4)	0	60	40	MHz
t _w	Pulse Width (Note 6)	Clock High	10		ns
		Clock Low	10		
		Clear Low	10		
t _{SU}	Setup Time (Notes 5, 6)	Select	15↑		ns
		Data High	7↑		
		Data Low	5↑		
t _H	Hold Time (Notes 5, 6)	5↑			ns
t _{REL}	Clear Release Time (Note 6)	10↑			ns
T _A	Free Air Operating Temperature	0		70	°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 3: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 5: Data includes the two serial inputs and the eight input/output data lines.

Note 6: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.2	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max Q _A thru Q _H	2.4	3.2		V
		V _{IL} = Max, V _{IH} = Min Q _A , Q _H	2.7	3.4		
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max			0.5	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max V _I = 2.7V			100	μA
		A thru H, S0, S1			50	
I _{IL}	Low Level Input Current	V _{CC} = Max V _I = 0.5V			-2	mA
		Clock, Clear			-0.5	
		S0, S1			-0.25	
		Other				

Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied (Q_A thru Q_H)	$V_{CC} = \text{Max}$, $V_O = 2.4V$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			100	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied (Q_A thru Q_H)	$V_{CC} = \text{Max}$, $V_O = 0.5V$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			-250	μA
I_{OS}	Short Circuit Output Current (Q_A thru Q_H)	$V_{CC} = \text{Max}$ (Note 8)	-40		-100	mA
	Short Circuit Output Current (Q_A , Q_H)	$V_{CC} = \text{Max}$ (Note 8)	-20		-100	
I_{CC}	Supply Current	$V_{CC} = \text{Max}$		140	225	mA

Note 7: All typicals are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$ (Note 10)				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	(Note 11)	50		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 10)	Clock to Q_A or Q_H		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 10)	Clock to Q_A or Q_H		20		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 10)	Clear to Q_A or Q_H		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q_A thru Q_H				24	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}1, \overline{G}2$ to Q_A thru Q_H				18	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}1, \overline{G}2$ to Q_A thru Q_H				18	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 9)	$\overline{G}1, \overline{G}2$ to Q_A thru Q_H		12			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 9)	$\overline{G}1, \overline{G}2$ to Q_A thru Q_H		12			ns

Note 9: $C_L = 5\text{ pF}$.

Note 10: $R_L = 1K\Omega$ for delays measured to Q_A and Q_H .

Note 11: For testing f_{MAX} all outputs are loaded simultaneously.

Function Table

Mode	Inputs						Inputs/Outputs								Outputs			
	Clear	Function Select		Output Control		Clock	Serial		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
		S1	S0	$\overline{G1}^\dagger$	$\overline{G2}^\dagger$		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected

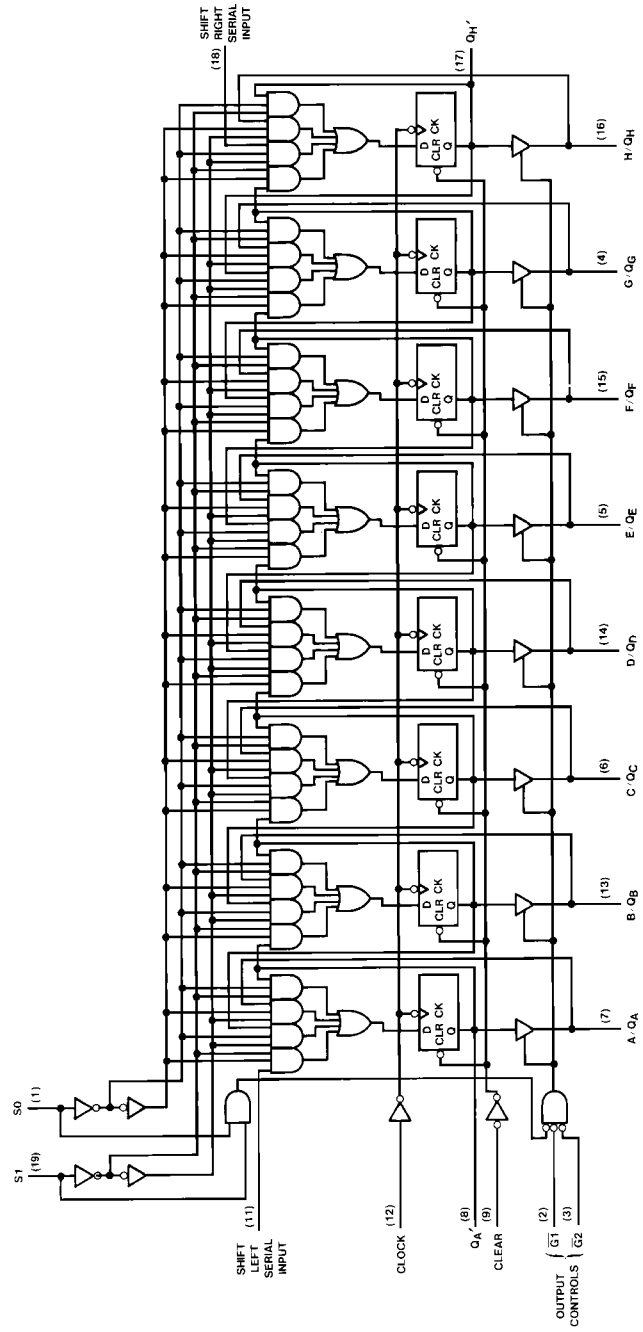
a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Q_{A0}...Q_{H0} = The output logic level of Q_x before the indicated input conditions were established.

H = high level, L = low logic level, X = either low or high logic level

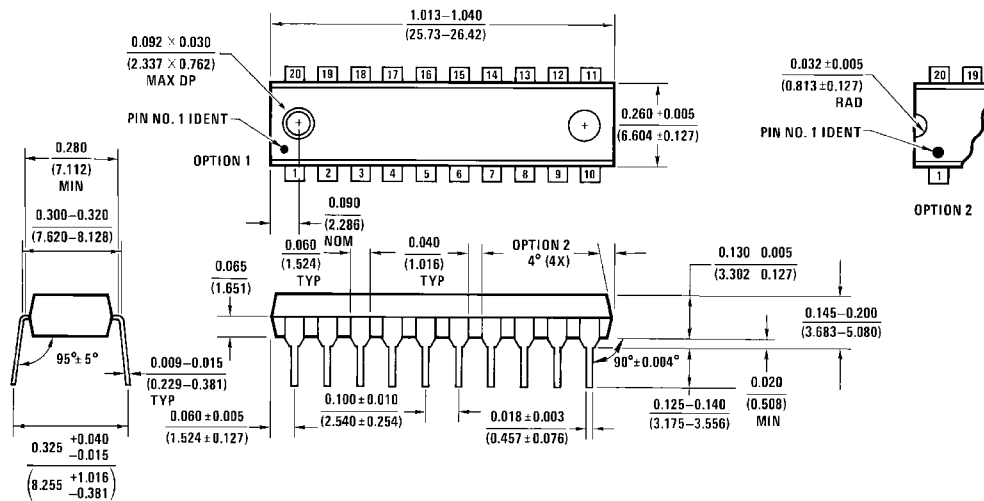
Q_{An}...Q_{Hn} = The output logic level before the active transition (↑) of the clock input.

Logic Diagram



DS006485-2

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74S299N
Package Number N20A

N20A (REV G)

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