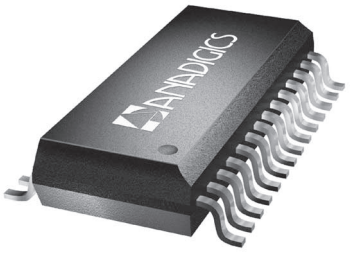
ACD2204

CATV/TV/Video Downconverter
with Dual Synthesizer

PRELIMINARY DATA SHEET - Rev 1.0

FEATURES

- Integrated Downconverter
- Integrated Dual Synthesizer
- 256 QAM Compatibility
- Single +5 V Power Supply Operation
- Low Noise Figure: 8 dB
- High Conversion Gain: 31 dB
- Low Distortion: -53 dBc
- Three-Wire Interface
- Small Size
- -40 °C to +85 °C



S8 Package
28 Pin SSOP

APPLICATIONS

- Set Top Boxes
- CATV Video Tuners
- Digital TV Tuners
- CATV Data Tuners
- Cable Modems

PRODUCT DESCRIPTION

The ACD2204 uses both GaAs and Si technology to provide the downconverter and dual synthesizer functions in a double conversion tuner gain block, local oscillator, balanced mixer, IF Amplifier, and dual synthesizer. The specifications meet the requirements of CATV/TV/Video and Cable Modem Data applications. The ACD2204 is supplied in a 28 lead SSOP package and requires a single +5 V supply voltage. The IC is well suited for applications where small size, low cost, low auxiliary parts count, and no-compromise performance is important. It provides for cost reduction by lowering the component and packaged IC count and decreasing the amount of labor-intensive production alignment steps, while significantly improving performance and reliability.

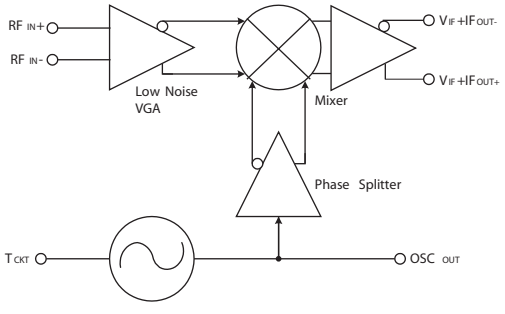


Figure 1: Downconverter Block Diagram

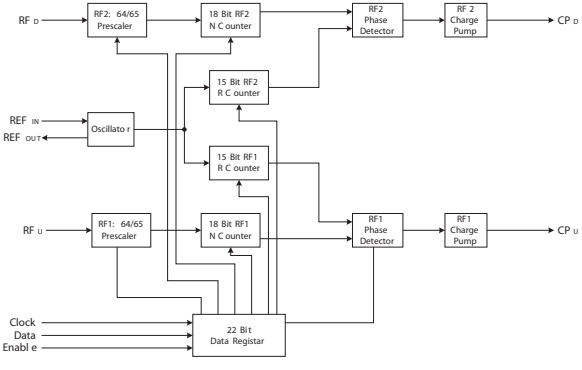


Figure 2: Dual Synthesizer Block Diagram

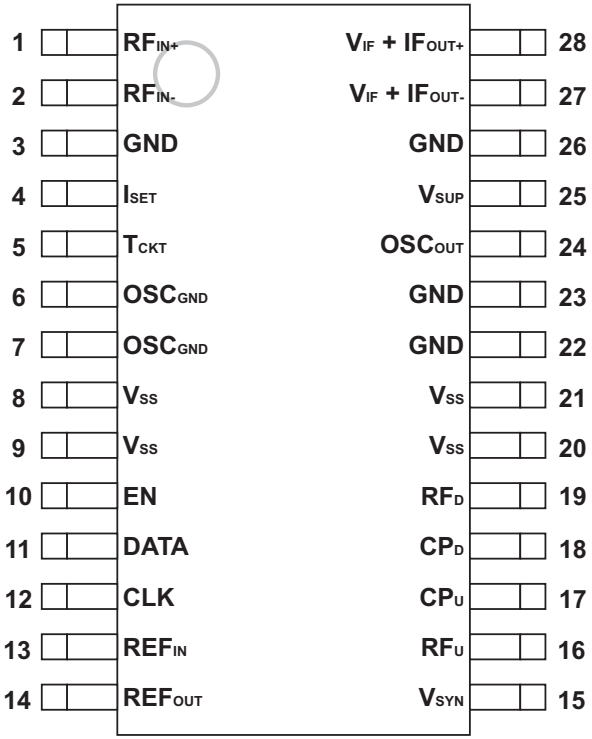


Figure 3: Pinout

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	RF_{IN+}	Downconverter Differential RFInput	28	V_{IF}+IF_{OUT+}	Differential IF Amplifier Output, Inductively coupled to +V_{DD}
2	RF_{IN-}	Downconverter Differential RFInput	27	V_{IF}+IF_{OUT} -	Differential IF Amplifier Output, Inductively coupled to +V_{DD}
3	GND	Downconverter Ground (Must be connected)	26	GND	Downconverter Ground (Must be connected)
4	I_{SET}	Downconverter Gilbert Cell Current Source Resistor	25	V_{SUP}	Downconverter Supply (+V_{DD})
5	T_{CKT}	Oscillator Input Port (Tank circuit connection)	24	OSC_{OUT}	Oscillator Output (Connected to Synthesizer RF Input)
6	OSC_{GND}	Oscillator Tank Circuit Ground (Not to be connected to any other circuit ground)	23	GND	Downconverter Ground (Must be connected)
7	OSC_{GND}	Same as Pin 6	22	GND	Downconverter Ground (Must be connected)
8	V_{SS}	Synthesizer Ground (Required)	21	V_{SS}	Synthesizer Ground (Required)
9	V_{SS}	Synthesizer Ground (Required)	20	V_{SS}	Synthesizer Ground (Required)
10	EN	3-Wire Interface Enable	19	RF_D	Synthesizer Downconverter RFInput
11	DATA	3-Wire Interface Data	18	CP_D	Synthesizer Downconverter Charge Pump Output
12	CLK	3-Wire Interface Clock	17	CP_U	Synthesizer Upconverter Charge Pump Output
13	REF_{IN}	Crystal Reference Input	16	RF_U	Synthesizer Upconverter RFInput
14	REF_{OUT}	Crystal Reference Output	15	V_{SYN}	Synthesizer Supply (+V_{DD})

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (pins 25, 27 & 28) (pin 15)	- -	+9 +6.5	VDC
Voltage on pins 10 through 14, 16 through 19 with V_{SS} = 0 V	-0.3	V_{SYN} +0.3	VDC
Input Voltages (pins 1, 2 & 5)	-	0	VDC
Input Power (pins 1 & 2) (pin 5) (pins 13, 16 & 19)	- - -	+10 +17 +20	dBm
Storage Temperature	-55	+150	° C
Soldering Temperature	-	260	° C
Soldering Time	-	4	Sec
Thermal Impedance, θ_{JC}	-	40	° C/W

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT
Downconverter Frequencies (1) RF Input (RF) IF Output (IF) Local Oscillator (LO)	 900 35 865	 - - -	 1200 150 1350	MHz
Synthesizer Frequencies Upconverter Synthesizer (RF_U) Downconverter Synthesizer (RF_D) Reference Oscillator (REF_{IN}) Phase Detector	 400 400 2 -	 - - 4 -	 2100 1400 20 10	MHz
Supply Voltage: V_{DD} (pins 15, 25, 27, 28)	+4.75	+5	+5.25	VDC
Ambient Operating Temperature: T_A	-40	-	+85	° C

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) Mixer operation is possible beyond these frequencies with slightly reduced performance.

Table 4: Electrical Specifications - Downconverter Section
(T_A = 25 °C, V_{DD} = +5 VDC, RF_{IN} = 1087 MHz, IF_{OUT} = 45 MHz)

PARAMETER	MIN	TYP	MAX	UNIT
Conversion Gain (1)	28	31	-	dB
SSB Noise Figure (1)	-	8	10	dB
Cross Modulation (1), (2), (4)	-	-59	-	dBc
3rd Order Intermodulation Distortion (IMD3) (1), (3), (4)	-	-	-53	dBc
2-Tone 3rd Order Input Intercept Point (IIP3) (1), (3), (4)	-10	-	-	dBm
LO Phase Noise (@ 10 KHz Offset) (1)	-	-90	-85.5	dBc/Hz
LO Output Power (pin 24) (1)	-	-5	-	dBm
Spurious @ IF Output				
LO Signals and Harmonics	-	-10	-	dBm
Beats Within Output Channel	-	-70	-	dBc
Other Beats from 2 to 200 MHz	-	-50	-	dBm
Other Spurious	-	-10	-	dBm
IF Supply Current (pin 27 & 28) (1), (4)	-	110	-	mA
Osc, Phase Splitter and Mixer Supply Current (pin 25)	-	70	-	mA
Power Consumption	-	900	-	mW

Notes:
(1) As measured in ANADIGICS test fixture.
(2) Two tones: 1085 and 1091 MHz, -40 dBm each, 1091 MHz tone AM-modulated 99% at 15 kHz.
(3) Two tones: 1085 and 1091 MHz, -30 dBm each.
(4) R1 = 0 Ohms

Table 5: Electrical Specifications - Synthesizer Section
(T_A = +25 °C, V_{DD} = +5 VDC)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Prescalar Input Sensitivity					(over operating frequency)
Upconverter: RF_U (pin 16) (1)	-7	-	+20	dBm	
Downconverter: RF_D (pin 19) (2)	-13	-	+20		
Reference Oscillator Sensitivity (pin 13)	-	0.5	-	V_{p-p}	
Charge Pump Output Current (3)					
SINK	-	1.25	-	mA	
SOURCE	-	-1.25	-		
Supply Current	-	35	50	mA	
Power Consumption	-	165	250	mW	

Notes:
(1) Measured at 250 kHz comparison frequency.
(2) Measured at 62.5 kHz comparison frequency.
(3) CP_U and CP_D = Vcc/2.

Table 6: Digital Interface Specifications
(T_A = 25 °C, V_{DD} = +5 VDC, ref. Figure 4)

PARAMETER	MIN	TYP	MAX	UNIT
Logic High Input: V_H (pins 10, 11, 12)	2.0	-	-	V
Logic Low Input: V_L (pins 10, 11, 12)	-	-	0.8	V
Logic Input Current Consumption (pins 10, 11, 12)	-	-	0.01	mA
Data to Clock Set Up Time: t_{CS}	50	-	-	ns
Data to Clock Hold Time: t_{CH}	10	-	-	ns
Clock Pulse Width High: t_{CWH}	50	-	-	ns
Clock Pulse Width Low: t_{CWL}	50	-	-	ns
Clock to Load Enable Setup Time: t_{ES}	50	-	-	ns
Load Enable Pulse Width: t_{EW}	50	-	-	ns
Rise Time: t_R	-	10	-	ns
Fall Time: t_F	-	10	-	ns

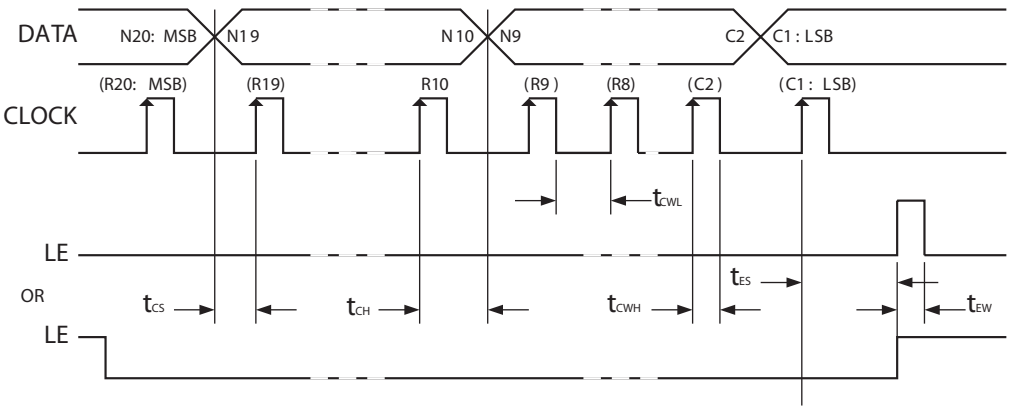


Figure 4: Serial Data Input Timing

PERFORMANCE DATA

Figure 5: Typical Upconverter Prescalar Sensitivity vs. Supply Voltage (T_A = +25 °C, f_{LO1} = 2100 MHz)

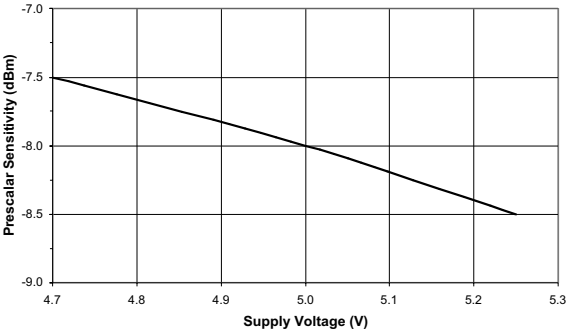


Figure 6: Typical Upconverter Prescalar Sensitivity vs. Local Oscillator Frequency (T_A = +25 °C, V_{DD} = +5 V)

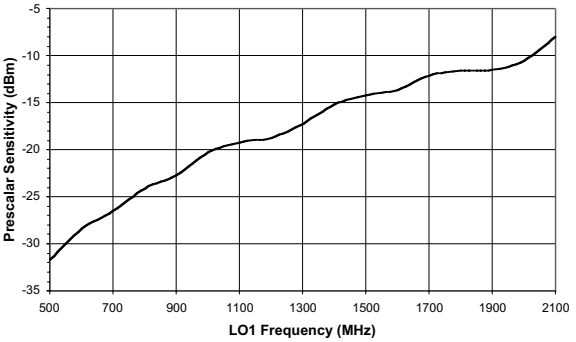


Figure 7: Typical Downconverter Prescalar Sensitivity vs. Supply Voltage (T_A = +25 °C, f_{LO2} = 1000 MHz)

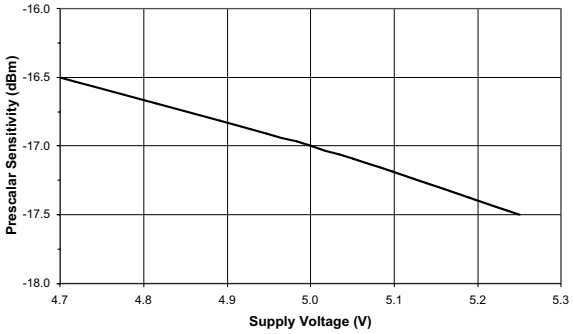


Figure 8: Typical Downconverter Prescalar Sensitivity vs. Local Oscillator Frequency (T_A = +25 °C, V_{DD} = +5 V)

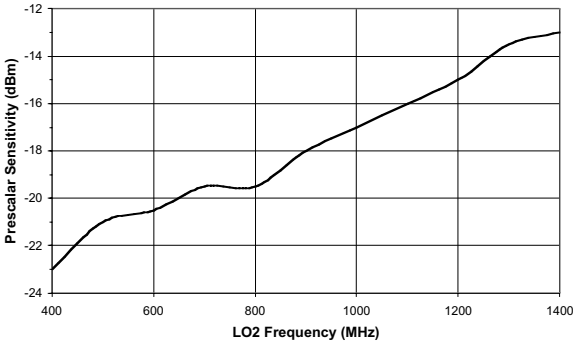
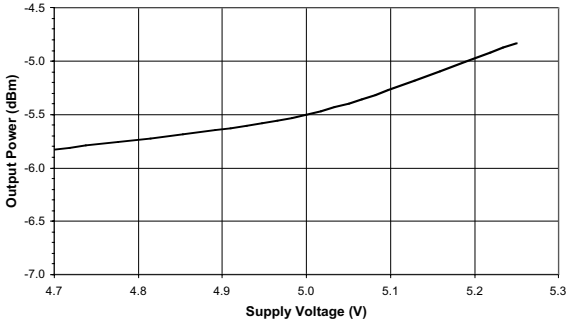


Figure 9: Typical Local Oscillator Output Power vs. Supply Voltage (T_A = +25 °C, f_{LO2} = 1042 MHz)



LOGIC PROGRAMMING

Synthesizer Register Programming

The ACD2204 includes two PLL synthesizers. Each synthesizer contains programmable Reference and Main dividers, which allow a wide range of local oscillator frequencies. The 22-bit registers that control the dividers are programmed via a shared three-wire bus, consisting of Data, Clock and Enable lines.

The data word for each register is entered serially in order with the most significant bit (MSB) first and the least significant bit (LSB) last. The rising edge of the Clock pulse shifts each data value into the register. The Enable line must be low for the duration of the data entry, then set high to latch the data into the register. (See Figure 4.)

Register Select Bits

The two least significant bits of each register are register select bits that determine which register is programmed during a particular data entry cycle. Table 7 indicates the register select bit settings used to program each of the available registers.

Table 7: Register Select Bits

SELECT BITS		DESTINATION REGISTER FOR SERIAL DATA
S 2	S 1	
0	0	Reference Divider Register for PLL2
0	1	Main Divider Register for PLL2
1	0	Reference Divider Register for PLL1
1	1	Main Divider Register for PLL1

Reference Divider Programming

The reference divider register for each synthesizer consists of fifteen divider bits, five program mode bits and the two register select bits, as shown in Table 8. The fifteen divider bits allow a divide ratio from 3 to 32767, inclusive, as shown in Table 9.

Table 8: Reference Divider Registers

MSB																			LSB	
22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Program Mode					Reference Divider Divide Ratio, R															Select	
D 5	D 4	D 3	D 2	D 1	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	S 2	S 1

Table 9: Reference Divider R Counter Bits

DIVIDE RATIO R	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes:
Divide ratios less than 3 are prohibited.

Main Divider Programming

The main divider register for each synthesizer consists of seven A counter bits, eleven B counter bits, two program mode bits and the two register select bits, as shown in Table 10. The main divider divide ratio, N, is determined by the values in the A and B counters. The eleven B Counter bits and allowed values are shown in Table 11, and the seven A Counter bits and allowed values are shown in Table 12. Note that there are some limitations on the ranges of the values for each counter.

Pulse Swallow Function

The VCO output frequency for the local oscillator is computed using the following equation; the variables are defined in Table 13:

$$f_{VCO} = N \times f_{osc}/R, \text{ where } N = [(P \times B) + A]$$

Table 10: Main Divider Registers

MSB **LSB**

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Program Mode		B Counter											A Counter							Select	
C 2	C 1	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1	A 7	A 6	A 5	A 4	A 3	A 2	A 1	S 2	S 1

Table 11: Main Divider B Counter Bits

VALUE OF B COUNTER	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
-	-	-	-	-	-	-	-	-	-	-	-
2047	1	1	1	1	1	1	1	1	1	1	1

Notes:
$B \geq A$, Divide ratios less than 3 are prohibited.

Table 12: Main Divider A Counter Bits

VALUE OF A COUNTER	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
-	-	-	-	-	-	-	-
127	1	1	1	1	1	1	1

Notes:
$B \geq A$, $A < P$

Table 13: Variable Definitions

VAR	DEFINITION
f_{VCO}	Desired output frequency of external voltage controlled oscillator (VCO)
B	Divide ratio of B counter (3 to 2047)
A	Divide ratio of A counter ($0 < A < P$, $A < B$)
f_{osc}	Frequency of external reference crystal or oscillator
R	Divide ratio of R counter (3 to 32767)
P	Preset modulus of prescalar (P = 64)

Programmable Modes

Each register contains bits set aside for programming different modes of operation in the synthesizers. Currently, the only programmable mode is the polarity of the phase detector in each of the synthesizers. Bit D1 in each reference divider register controls this feature. Bits D2 through D5 in the reference divider registers and bits C1 and C2 in the main divider registers are reserved for future use, and have no current function. They can be set either high or low without affecting synthesizer performance.

Setting Phase Detector Polarity

Table 14 shows how bit D1 of each reference divider register controls the polarity of the phase detector associated with each PLL. The correct setting is determined by using Table 15 and Figure 10.

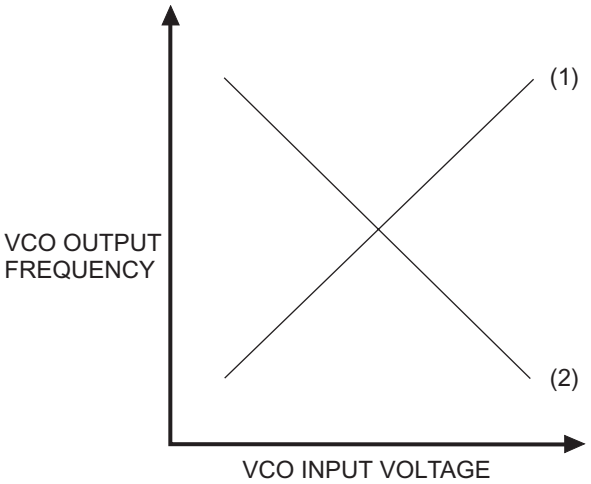
Table 14: Phase Detector Polarity Bit

S 2	S 1	D 1
0	0	PLL2 Phase Detector Polarity
1	0	PLL1 Phase Detector Polarity

Table 15: Phase Detector Polarity Selection

D 1	PHASE DETECTOR POLARITY	VCO CHARACTERISTICS (SEE FIGURE 12)
0	Negative	curve (2)
1	Positive	curve (1)

Figure 10: VCO Characteristics



Synthesizer Programming Example

The following example for programming the two synthesizers in the ACD2204 details the calculations used to determine the required value of each bit in all four registers:

Requirements

Desired CATV input channel: “HHH” - 499.25 MHz picture carrier (501 MHz digital channel center frequency)
(Second) IF picture carrier output frequency: 45.75 MHz (44 MHz digital channel center frequency)
First IF frequency: 1087.75 MHz
Phase detector comparison frequency for down converter (also tuning increment): 62.5 KHz
Phase detector comparison frequency for up converter: 250 KHz
Crystal reference oscillator frequency: 4 MHz

Calculation of Reference Divider Values

The value for each reference divider is calculated by dividing the reference oscillator frequency by the desired phase detector comparison frequency:

$$R = f_{OSC} / f_{PD}$$

For the down converter, the 4 MHz crystal oscillator frequency and the 62.5 KHz phase detector comparison frequency are used to yield R_{PLL2} = 4 MHz / 62.5 KHz = 64, and so the bit values for the down converter R counter are R_{PLL2} = 000000001000000.

For the up converter, the 4 MHz crystal oscillator frequency and the 250 KHz phase detector comparison frequency are used to yield R_{PLL1} = 4 MHz / 250 KHz = 16, and so the bit values for the up converter R counter are R_{PLL1} = 000000000010000.

Calculation of Main Divider Values

The values for the A and B counters are determined by the desired VCO output frequency for the local oscillator and the phase detector comparison frequency:

$$N = f_{VCO} / f_{PD} \qquad B = \text{trunc}(N / P) \qquad A = N - (B \times P)$$

The down converter local oscillator frequency will be 1087.75 MHz - 45.75 MHz = 1042 MHz in this example. The main divider ratio for the down converter, then, is N_{PLL2} = 1042 MHz / 62.5 KHz = 16672. Since P = 64 in the ACD2204, B_{PLL2} = trunc(16672 / 64) = 260, and A_{PLL2} = 16672 - (260 x 64) = 32. These results give bit values of B_{PLL2} = 00100000100 and A_{PLL2} = 0100000 for the B and A counters.

The up converter local oscillator frequency will be 499.25 MHz + 1087.75 MHz = 1587 MHz in this example. Therefore, N_{PLL1} = 1587 MHz / 250 KHz = 6348, B_{PLL1} = trunc(6348 / 64) = 99, and A_{PLL1} = 6348 - (99 x 64) = 12. These results give bit values of B_{PLL1} = 00001100011 and A_{PLL1} = 0001100 for the B and A counters.

Phase Detector Polarity

Assuming the VCO for the up converter has a negative slope, the phase detector polarity for PLL1 should be negative, and $D1_{PLL1}$ = 1. If the VCO for the down converter has a positive slope, the phase detector polarity for PLL2 should be positive, and $D1_{PLL2}$ = 0.

In summary, for this example, the four register programming words are shown in Tables 16 and 17:

Table 16: PLL1 and PLL2 Reference Divider Register Bits for Synthesizer Programming Example

MSB LSB

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Program Mode		**Main Divider B Counter**											**Main Divider A Counter**							**Select**	
C 2	C 1	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1	A 7	A 6	A 5	A 4	A 3	A 2	A 1	S 2	S 1
0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0	1	1

Table 17: PLL1 and PLL2 Main Divider Register Bits for Synthesizer Programming Example

MSB LSB

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Program Mode					**Reference Divider R Counter**															**Select**	
D 5	D 4	D 3	D 2	D 1	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	S 2	S 1
0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

APPLICATION INFORMATION

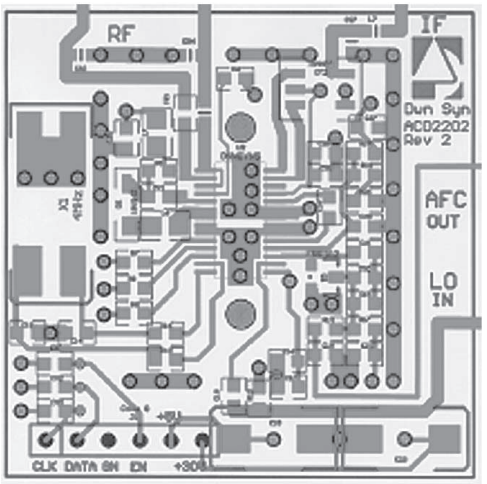


Figure 11: PC Board Layout Top View

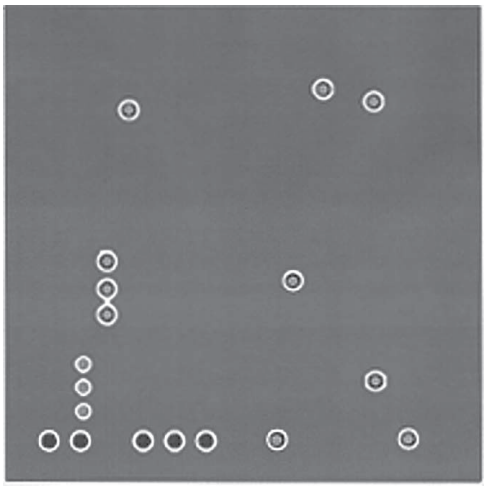


Figure 12: PC Board Layout Mid View

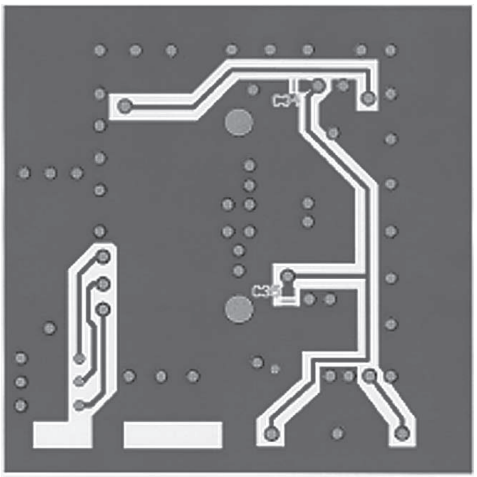


Figure 13: PC Board Layout Bottom View

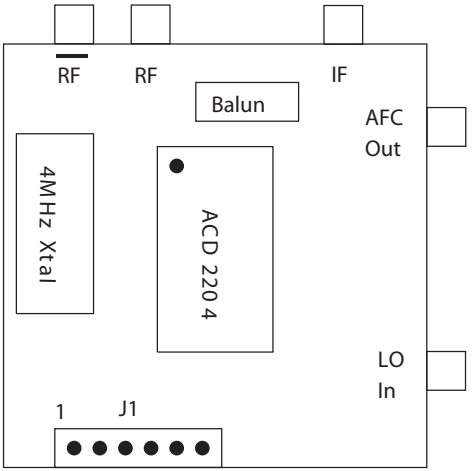


Figure 14: Evaluation Fixture

Table 18: J1 Header Pinout

PIN	FUNCTION
1	Clock
2	Data
3	Ground
4	Enable
5	+5 VDC
6	+30 VDC

Table 19: Fixture Pinout

PIN	FUNCTION
$\overline{RF}$	Downconverter $\overline{RF}$ Input
RF	Downconverter RF Input
IF	IF Output (Single Ended)
AFC Out	To Oscillator Tuning Circuit
LO In	Synthesizer RF_U Input

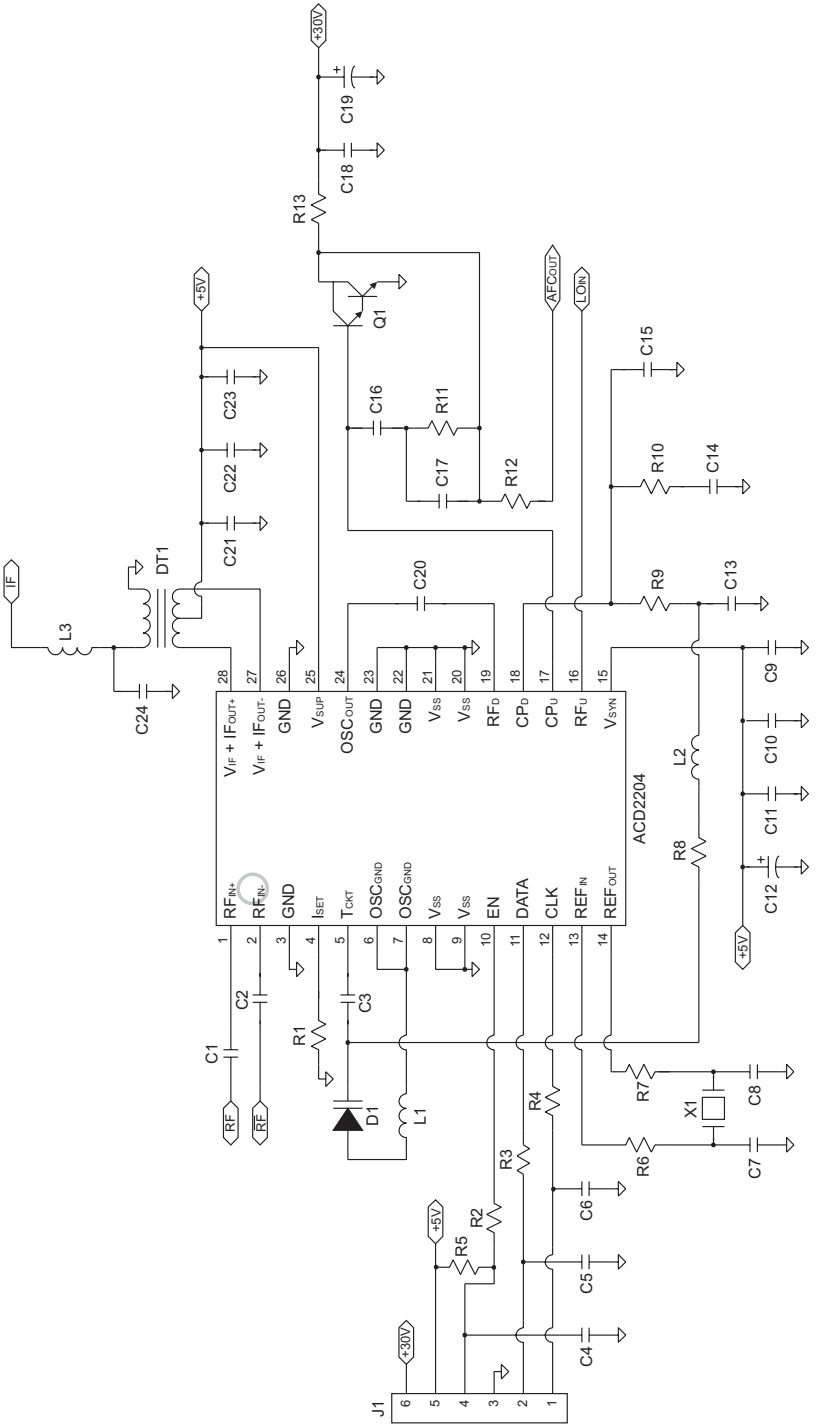


Figure 15: Evaluation Fixture Schematic

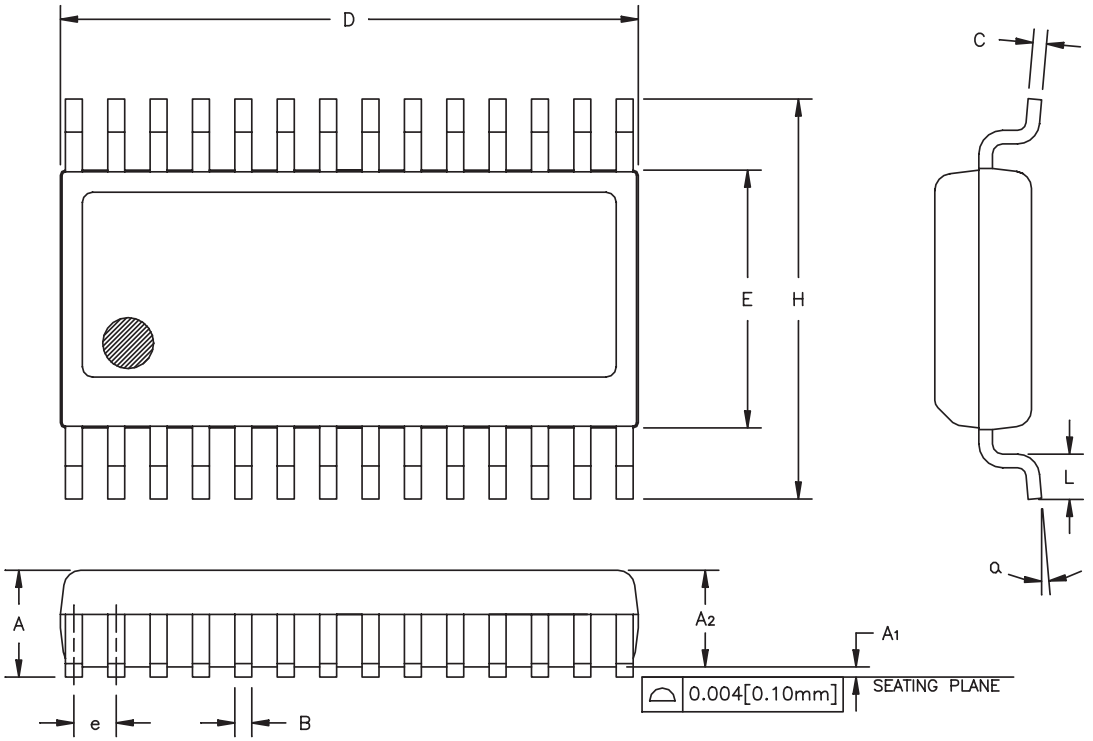
Table 20: Evaluation Fixture Parts List

ITEM #	VALUE	SIZE	DESCRIPTION	PART #	QTY	VENDOR
C1, C2, C20	100pF	0603	Chip-capacitor	GRM39COG101J50V	3	Murata
C3	9pF	0603	Chip-capacitor	GRM39COG090C50V	1	Murata
C7, C8	30pF	0603	Chip-capacitor	GRM39COG300J50V	2	Murata
C12	220uF	10V VA Series	Capacitor	PCE2040CT-ND	1	DIGI-KEY
C9, C11, C14, C21, C22	.1uF	0603	Chip-capacitor	GRM39Y5V104Z16V	5	Murata
C10, C23	1000pF	0603	Chip-capacitor	GRM39X7R102K50V	2	Murata
C15, C17	4700pF	0603	Chip-capacitor	GRM39X7R472K25V	2	Murata
C16	1uF	0603	Radial-lead Chip-capacitor	RPE113-X7R-105-K-050	1	Murata
C18	.01uF	0603	Chip-capacitor	GRM39X7R103K25V	1	Murata
C19	10uF	35 V TANT	TE Series Cap.	PCS6106CT-ND	1	DIGI-KEY
C24	15pF	0603	Chip-capacitor	GRM39COG150J50V	1	Murata
C13	5600pF	0603	Chip-capacitor	GRM39X7R562K50V	1	Murata
C4, C5, C6	33pF	0603	Chip-capacitor	GRM39COG330J50V	3	Murata
R8	51	0603	Chip Resistor	ERJ-3GSYJ510	1	Panasonic
R5	10K	0603	Chip Resistor	ERJ-3GSYJ103	1	Panasonic
R2, R3, R4	2K	0603	Chip Resistor	ERJ-3GSYJ202	3	Panasonic
R12	1K	0603	Chip Resistor	ERJ-3GSYJ102	1	Panasonic
R11	2.7K	0603	Chip Resistor	ERJ-3GSYJ272	1	Panasonic
R7	3K	0603	Chip Resistor	ERJ-3GSYJ302	1	Panasonic
R13	22K	0603	Chip Resistor	ERJ-3GSYJ223	1	Panasonic
R10	8.2K	0603	Chip Resistor	ERJ-3GSYJ822	1	Panasonic

Table 20: Evaluation Fixture Parts List continued

ITEM #	VALUE	SIZE	DESCRIPTION	PART #	QTY	VENDOR
R1, R6, R9	0	0603	Chip Resistor	ZC0603	3	RCD
L1	5.6nH	0805	Inductor	0805CS-050X-BC	1	Coilcraft
L2	68nH	0805	Inductor	0805CS-680X-BC	1	Coilcraft
L3	270nH	0805	Inductor	0805CS-271X-BC	1	Coilcraft
D1	1SV245		Varactor diode	1SV245	1	Toshiba
DT1	4:1		Transformer	ETC4-1-2	1	M/A-COM, Inc. North America
Q1	30V SMD	SOT-23	Transistor NPN Darl.	FMMTA13CT-ND	1	DIGI-KEY
X1	4MHZ		Crystal	SE2618CT-ND	1	DIGI-KEY

PACKAGE OUTLINE



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.053	0.069	1.35	1.75	
A1	0.004	0.010	0.10	0.25	
A2	–	0.059	–	1.50	
B	0.008	0.012	0.20	0.30	
C	0.007	0.010	0.18	0.25	
D	0.386	0.394	9.80	10.00	2
E	0.150	0.157	3.81	3.98	3
e	0.025 BSC		0.64 BSC		4
H	0.228	0.244	5.79	6.19	
L	0.016	0.050	0.40	1.27	
α	0°	8°	0°	8°	

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ±0.0035 [0.089mm].
5. REFERENCE JEDEC MO–137 AF.

Figure 16: S8 Package Outline - 28 Pin SSOP

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ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
ACD2204S8P1	-40° C to +85° C	28 Pin SSOP	Tape & Reel, 3500 pieces per reel
ACD2204S8P0	-40° C to +85° C	28 Pin SSOP	Tubes, 50 pieces per tube

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