19-1166; Rev 0; 12/96

MAXIM

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

General Description

The MAX1101 is a highly integrated IC designed primarily for digitizing the output of a linear CCD array. It provides the components required for all necessary analog functions, including clamp circuitry for black-level correction or correlated double sampling (CDS), a three-input multiplexer (mux), and an 8-bit analog-to-digital converter (ADC).

The MAX1101 operates with a sample rate up to 1MHz and with a wide range of linear CCDs. The logic interface is serial, and a single input sets the bidirectional data line as either data in or data out, thus minimizing the I/O pins required for communication.

Packaged in a 24-pin SO, the MAX1101 is available in the commercial (0°C to +70°C) temperature range.

Features

- ♦ **1.0 Million Pixels/sec Conversion Rate**
- ♦ **Built-In Clamp Circuitry for Black-Level Correction or Correlated Double Sampling**
- ♦ **64-Step PGA, Programmable from Gain = -2 to -10**
- ♦ **Auxiliary Mux Inputs for Added Versatility**
- ♦ **Compatible with a Large Range of CCDs**
- ♦ **8-Bit ADC Included**
- ♦ **Space-Saving, 24-Pin SO Package**

Applications

Scanners

Fax Machines

Digital Copiers

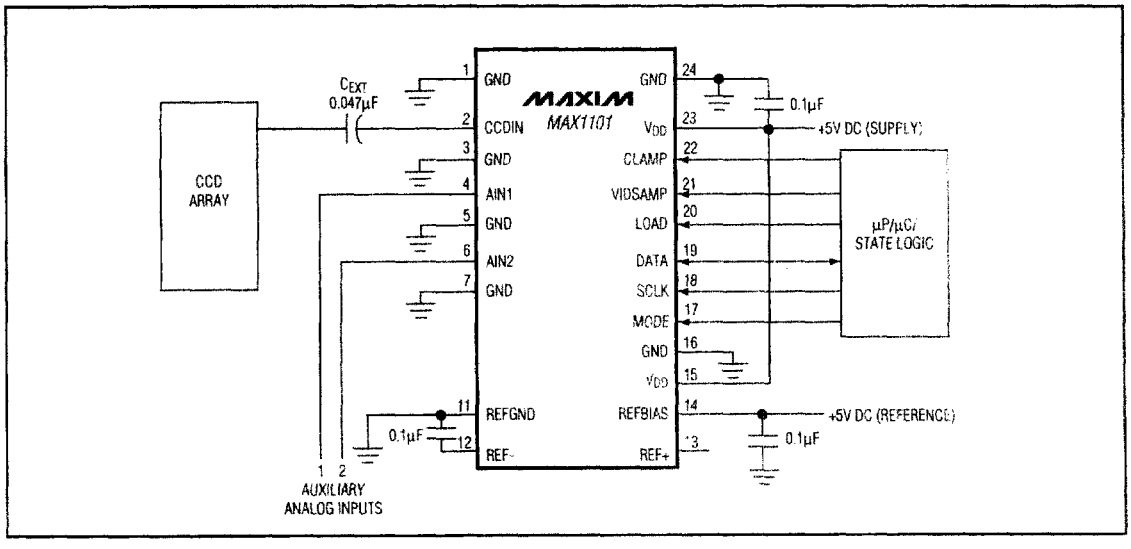
CCD Imaging

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1101CWG	0°C to +70°C	24 Wide SO

Pin Configuration appears on last page.

Typical Operating Circuit



Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +12V
All Pins to GND .....-0.3V to (V_{DD} + 0.3V)
Current into Every Pin (except V_{DD}) .....±20mA
Current into V_{DD} .....±50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 11.76mW/°C above +70°C) 941mW

Operating Temperature Range .....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = $V_{REFBIAS}$ = +4.75V to +5.25V, REFGND = 0V, REF- bypassed to REFGND with 0.1µF, C_{EXT} = 47nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG-TO-DIGITAL CONVERTER							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±0.5	±1	LSB
Integral Nonlinearity	INL	Best straight-line fit			±1	±1.5	LSB
Total Unadjusted Error	TUE					±2.5	LSB
Zero-Scale Drift	TCVOS				125		%µV/°C
Full-Scale Drift	TCFS				0.016		%FS/°C
Maximum Sample Rate	f_S			0.67	1.2		MHz
Minimum Sample Rate		(Note 1)		1			kHz
Input Full-Power Bandwidth		V_{IN} = 2.5Vp-p			1		MHz
Aperture Delay	t_{AP}				10		ns
ANALOG INPUT—CCD INTERFACE							
Maximum Peak CCD Differential Signal Range	V_{WHITE}	V_{WHITE} = (V_{REF+} - V_{REF-}) / G_{PGA}	G_{PGA} = -2		1.25		V
			G_{PGA} = -10		0.25		
Minimum PGA Gain Setting				-1.9	-2	-2.1	V/V
Maximum PGA Gain Setting				-9.375	-9.875	-10.375	V/V
Gain Adjust Resolution					64		Steps
Gain Adjust Step Size					0.125		V/V
PGA Gain Error					±5		% Gain
Black Sample Switch On-Resistance	$R_{ON(BSS)}$				60	150	Ω
Input Leakage (Note 2)	$I_{L(CCDIN)}$	Including black sample switch off-leakage			1	50	nA
CCD Interface Offset Voltage	$V_{OS(CCD)}$	V_{VIDEO} = V_{RESET} (Figure 4)		0	4	8	LSB
ANALOG INPUT—AUXILIARY INPUTS							
Input Voltage Range	V_{IN}			V_{REF-}		V_{REF+}	V
Input Capacitance (Note 1)	$C_{IN(ON)}$	Channel on				45	pF
	$C_{IN(OFF)}$	Channel off				10	
On-Resistance	R_{ON}				120		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $V_{REFBIAS}$ = +4.75V to +5.25V, REFGND = 0V, REF- bypassed to REFGND with 0.1µF, C_{EXT} = 47nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE INPUT						
Positive Reference Voltage	V_{REF+}	Internally generated, $V_{REFBIAS}$ = 5V	2.94	3.00	3.06	V
Negative Reference Voltage	V_{REF-}	Internally generated, $V_{REFBIAS}$ = 5V	0.49	0.50	0.51	V
POWER SUPPLIES						
Positive Supply-Voltage Range	V_{DD}		4.75	5	5.25	V
PSRR, PGA and ADC	PSRR	4.75V ≤ V_{DD} ≤ 5.25V	48	60		dB
Supply Current	I_{DD}			20	40	mA
DIGITAL INPUTS/OUTPUTS						
Digital Input Voltage High	V_{IH}		3.5			V
Digital Input Voltage Low	V_{IL}				1.5	V
Digital Input Leakage Current	I_{IL}		-10		10	µA
Digital Output Voltage High	V_{OH}	I_{SOURCE} = 4mA	V_{DD} - 0.5			V
Digital Output Voltage Low	V_{OL}	I_{SINK} = 4mA			0.5	V
Digital Output Leakage Current	I_{OL}	Output in high-impedance mode	-10		10	µA
DIGITAL TIMING SPECIFICATIONS (t_r, t_f ≤ 10ns, C_L ≤ 50pF, unless otherwise noted)						
SCLK Frequency	f_{SCLK}				10	MHz
SCLK Pulse Width	t_{SPW}		50			ns
VIDSAMP Pulse Width	t_{VS}		500			ns
VIDSAMP to CLAMP Separation	t_{VB}		50			ns
LOAD Pulse Width	t_{LD}		50			ns
VIDSAMP Fall to SCLK Rise Time	t_{VLS}	MODE = 1	50			ns
VIDSAMP Fall to DATA	t_{VLD}	MODE = 1			60	ns
VIDSAMP to Reset Separation	t_{VR}	(Note 2)	50			ns
Reset to CLAMP Separation	t_{RB}	(Note 2)	50			ns
SCLK Rise to DATA	t_{SD}				60	ns
DATA Set-Up Time	t_{DSU}		20			ns
DATA Hold Time	t_{DH}		20			ns
LOAD Fall to SCLK Rise Time	t_{LS}	MODE = 0	50			ns
SCLK Rise to LOAD Rise Time	t_{SL}	MODE = 0	50			ns
MODE Setup Time	t_{MSU}	Same as bus-relinquish time	50			ns
CLAMP Pulse Width	t_{BS}		300			ns
CLAMP Fall to Video Update	t_{BC}	(Note 1)	20			ns
Digital Quiet Time (Note 3)	t_Q	± around VIDSAMP falling edge	20			ns

Note 1: Due to leakage in the PGA and ADC, operation at sample rates below 1ksps is not recommended, as performance may degrade, particularly at high temperatures.

Note 2: Production test equipment settling time prohibits leakage measurements below 1nA. Lab equipment has shown the MAX1101 switch input leakage below 1pA at T_A = +25°C, and below 50pA at T_A = +70°C.

Note 3: Not a test parameter. Recommended for optimal performance.

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Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 10, 16, 24	GND	Ground
2	CCDIN	CCD Input. Connect CCD through a series 0.047µF capacitor (C_{EXT}).
4	AIN1	Auxiliary Analog Input Channel 1
6	AIN2	Auxiliary Analog Input Channel 2
8, 9, 10	I.C.	Internally Connected. Do not connect to this pin.
11	REFGND	Reference Ground. Ground reference for all analog signals.
12	REF-	Lower Limit of Reference Span. Sets the zero-code voltage. Range is GND ≤ REF- ≤ REF+. Nominally 0.5V.
13	REF+	Upper Limit of Reference Span. Sets the full-scale input. Voltage range is REF- ≤ REF+ ≤ V_{DD}. Nominally 3.0V.
14	REFBIAS	Reference Power Supply. Connect to external +5.0V to set V_{REF+} to +3.0V and V_{REF-} to +0.5V.
15, 23	V_{DD}	Power Supply, +5V. Bypass to ground very close to the device and connect the two pins together, close to the MAX1101.
17	MODE	Control Input. Set high, DATA is an output of the ADC. Set low, DATA enables programming of the PGA and mux.
18	SCLK	Serial Clock Input
19	DATA	Data Input or Output, as controlled by MODE
20	LOAD	Control Input. Loads serial shift-register data to PGA and multiplexer registers when MODE = 0.
21	VIDSAMP	Control Input. Samples the video level and initiates the ADC conversion.
22	CLAMP	Control Input. Samples black level. Can be used for correlated double sampling.

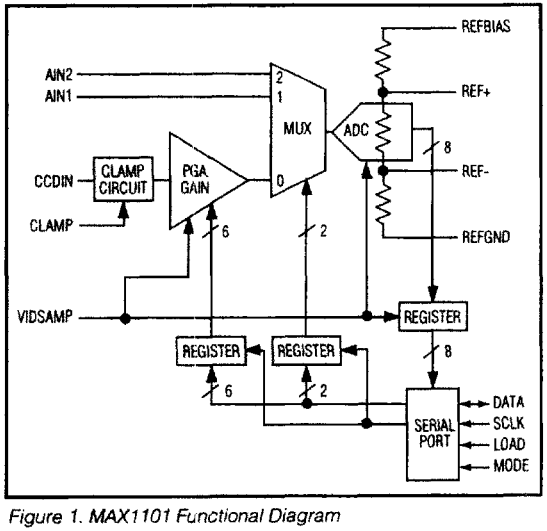

Figure 1. MAX1101 Functional Diagram

Detailed Description

Overview

The MAX1101 directly processes the pixel stream from a monochrome CCD, and removes black level, offset, and noise errors through an internal clamp circuit, which can be used as a correlated double sampler (CDS). It uses a 6-bit, programmable-gain amplifier (PGA) to adjust gain. A three-input multiplexer (mux) selects either the PGA output or two unassigned inputs (AIN1, AIN2). The processed analog signal is digitized by an 8-bit, half-flash analog-to-digital converter (ADC), and output serially through the DATA pin.

Digital data is input and output through the bidirectional serial pin (DATA) synchronously with the external serial clock (SCLK). When MODE = 0, the mux channels and the PGA gain can be programmed via DATA. With MODE = 1 (high), ADC serial data is output through this pin.

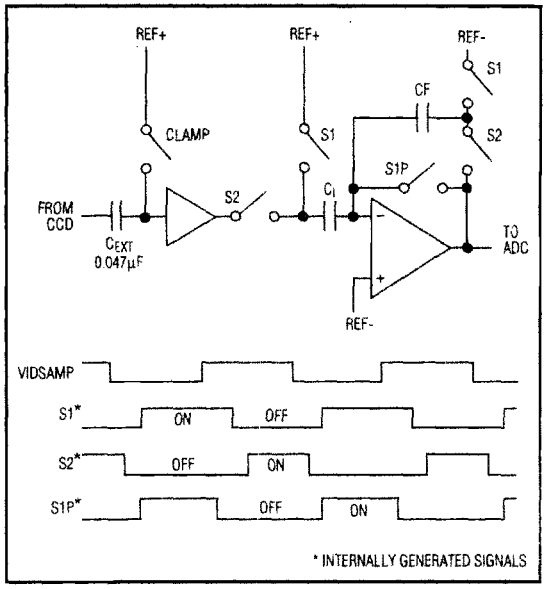

Figure 2. PGA Functional Diagram

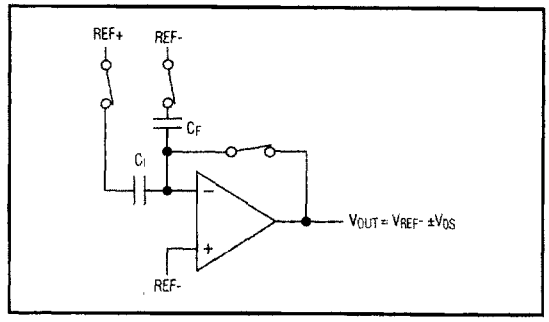

Figure 3a. PGA Connection with VIDSAMP = Low

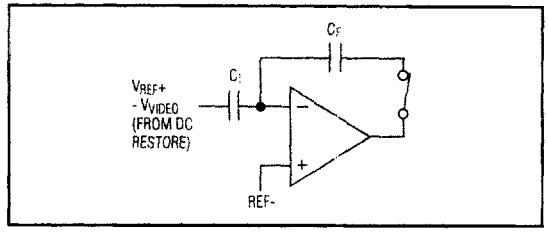

Figure 3b. PGA Connection with VIDSAMP = High

Programmable-Gain Amplifier

The PGA amplifies the differential video signal from the CCD (at CCDIN). Gain is settable with the 6-bit control word from -2 to -10 in 64 steps, in increments of -0.125. The PGA also provides for periodic DC restoration of the capacitively coupled input.

As shown in Figure 2, the switched-capacitor amplifier's gain is set by the ratio C_I/C_F. The input is sampled on the C_I capacitors, which is a set of equal capacitors. The 6-bit gain control word determines the number of capacitors used. Thus the PGA gain is set from -2 to -10.

A voltage equal to V_{REF-} is applied to the PGA's noninverting input. This offsets the PGA output to be within the range of the ADC (V_{REF-} to V_{REF+}).

Clamp Circuit

As shown in Figure 2, the CCD output is connected to the MAX1101 input (CCDIN) through an external capacitor, which removes the potentially large DC common-mode voltages from the input signal. Whenever CLAMP is high, the CLAMP switch is closed and C_{EXT} is charged to V_{REF+}. It can be actuated either once per pixel (sampling reset level) or less frequently (such as for restoring optical black level once per line), as required by the application.

VIDSAMP controls the sampling of the video signal and offset nulling of the PGA. To null out the offset, VIDSAMP causes switches S1 and S1P to close, placing the amplifier in a unity-gain configuration, as shown in Figure 3a. This configuration causes the amplifier's offset voltage to be stored on CF. In the next portion of the cycle, when VIDSAMP returns low, the S1 switches are opened and S2 is closed (Figure 3b). This is the standard inverting op-amp configuration. The only difference is that capacitors are used to set the gain, and the amplifier's offset voltage has been stored on these capacitors and is thus canceled. The amplifier's output is $[C_F/C_I] \times V_{VIDEO} + V_{REF-}$. The CDS function is shown in Figure 4.

ADC

The ADC uses a recycling half-flash conversion technique in which a 4-bit flash ADC section achieves an 8-bit result in two steps (Figure 5). Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder (using REF+ and REF-) and provides the upper four data bits.

An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown voltage

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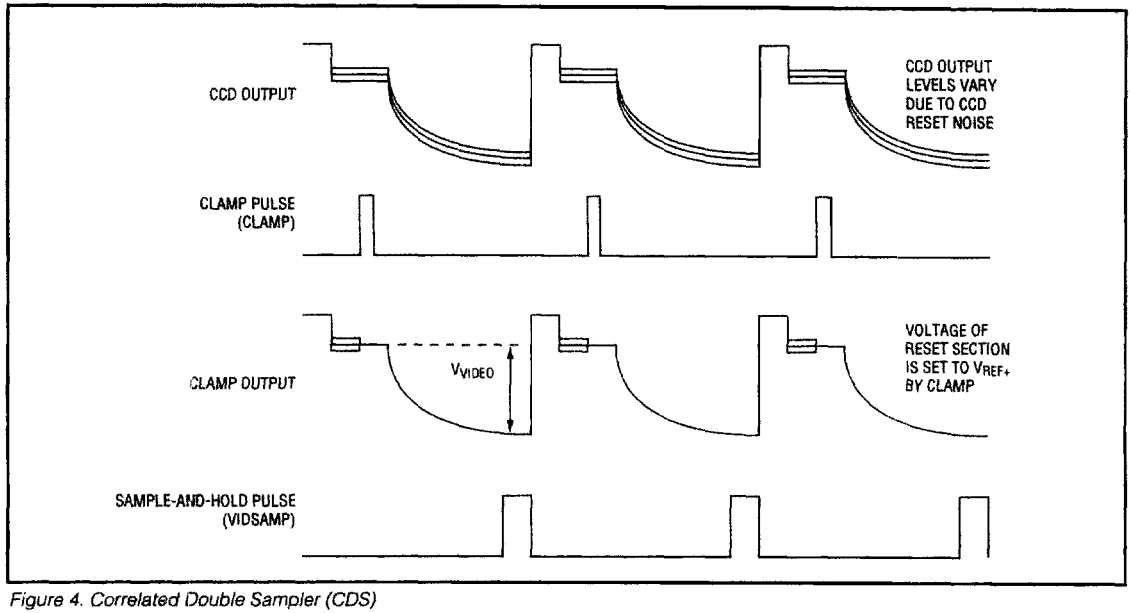

Figure 4. Correlated Double Sampler (CDS)

and the DAC output. The residue is then compared again with the flash comparators to obtain the lower four data bits.

Single-shot timers control the timing of the two conversion steps. Once both MSBs and LSBs have been determined, the comparators return to input-acquisition/auto-zero mode.

REF+ and REF-

The REF+ and REF- pins set the ADC's full-scale range. The optimum input range is +0.5V to +3.0V. Figure 6 shows a matched resistive ladder that generates the reference voltages. Four pins are available: REF+, REF-, REFBIAS, and REFGND. If 5.00V is applied to REFBIAS while REFGND is grounded, then 3.00V and 0.50V are generated at REF+ and REF-, respectively.

For increased accuracy or power-supply immunity, REF+ can be connected to an external +3.00V reference. If this is done, the accuracy must be better than ±5%. REFBIAS should be left open in this case.

Multiplexer

The mux selects either the output of the PGA or one of two other inputs to the ADC. The mux switching is break-before-make to prevent transient shorts between channels. The first two bits of the input control byte select the mux input channel (Table 1).

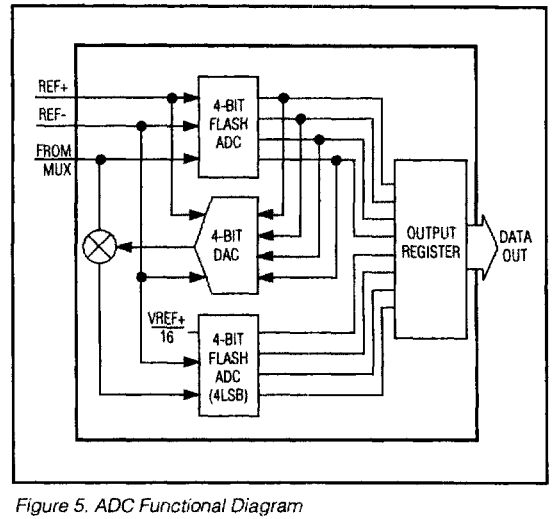

Figure 5. ADC Functional Diagram

Serial-Interface Logic

The serial interface inputs and outputs data in 8-bit words. The interface is controlled by four signals: MODE, LOAD, DATA, and SCLK.

MODE

MODE controls the direction of data transfer. When MODE = 0, data is being shifted into the MAX1101 at the DATA pin either for the mux or the PGA. When MODE = 1, the ADC output is shifted out from the MAX1101 at the DATA pin. Data is shifted in and out of the MAX1101 at the rising edge of SCLK.

LOAD

LOAD is normally low and used only when MODE = 0. Once all eight bits have been clocked in, bring LOAD high to update the MAX1101 registers.

DATA

DATA is a bidirectional I/O pin. MODE controls the direction of data transfer. When MODE = 1, DATA is configured as an output from the shift register. Data is clocked out of the shift register by SCLK's rising edge. When MODE = 0, DATA is configured as an input to the shift register, shifted in by the rising edge of SCLK. In this mode, the DATA output driver is disabled, putting DATA into a high-impedance state and allowing it to be driven externally.

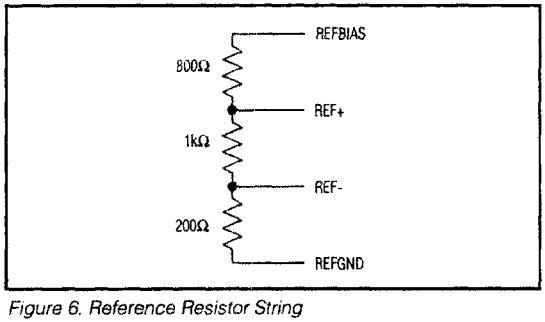

Figure 6. Reference Resistor String

Data Output

Data is clocked in and out of the device with the rising edge of SCLK. The first bit (the MSB, D7) immediately follows the falling edge of VIDSAMP (Figures 7 and 8). The first rising edge of SCLK clocks out the next bit, D6. Data is loaded into the shift register at the falling edge of VIDSAMP. Following the output of D0, DATA output is unspecified for additional SCLK pulses.

Eight-bit-wide storage and output registers hold data from the ADC and delay the data output. The timing diagram in Figure 9 shows the data latency of two VIDSAMP cycles. New data is available after the second falling edge of VIDSAMP.

Data Input

During data input, the first two bits (A0, A1) are the address, selecting either the mux or PGA. The next six bits set the input channel or PGA gain (Table 1).

CLAMP and VIDSAMP

The last two digital inputs are VIDSAMP and CLAMP. VIDSAMP controls the overall cycle timing, with one VIDSAMP cycle corresponding to one CCD pixel. The input is sampled into the ADC by the falling edge of VIDSAMP. CLAMP controls the black sample switch, which sets a reference DC voltage level (V_{REF+}) at the capacitively coupled CCDIN input. The sample switch is on when CLAMP is high.

Control and Interface Logic

The control and interface logic consists of a serial I/O port, which shifts data into and out of the MAX1101, and two registers for storing the mux channel and the PGA gain data.

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Table 1. Control-Byte Format

FUNCTION	A0	A1	D5 MSB	D4	D3	D2	D1	D0 LSB
Address Analog Input Mux	0	0	—	—	—	—	—	—
Address CCD PGA	0	1	—	—	—	—	—	—
No Operation	1	X	X	X	X	X	X	X
Select CCD input	0	0	0	0	0	X	X	X
Select AIN1	0	0	0	1	0	X	X	X
Select AIN2	0	0	1	0	0	X	X	X
Set PGA Gain to -2	0	1	0	0	0	0	0	0
Set PGA Gain to -2.125	0	1	0	0	0	0	0	1
Set PGA Gain to -9.750	0	1	1	1	1	1	1	0
Set PGA Gain to -9.875	0	1	1	1	1	1	1	1

X = Don't Care

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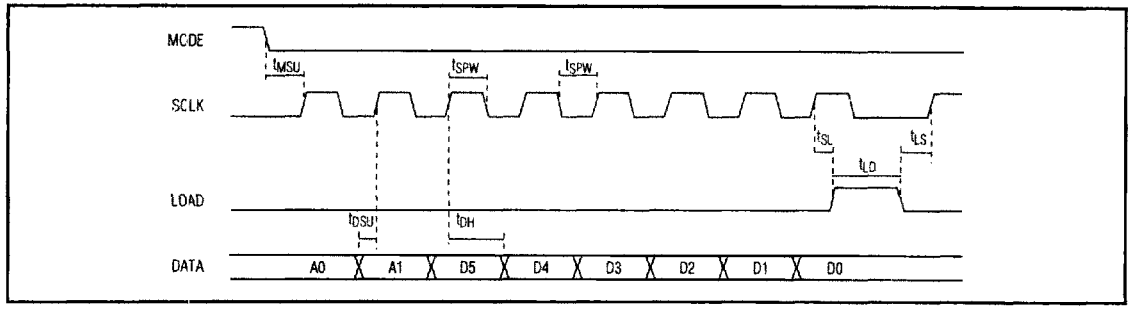

Figure 7. MODE = 0 Timing

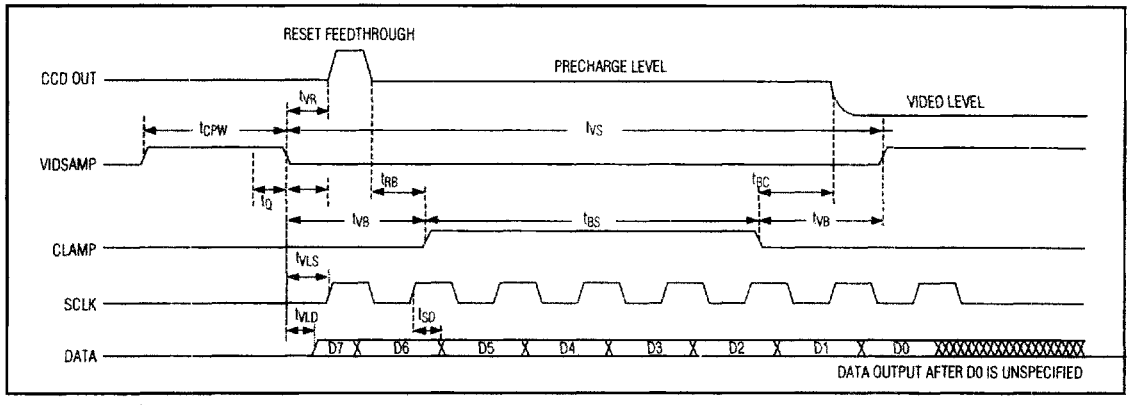

Figure 8. MODE = 1 Timing

LOAD controls the loading of data into the internal storage registers during data input. Once all eight input bits have been clocked into the shift register, a rising edge on LOAD clocks the data into the appropriate storage register (mux or PGA), decoded from the first two input bits.

The logic is divided into four blocks: the two storage registers, the serial I/O port, and a power-on reset generator. The registers are reset by the power-on reset to place them in a predictable state (input channel = CCD, PGA gain = -2) on power-up. The power-on reset typically has a 2.1µs pulse width.

The serial I/O port consists of a shift register, an 8-bit storage register, decode logic to clock input data into the appropriate storage register, and an output driver. The 8-bit storage register takes input data from the ADC.

Input Buffers and Output Drivers

The DATA driver is capable of driving 50pF load capacitance while meeting the output delay specifications given in the *Electrical Characteristics*. The gates of the P-channel and N-channel drivers are driven separately. If MODE is low, both drivers are off and the output is high impedance.

The VIDSAMP, CLAMP, SCLK, and LOAD inputs are buffered and have hysteresis to reject noise with slow-slewing signal edges.

Applications Information

MAX1101 Timing

Figure 7 shows the timing configuration when MODE = 0 and data is loaded into the MAX1101. Figure 8 shows timing when MODE = 1 and the CCD signal is digitized. Figure 9 is an expansion of Figure 8, illustrating the two-VIDSAMP-cycle data latency. Figure 10 shows the relationship of CLAMP to VIDSAMP when MODE = 1.

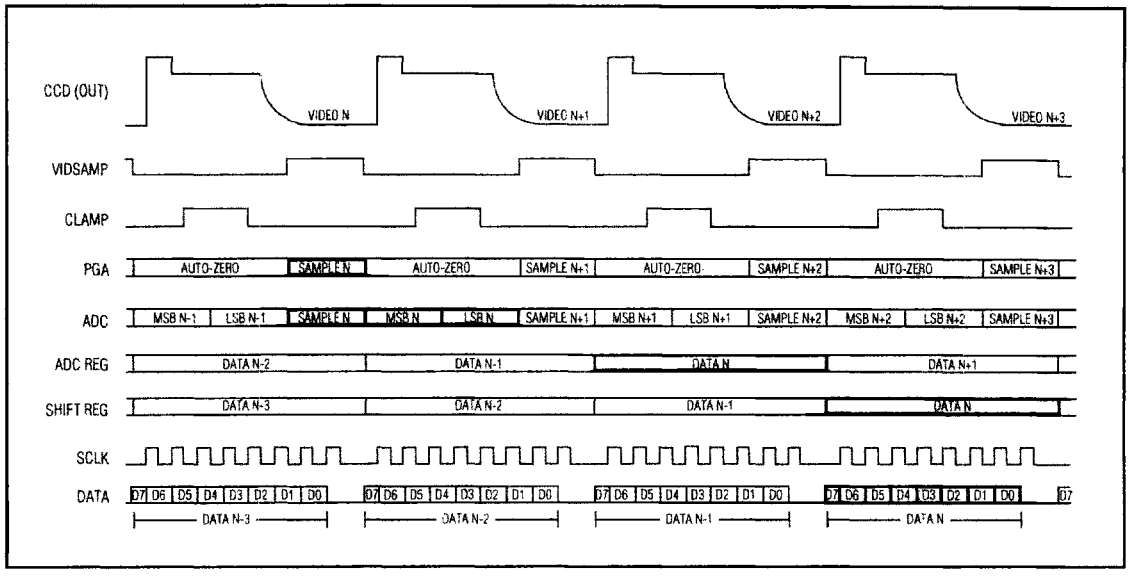

Figure 9. MODE = 1 Timing Showing Data Latency

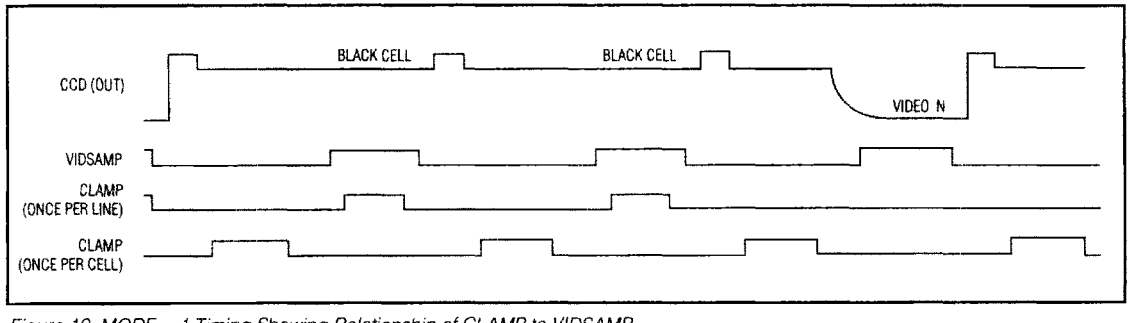

Figure 10. MODE = 1 Timing Showing Relationship of CLAMP to VIDSAMP

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Input/Output Transfer Function

CCD Input

Figure 11 shows the MAX1101 transfer function for CCDIN. Coding is binary, with a -4LSB offset added to ensure that offsets within the MAX1101, which can be positive or negative, do not cause the ADC to be out of range. Full-scale input range at CCDIN is:

$$(V_{REF+} - V_{REF-}) / G_{PGA}$$

where G_{PGA} is the gain of the programmable gain amplifier.

Analog Inputs (AIN_)

The transfer function for auxiliary inputs is shown in Figure 11. Again, coding is binary and full-scale range is V_{REF-} to V_{REF+}. An offset has not been added to these channels; however, code transitions occur at the 1/2LSB point, as shown in Figure 12.

Implementing Correlated Double Sampling (CDS) or Black-Level Compensation

The CLAMP circuit in the MAX1101 can be used to either accomplish CDS or to compensate for the CCD black level. To accomplish CDS, CLAMP is activated once per

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pixel during the CCD output waveform's reset phase. To compensate for the CCD black level, CLAMP is activated during the black-pixel portion of the linear array, as shown in Figure 10. Each of these modes requires a different value of C_{EXT}, as described in the following section.

Choosing C_{EXT} for CDS

In CDS applications, C_{EXT} = 4nF. This value is the best compromise to minimize errors due to the CLAMP switch resistance/C_{EXT} time constant and switch charge injection. The following equation represents the error due to incomplete charging of C_{EXT} during integration time:

$$\varepsilon = \Delta V_{RESET} \times e^{-t/RC}$$

where ΔV_{RESET} = the maximum change in reset level from one pixel to the next, t = CLAMP pulse width, and R = CLAMP switch resistance (150Ωmax). At a sample rate of 670kHz, with t = 750nsec, a 4nF capacitor removes at least 70% of the change in reset voltage level. Typically, R = 60Ω, which corresponds to a 96% cancellation of the change in reset level.

The offset due to switch charge injection is represented by 13pC / 4nF = 3mV. Note that this error will behave like any DC offset; that is, it will be constant from pixel to pixel.

Choosing C_{EXT} in Black-Level Compensation

In activating CLAMP once per line to compensate for the CCD black level, the recommended value of C_{EXT} is governed by the following equations:

$$C_{EXT} \geq 12nF$$

and

$$C_{EXT} \leq N \times t \times 760pF/\mu sec$$

where N is the number of light-shielded cells, and t is the width of the CLAMP pulse in µsec.

The second equation ensures that the time constant formed by R x C_{EXT} is small enough that the black level is captured to within 0.5mV during the dark pixel phase. For example, in an array with 27 dark pixels at a 670kHz sample rate, with t = 750nsec, the second equation becomes $C_{EXT} \leq 15nF$. Capacitors smaller than 12nF can be used; however, offset increases due to switch charge injection, as explained in the section *Choosing C_{EXT} for CDS*.

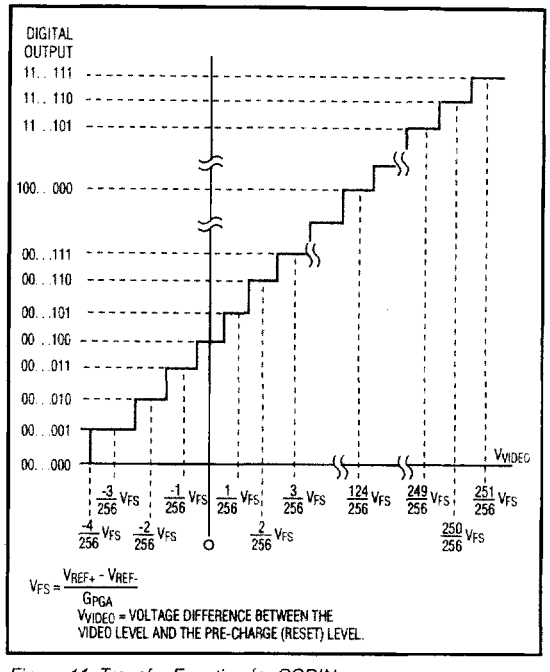


Figure 11. Transfer Function for CCDIN

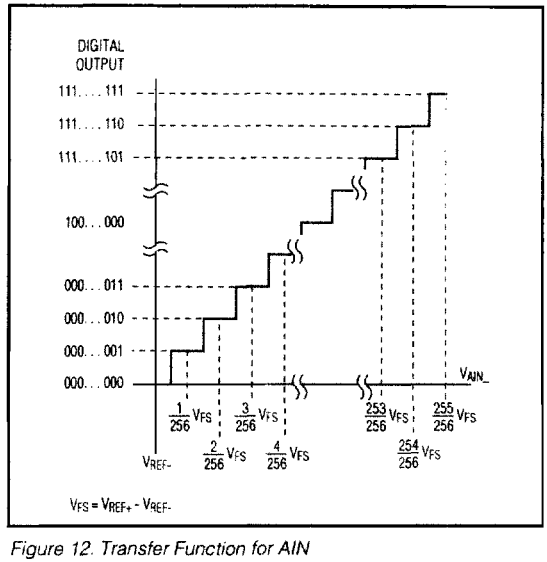


Figure 12. Transfer Function for AIN

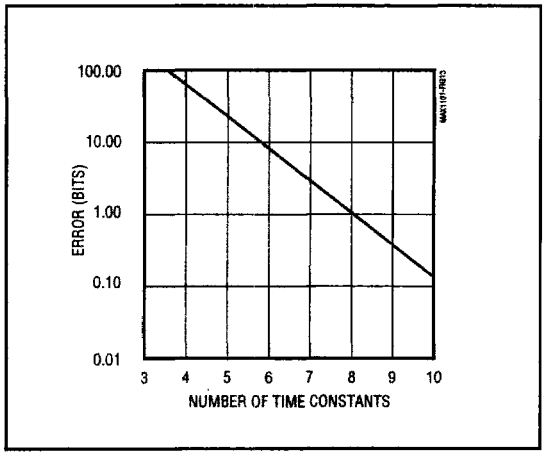


Figure 13. Black Level Error vs. C_{EXT} Time Constant at Maximum PGA Gain (1mV/bit)

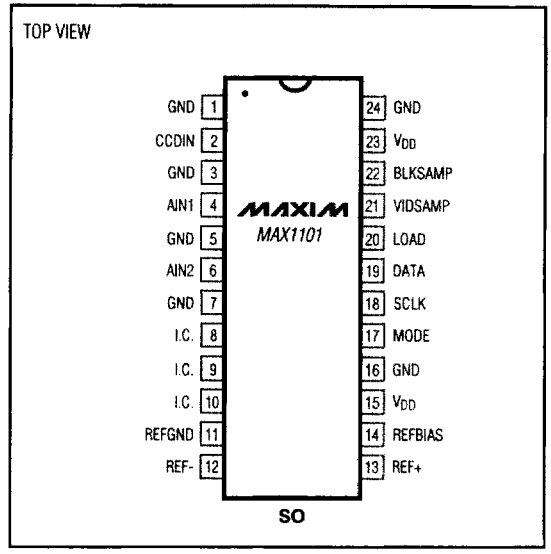
Bypassing and Layout Considerations

Solder the MAX1101 to a multilayer board (two or more layers) where the layer immediately beneath the device is a ground plane.

Connect the V_{DD} pins together at the MAX1101. Connect all ground pins together at the device.

Bypass V_{DD} to ground with at least a 0.1µF ceramic capacitor. If larger capacitors are used, tantalum is satisfactory.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 3430