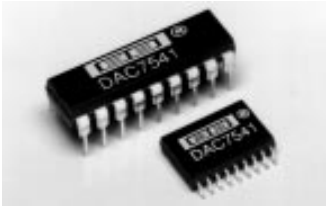
BURR - BROWN®



DAC7541A

Low Cost 12-Bit CMOS Four-Quadrant Multiplying DIGITAL-TO-ANALOG CONVERTER

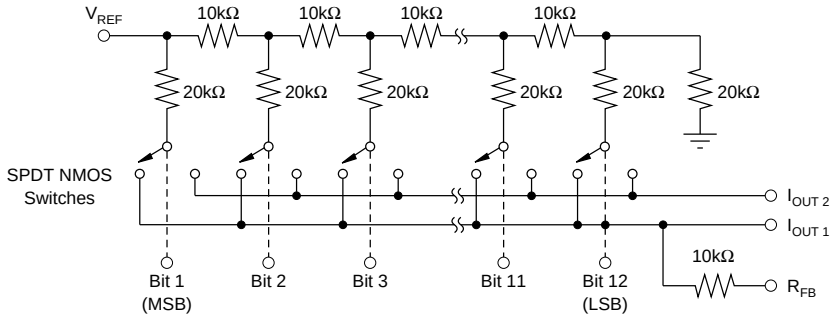
FEATURES

- FULL FOUR-QUADRANT MULTIPLICATION
- 12-BIT END-POINT LINEARITY
- DIFFERENTIAL LINEARITY ±1/2LSB MAX OVER TEMPERATURE
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- TTL-/CMOS-COMPATIBLE
- SINGLE +5V TO +15V SUPPLY
- LATCH-UP RESISTANT
- 7521/7541/7541A REPLACEMENT
- PACKAGES: Plastic DIP, Plastic SOIC
- LOW COST

DESCRIPTION

The Burr-Brown DAC7541A is a low cost 12-bit, four-quadrant multiplying digital-to-analog converter. Laser-trimmed thin-film resistors on a monolithic CMOS circuit provide true 12-bit integral and differential linearity over the full specified temperature range.

DAC7541A is a direct, improved pin-for-pin replacement for 7521, 7541, and 7541A industry standard parts. In addition to a standard 18-pin plastic package, the DAC7541A is also available in a surface-mount plastic 18-pin SOIC.



Digital Inputs (DTL-/TTL-/CMOS-compatible)
Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

Switches shown for digital inputs "HIGH".

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SPECIFICATIONS

ELECTRICAL

At +25°C, $+V_{DD}$ = +12V or +15V, V_{REF} = +10V, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V, unless otherwise specified.

PARAMETER	DAC7541A GRADE	T_A = +25°C	$T_A = T_{MAX}, T_{MIN}$[1]	UNITS	TEST CONDITIONS/COMMENTS
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J	±1	±1	LSB max	±1LSB = ±0.024% of FSR.
	K	±1/2	±1/2	LSB max	±1/2LSB = ±0.012% of FSR.
Differential Non-linearity	J	±1	±1	LSB max	All grades guaranteed monotonic to 12 bits,
	K	±1/2	±1/2	LSB max	T_{MIN} to T_{MAX}.
Gain Error	J	±6	±8	LSB max	Measured using internal R_{FB} and includes effect
	K	±1	±3	LSB max	of leakage current and gain T.C.
					Gain error can be trimmed to zero.
Gain Temperature Coefficient					
(ΔGain/ΔTemperature)	ALL		5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current: Out_1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
Out_2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
REFERENCE INPUT					
Voltage (Pin 17 to GND)	All	–10/+10	–10/+10	V min/max	
Input Resistance (Pin 17 to GND)	All	7-18	7-18	kΩ min/max	
					Typical input resistance = 11kΩ.
					Typical input resistance temperature coefficient is –50ppm/°C.
DIGITAL INPUTS					
V_{IN} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	µA max	Logic inputs are MOS gates.
					I_{IN} typ (25°C) = 1nA
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
$\Delta Gain/\Delta V_{DD}$	All	±0.01	±0.02	% per % max	V_{DD} = +11.4V to +16V
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min to V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IN}.
	All	100	500	µA max	All digital inputs 0V or V_{DD}.

NOTES: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions. (2) Guaranteed by design but not production tested.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not production tested.
V_{DD} = +15V, V_{REF} = +10V except where stated, $V_{PIN\ 1} = V_{PIN\ 2}$ = 0V, output amp is OPA606 except where stated.

PARAMETER	DAC7541A GRADE	T_A = +25°C	$T_A = T_{MAX}, T_{MIN}$[1]	UNITS	TEST CONDITIONS/COMMENTS
PROPAGATION DELAY					
(from Digital Input change to 90% of					Out_1 Load = 100Ω, C_{EXT} = 13pF.
final Analog Output)	All	100	—	ns typ	Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	1000	—	nV-s typ	V_{REF} = 0V, all digital inputs 0V to V_{DD} or V_{DD} to 0V. Measured using OPA606 as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR					
(V_{REF} to Out_1)	All	1.0	—	mVp-p max	V_{REF} = ±10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME					
	All	0.6	—	µs typ	To 0.01% of Full Scale Range.
					Out_1 Load = 100Ω, C_{EXT} = 13pF.
	All	1.0	—	µs max	Digital Inputs: 0V to V_{DD} or V_{DD} to 0V.
OUTPUT CAPACITANCE					
$C_{OUT\ 1}$ (Pin 1)	All	100	100	pF max	Digital Inputs = V_{IH}
$C_{OUT\ 2}$ (Pin 2)	All	60	60	pF max	Digital Inputs = V_{IH}
$C_{OUT\ 1}$ (Pin 1)	All	70	70	pF max	Digital Inputs = V_{IL}
$C_{OUT\ 2}$ (Pin 2)	All	100	100	pF max	Digital Inputs = V_{IL}

NOTE: (1) Temperature ranges are: = 0°C to + 70°C for JP, KP, JU and KU versions.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} (Pin 16) to Ground	+17V
V_{REF} (Pin 17) to Ground	+25V
V_{RPB} (Pin 18) to Ground	±25V
Digital Input Voltage (pins 4-15) to Ground	–0.4V, V_{DD}
$V_{PIN\ 1}$, $V_{PIN\ 2}$ to Ground	–0.4V, V_{DD}
Power Dissipation (any Package):	
To +75°C	450mW
Derates above +75°C	–6mW/°C
Lead Temperature (soldering, 10s)	+300°C
Storage Temperature: Plastic Package	+125°C

NOTE: (1) Stresses above those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

The DAC7541A is an ESD (electrostatic discharge) sensitive device. The digital control inputs have a special FET structure, which turns on when the input exceeds the supply by 18V, to minimize ESD damage. However, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. When not in use, devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

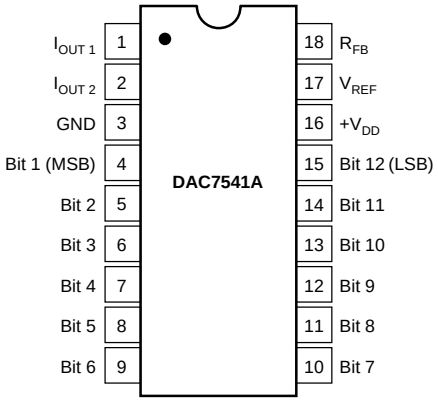
BURN-IN SCREENING

Burn-in screening is an option available for the models in the Ordering Information table. Burn-in duration is 160 hours at the indicated temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

PIN CONNECTIONS

Top View **DIP/SOIC**



PACKAGE INFORMATION

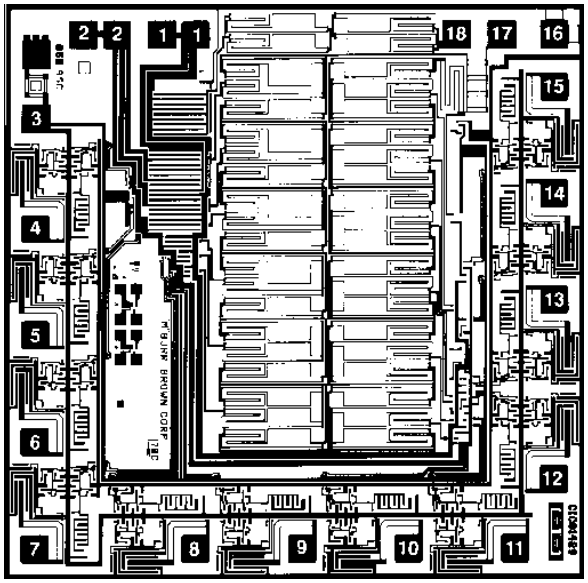
MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC7541JP	Plastic DIP	218
DAC7541KP	Plastic DIP	218
DAC7541JU	Plastic SOIC	219
DAC7541KU	Plastic SOIC	219
DAC7541JP-BI	Plastic DIP	218
DAC7541KP-BI	Plastic DIP	218

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	RELATIVE ACCURACY (LSB)	GAIN ERROR (LSB)
DAC7541AJP	Plastic DIP	0°C to +70°C	±1	±6
DAC7541AKP	Plastic DIP	0°C to +70°C	±1/2	±1
DAC7541AJU	Plastic SOIC	0°C to +70°C	±1	±6
DAC7541AKU	Plastic SOIC	0°C to +70°C	±1/2	±1
BURN-IN SCREENING OPTION See text for details.				
MODEL	**PACKAGE**	**TEMPERATURE RANGE**	**RELATIVE ACCURACY (LSB)**	**BURN-IN TEMP. (160 Hours)[1]**
DAC7541AJP-BI	Plastic DIP	0°C to +70°C	±1	+85°C
DAC7541AKP-BI	Plastic DIP	0°C to +70°C	±1/2	+85°C

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.



DIE TOPOLOGY DAC7541A

PAD	FUNCTION	PAD	FUNCTION
1	I_{OUT1}	10	Bit 7
2	I_{OUT2}	11	Bit 8
3	GND	12	Bit 9
4	Bit 1 (MSB)	13	Bit 10
5	Bit 2	14	Bit 11
6	Bit 3	15	Bit 12 (LSB)
7	Bit 4	16	$+V_{DD}$
8	Bit 5	17	V_{REF}
9	Bit 6	18	$R_{FEEDBACK}$

Substrate Bias: Isolated.
NC: No Connection.

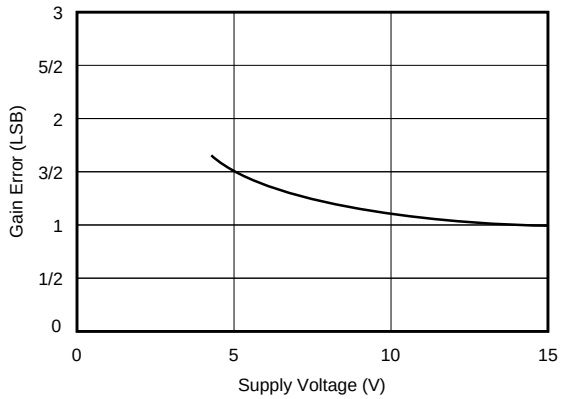
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	104 x 105 ±5	2.64 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

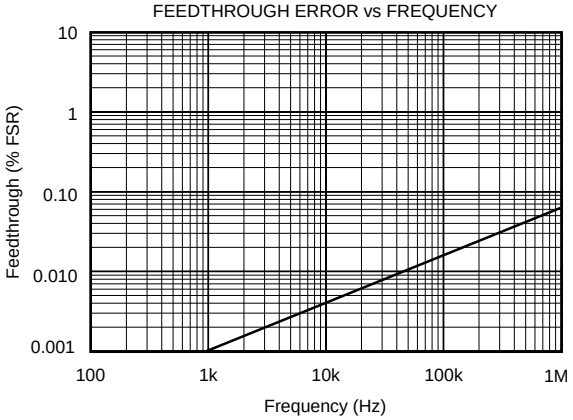
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V, unless otherwise noted.

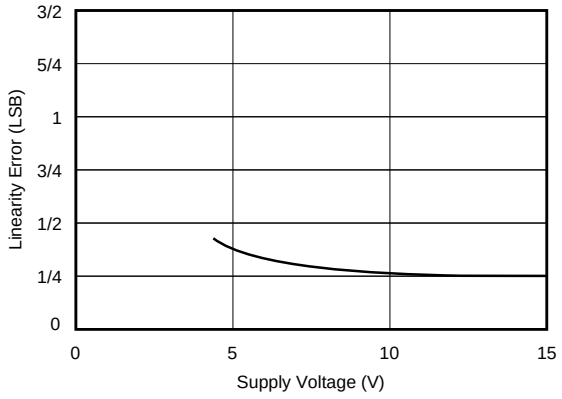
GAIN ERROR vs SUPPLY VOLTAGE



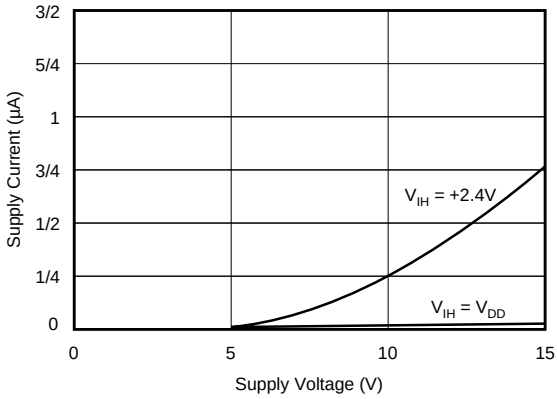
FEEDTHROUGH ERROR vs FREQUENCY



LINEARITY vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DISCUSSION OF SPECIFICATIONS

RELATIVE ACCURACY

This term (also known as linearity) describes the transfer function of analog output to digital input code. The linearity error describes the deviation from a straight line between zero and full scale.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1LSB change in the output, from one adjacent output state to the next. A differential nonlinearity specification of ±1.0LSB guarantees monotonicity.

GAIN ERROR

Gain error is the difference in measure of full-scale output versus the ideal DAC output. The ideal output for the DAC7541A is –(4095/4096) X (V_{REF}). Gain error may be adjusted to zero using external trims.

OUTPUT LEAKAGE CURRENT

The measure of current which appears at Out_1 with the DAC loaded with all zeros, or at Out_2 with the DAC loaded with all ones.

MULTIPLYING FEEDTHROUGH ERROR

This is the AC error output due to capacitive feedthrough from V_{REF} to Out_1 with the DAC loaded with all zeros. This test is performed at 10kHz.

OUTPUT CURRENT SETTLING TIME

This is the time required for the output to settle to a tolerance of ±0.5LSB of final value from a change in code of all zeros to all ones, or all ones to all zeros.

PROPAGATION DELAY

This is the measure of the delay of the internal circuitry and is measured as the time from a digital code change to the point at which the output reaches 90% of final value.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is the measure of the area of the glitch energy measured in nV-seconds. Key contributions to glitch energy are digital word-bit timing differences, internal circuitry timing differences, and charge injected from digital logic.

MONOTONICITY

Monotonicity assures that the analog output will increase or stay the same for increasing digital input codes. The DAC7541A is guaranteed monotonic to 12 bits.

POWER SUPPLY REJECTION

Power supply rejection is the measure of the sensitivity of the output (full scale) to a change in the power supply voltage.

CIRCUIT DESCRIPTION

The DAC7541A is a 12-bit multiplying D/A converter consisting of a highly stable thin-film R-2R ladder network and 12 pairs of current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the DAC7541A is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\ 1}$ and $I_{OUT\ 2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity.

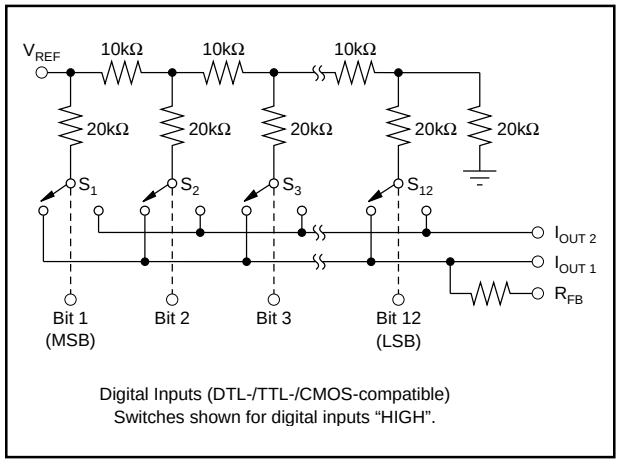


FIGURE 1. Simplified DAC Circuit.

EQUIVALENT CIRCUIT ANALYSIS

Figures 2 and 3 show the equivalent circuits for all digital inputs low and high, respectively. The reference current is switched to $I_{OUT\ 2}$ when all inputs are low and $I_{OUT\ 1}$ when inputs are high. The I_L current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant one-bit current drain through the ladder terminal.

DYNAMIC PERFORMANCE

Output Impedance

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\ 1}$ terminal may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output

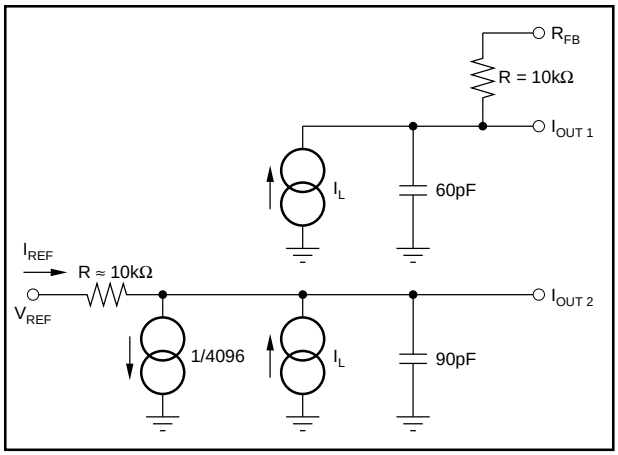


FIGURE 2. DAC7541A Equivalent Circuit (All inputs LOW).

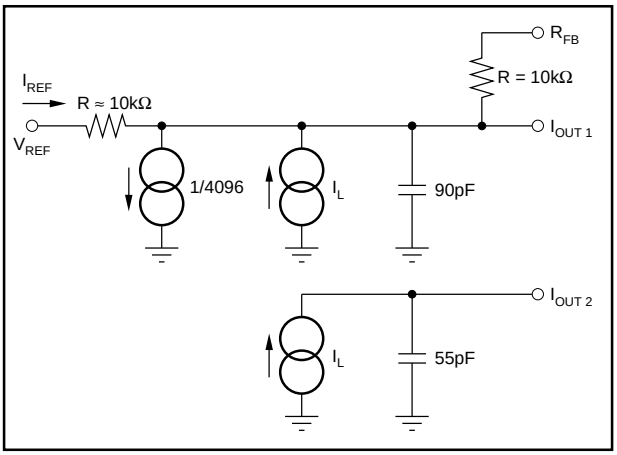


FIGURE 3. DAC7541A Equivalent Circuit (All inputs HIGH).

amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the DAC7541A. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically dampen the output. See Figures 4 and 6.

APPLICATIONS

OP AMP CONSIDERATIONS

The input bias current of the op amp flows through the feedback resistor, creating an error voltage at the output of the op amp. This will show up as an offset through all codes of the transfer characteristics. A low bias current op amp such as the OPA606 is recommended.

Low offset voltage and V_{OS} drift are also important. The output impedance of the DAC is modulated with the digital code. This impedance change (approximately 10kΩ to 30kΩ) is a change in closed-loop gain to the op amp. The result is that V_{OS} will be multiplied by a factor of one to two depending on the code. This shows up as a linearity error. Offset can be adjusted out using Figure 4. Gain may be adjusted using Figure 5.

UNIPOLAR BINARY OPERATION (Two-Quadrant Multiplication)

Figure 4 shows the analog circuit connections required for unipolar binary (two-quadrant multiplication) operation. With a DC reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an AC reference voltage or current, the circuit provides two-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I.

BINARY INPUT	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$-V_{REF}$ (4095/4096)
1000 0000 0000	$-V_{REF}$ (2048/4096)
0000 0000 0001	$-V_{REF}$ (1/4096)
0000 0000 0000	0V

TABLE I. Unipolar Codes.

C_1 phase compensation (10 to 25pF) in Figure 4 may be required for stability when using high speed amplifiers. C_1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at Out_1.

R_1 in Figure 5 provides full scale trim capability—load the DAC register to 1111 1111 1111, adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096). Alternatively, full scale can be adjusted by omitting R_1 and R_2 and trimming the reference voltage magnitude.

BIPOLAR FOUR-QUADRANT OPERATION

Figure 6 shows the connections for bipolar four-quadrant operation. Offset can be adjusted with the A_1 to A_2 summing resistor, with the input code set to 1000 0000 0000. Gain may be adjusted by varying the feedback resistor of A_2. The input/output relationship is shown in Table II.

BINARY INPUT	ANALOG OUTPUT
MSB LSB	
1111 1111 1111	$+V_{REF}$ (2047/2048)
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}$ (1/2048)
0000 0000 0000	$-V_{REF}$ (2048/2048)

TABLE II. Bipolar Codes.

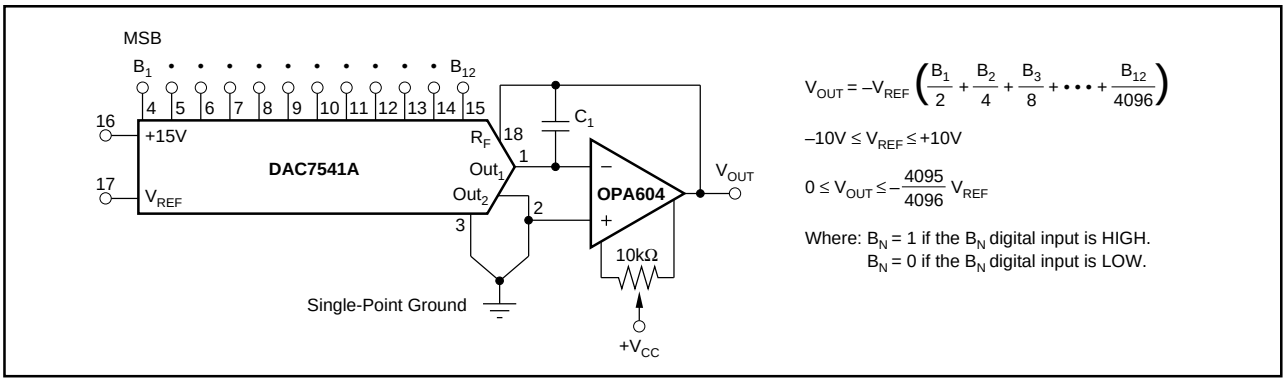


FIGURE 4. Basic Connection With Op Amp V_{OS} Adjust: Unipolar (two-quadrant) Multiplying Configuration.

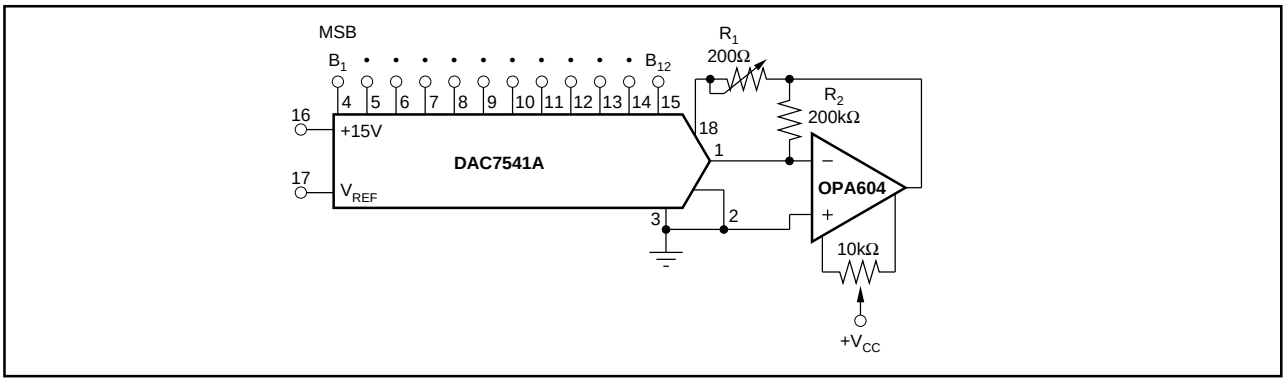


FIGURE 5. Basic Connection With Gain Adjust (allows adjustment up or down).

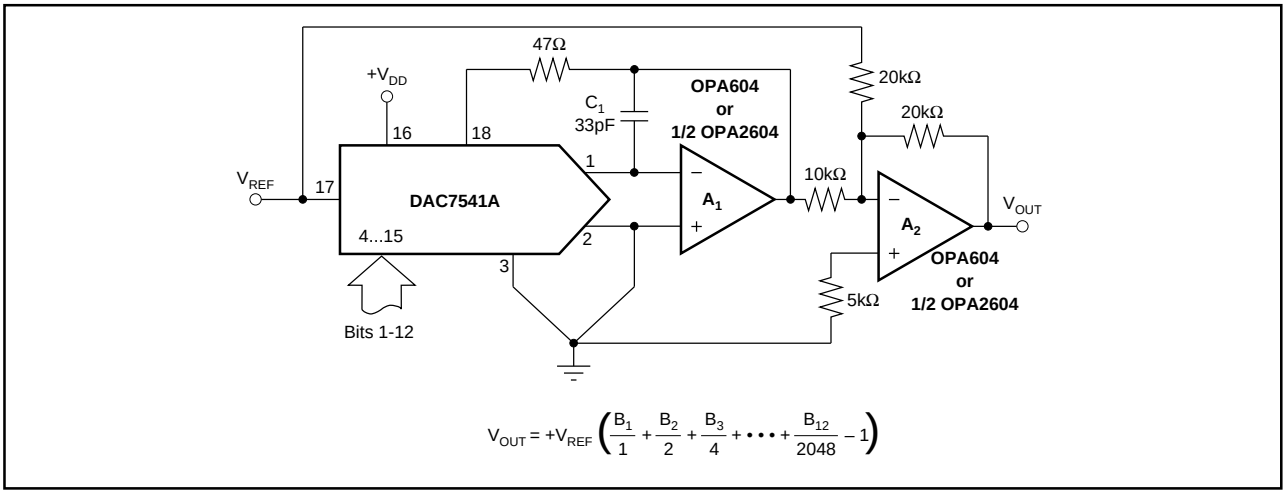


FIGURE 6. Bipolar Four-Quadrant Multiplier.

DIGITALLY CONTROLLED GAIN BLOCK

The DAC7541A may be used in a digitally controlled gain block as shown in Figure 7. This circuit gives a range of gain from one (all bits = one) to 4096 (LSB = one). The transfer function is:

$$V_{OUT} = \frac{-V_{IN}}{\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \bullet\bullet\bullet + \frac{B_{12}}{4096}\right)}$$

All bits off is an illegal state, as division by zero is impossible (no op amp feedback). Also, errors increase as gain increases, and errors are minimized at major carries (only one bit on at a time).

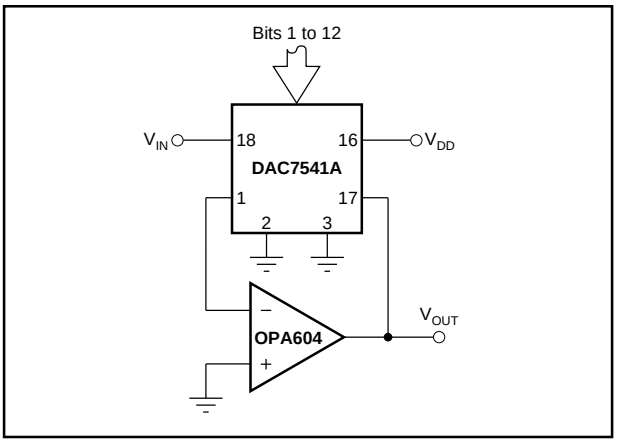


FIGURE 7. Digitally Programmable Gain Block.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7541AJU	OBSOLETE	SOP	DTC	18		TBD	Call TI	Call TI	0 to 70	DAC7541AJU	
DAC7541AJUG4	OBSOLETE	SOP	DTC	18		TBD	Call TI	Call TI	0 to 70	DAC7541AJU	
DAC7541AKU	OBSOLETE	SOP	DTC	18		TBD	Call TI	Call TI	0 to 70	DAC7541AKU	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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