GENERAL INSTRUMENT	27C128	PRELIMINARY INFORMATION

128K (16K x 8) CMOS UV Erasable PROM

FEATURES

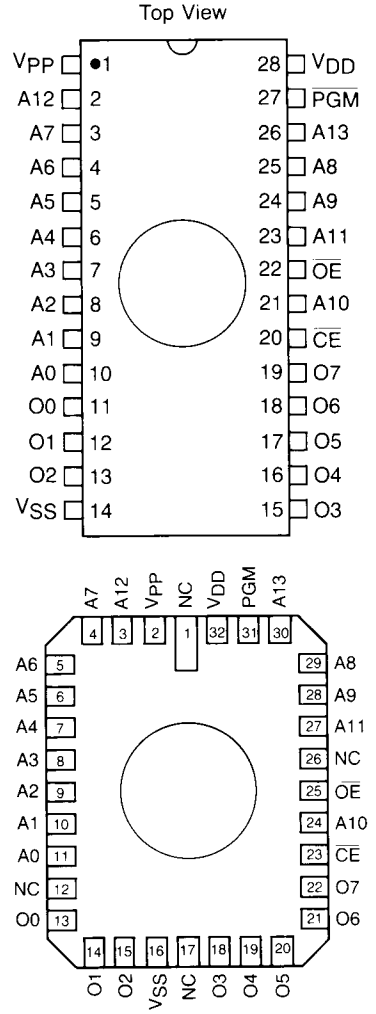
- High Speed Performance — 125ns maximum access time
- CMOS Design — Ultra Low Power Dissipation
  - — 20mA Active Current
  - — 100μA Standby Current
- Fully Static Operation, no clocks required
- All Inputs and Outputs TTL Compatible
- Auto ID™ Identification; Aids Automated Programming
- Separate Chip Enable and Output Enable Control Inputs
- Fast Programming Algorithm
- Organized 16K x 8 — JEDEC Standard Pinouts
  - — 28 Pin Dual In Line Package
  - — 32 Pin Leadless Chip Carrier
- Available for Extended Temperature Ranges:
  - — Commercial (C) = 0° to 70°C
  - — Industrial (I) = −40° to 85°C
  - — Military* (M) = −55° to +125°C

DESCRIPTION

The General Instrument 27C128 is a CMOS 128K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 16K words by 8 bits (16K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 125ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. The CMOS design and processing enables this part to be used in systems where reduced power consumption and enhanced reliability are requirements.

PIN CONFIGURATION

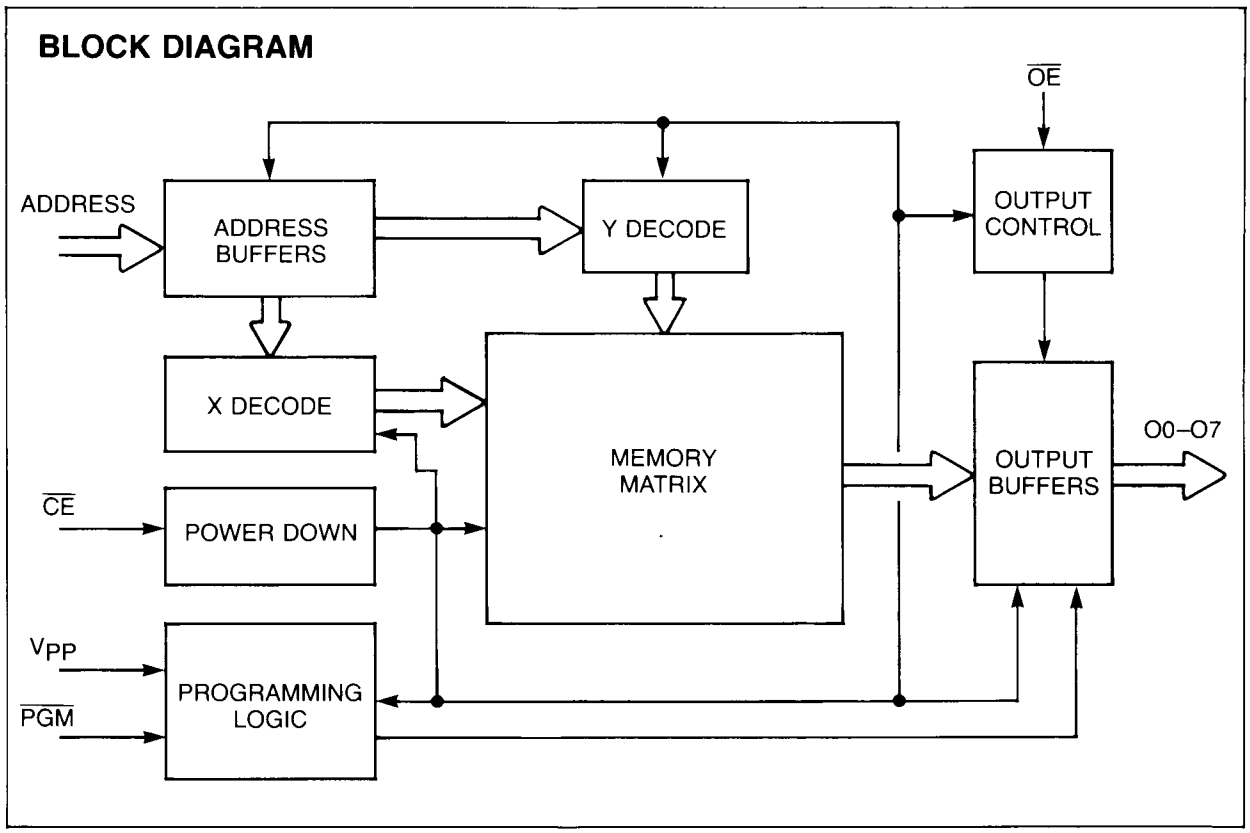
Top View



34 Pcs Only
005970
5970 GI

*Military Version (MR) screened to MIL STD 883 Rev. C, Method 5004 Test Specification.

BLOCK DIAGRAM



MODES

MODES	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	A9	O0–O7
Read	V_{IL}	V_{IL}	V_{IH}	V_{DD}	X	D_{out}
Program	V_{IL}	V_{IH}	V_{IL}	12V	X	D_{in}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12V	X	D_{out}
Program Inhibit	V_{IH}	X	X	12V	X	High Z
Standby	V_{IH}	X	X	V_{DD}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{DD}	X	High Z
Identity	V_{IL}	V_{IL}	V_{IH}	V_{DD}	+12V	Code

READ MODE (See Timing Diagrams and AC Characteristics)

Read mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip.
b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$.

STANDBY MODE

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not defined.

When these conditions are met, the supply current will drop from 20mA to 100μA.

OUTPUT ENABLE

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

The $\overline{OE}$ pin is high and a program mode is not defined.

ERASE MODE

The memory matrix is erased to the all "1" 's state as a result of being exposed to ultraviolet light. To ensure complete erasure a dose of 15 watt-second / cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms and intensity of 12,000μW/cm^2 for 20 minutes.

PROGRAMMING MODE

Programming takes place when both:

a) V_{PP} is 12.5 ± .5V and
b) The $\overline{CE}$ pin is low.
c) The $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via A0–A13 and the data to be programmed is presented to O0–O7. When data and address are stable, $\overline{CE}$ is low, a low going pulse on the $\overline{PGM}$ line programs that location. The fast programming technique will be accepted by the chip.

A 1-msec programming pulse will be given and the byte then verified. If the byte failed to verify, apply another 1-msec programming pulse and check the byte again. Continue applying 1-msec pulses until either the byte verifies or 25 pulses have been applied. If 25 pulses are applied and byte still does not verify, fail the device. After the byte verifies, a single pulse of a width three times the number of 1-msec pulses previously given will be applied; i.e., the minimum overprogramming pulse for each byte will be 3 x 1 msec, the maximum being (3 x 25) 75 msec.

VERIFY

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{PP} is 12.5 ± 5V
b) the $\overline{OE}$ line is low
c) the $\overline{PGM}$ line is high
d) the $\overline{CE}$ line is low.

INHIBIT

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, all other devices with $\overline{CE}$ held high will not be programmed with the data although address and data will be available on their input pins, i.e. when a high level is present on $\overline{CE}$ or $\overline{PGM}$, the device is inhibited from programming.

MANUFACTURERS IDENTITY

In this mode specific data is outputted identifying the manufacturer as General Instrument, device type, where manufactured, etc. This mode is entered when pin (A9) is taken up to between 11.5–12.5V. The row x decoders become disabled internally and the ROM data can be outputted. The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7. The General Instrument identify code is as follows:

The General Instrument identity code is as follows:

Pin / Identity	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex Code
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type	V_{IH}	1	0	0	0	0	0	1	1	83

*Code subject to change.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and input voltages w.r.t. V_{SS} . . . . −0.6 to +6.25V
V_{PP} voltage w.r.t. V_{SS} during programming . . . . . −0.6 to +14V
Voltage on A9 w.r.t. V_{SS} . . . . . −0.6 to +13.5V
Storage temperature . . . . . −65°C to +150°C
Ambient temperature with power applied. . −65°C to +125°C

Set Up Conditions for DC Characteristics (Read Operation)

V_{DD} = +5V ± 10%[1]
T_{AMB}: Commercial (C) = 0°C to 70°C
Industrial (I) = −40°C to +85°C
Military (M) = −55°C to +125°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (READ OPERATION)

PARAMETER	SYM	MIN	MAX	UNITS	CONDITIONS
Inputs					
Address lines A0–A13					
Data lines (program mode) O0–O7					
$\overline{CE}$ & $\overline{OE}$					
Logic "1"	V_{IH}	2.0	$V_{DD}+1$	V	
Logic "0"	V_{IL}	−0.1	0.8	V	
Leakage	I_{IL}	−10	10	µA	V_{IN} = 0 to V_{DD}
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V, T_{AMB} = 25°C, f = 1MHz
Outputs					
In read/verify mode O0–O7					
Logic "1"	V_{OH}	2.4		V	I_{OH} = −400µA
Logic "0"	V_{OL}		0.45	V	I_{OL} = 2.1mA
Leakage	I_{OL}	−10	10	µA	V_{OUT} = 0 to V_{DD}
Output Capacitance	C_{OUT}		12	pF	V_{OUT} = 0V, T_{AMB} = 25°C, f = 1MHz
Power Supply Current					
I_{DD} Active (TTL Inputs)	I_{DD}		20	mA	V_{DD} = 5.5V, V_{PP} = V_{DD}, $\overline{OE}$ = $\overline{CE}$ = V_{IL}, T_{AMB} = 0°C to 70°C, V_{IL} = −0.1V to 0.8V, V_{IH} = 2.0V to V_{DD}
I_{DD} Active (TTL Inputs) (Extended Temp. Range)	I_{DD}		25	mA	V_{DD} = 5.5V, V_{PP} = V_{DD}, $\overline{OE}$ = $\overline{CE}$ = V_{IL}, T_{AMB} = −55°C to 125°C, V_{IL} = −0.1V to 0.8V, V_{IH} = 2.0V to V_{DD}
I_{DD} Standby (TTL Inputs)	$I_{DD(S)TTL}$		2	mA	$\overline{CE}$ = V_{IH}
I_{DD} Standby (TTL Inputs) (Extended Temperature Range)	$I_{DD(S)TTL}$		3	mA	$\overline{CE}$ = V_{IH}, T_{AMB} = −55°C to 125°C
I_{DD} Standby (CMOS Inputs)	$I_{DD(S)CMOS}$		100	µA	$\overline{CE}$ = V_{DD} ± 0.2V
I_{PP} (Read Mode)			100	µA	V_{PP} = 5.5V
V_{PP} READ VOLTAGE	V_{PP}	$V_{DD}-0.7$	V_{DD}	V	(NOTE 1)

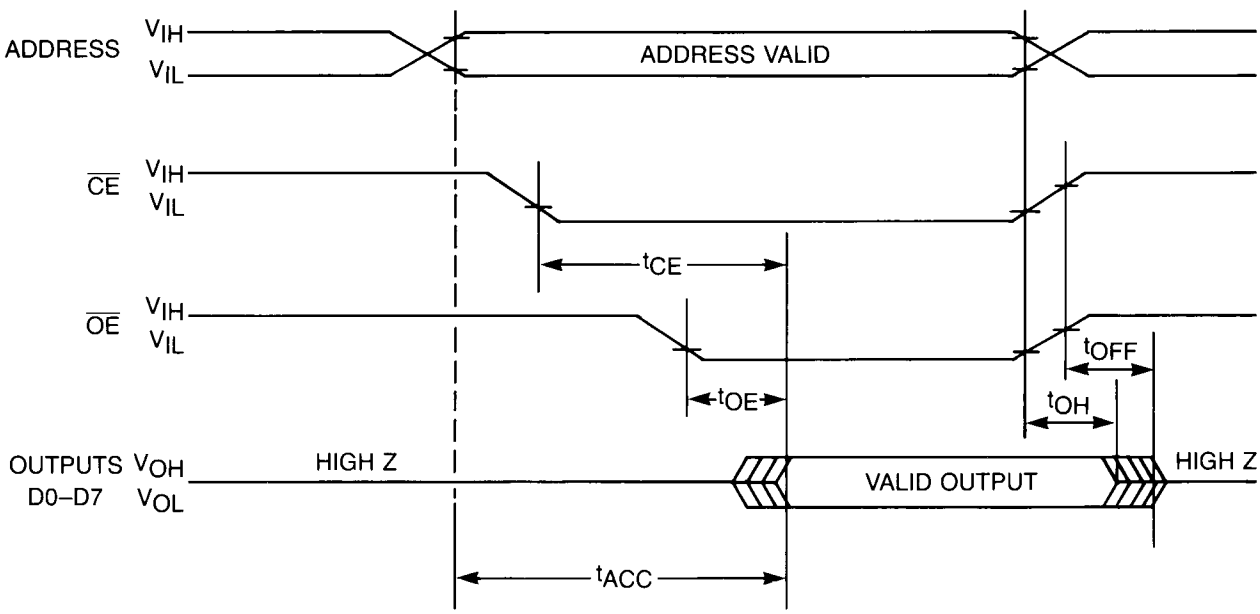
NOTES: 1. V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS (READ OPERATION)

AC TESTING WAVEFORM
V_{IH} = 2.4V AND V_{IL} = 0.45V
V_{OH} = 2.0V AND V_{OL} = 0.8V
Output Load = 1 TTL Load + 100pF
Note: 27C128-12 is only available in commercial temperature range.

T_A: Commercial (C) = 0°C to 70°C
Industrial (I) = −40°C to +85°C
Military (M) = −55°C to +125°C

SYM	PARAMETER	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{ACC}	Address to Output Delay		125		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		125		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
t_{OE}	$\overline{OE}$ to Output Delay		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
t_{OFF}	$\overline{OE}$ to O/P High Impedance	0	50	0	50		50	0	55	0	60	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold From Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	0		0		0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}



DC PROGRAMMING CHARACTERISTICS

T_A = 25 ± 5°C, V_{DD} = 6.0 ± 0.25V, V_{PP} = 12.5 ± 0.5V

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS (SEE NOTE 1)
I_{LI}	Input Current (All Inputs)	−10	10	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{DD}+1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage During Verify	2.4		V	I_{OH} = −400µA
I_{DD2}	V_{DD} Supply Current (Program & Verify)		20	mA	
I_{PP2}	V_{PP} Supply Current (Program)		25	mA	$\overline{CE} = V_{IL}$
V_{ID}	A9 Product Identification Voltage	11.5	12.5	V	

NOTES: 1. V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS

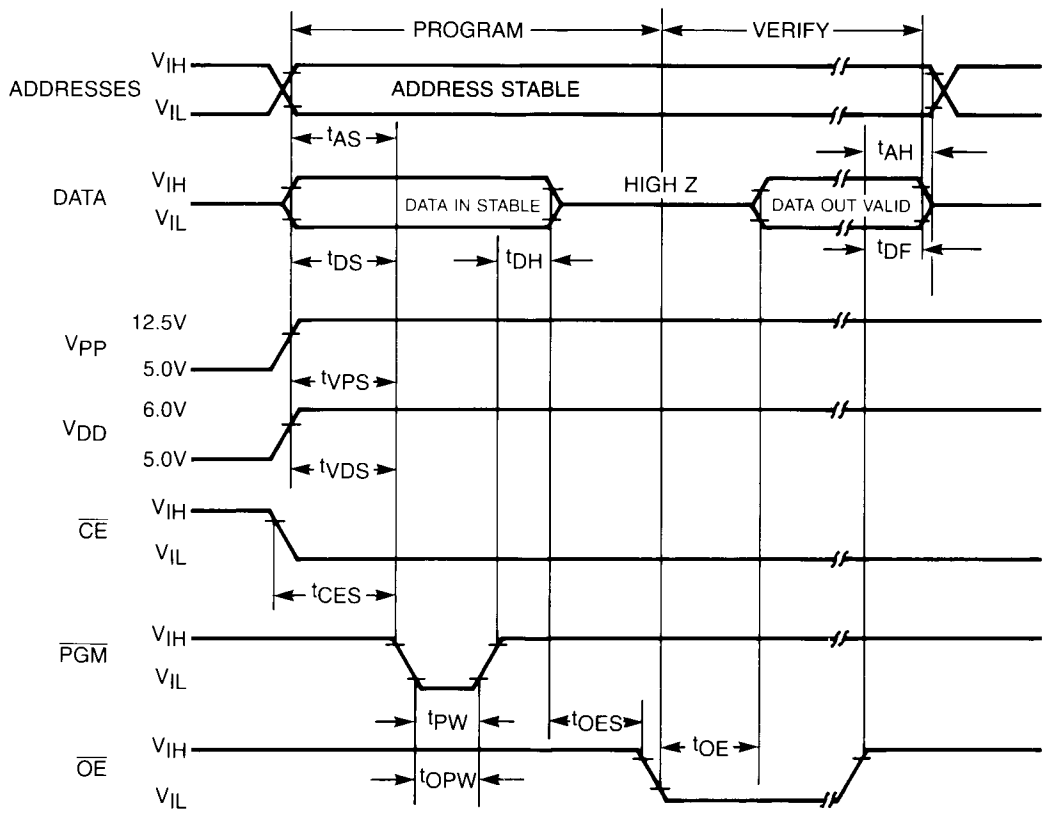
Conditions: 25°C ± 5°C, V_{DD} = 6.0 ± 0.25V, V_{PP} = 12.5 ± 0.5V

Program, Program Verify, and Program Inhibit Modes

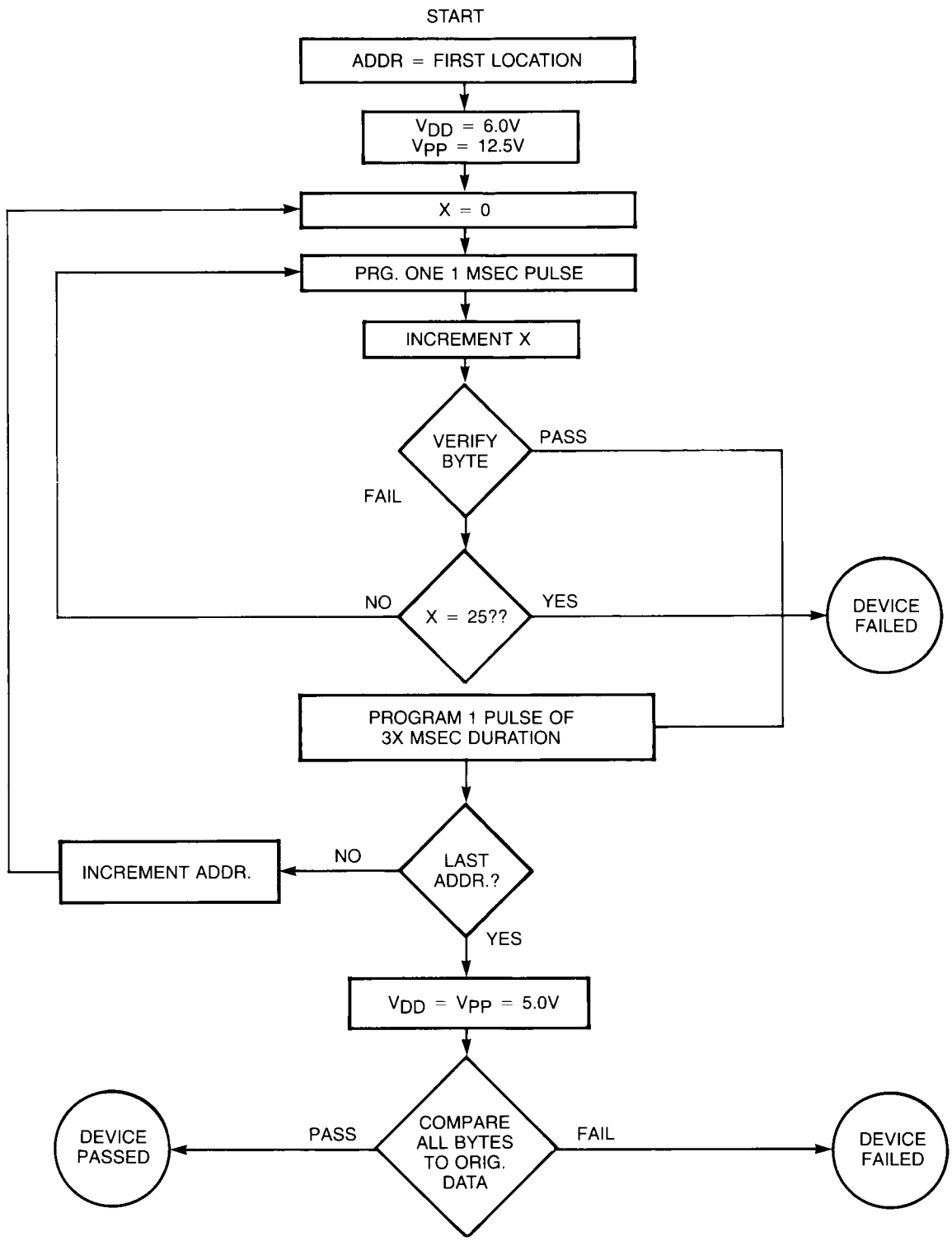
PARAMETER	SYM	MIN	TYP	MAX	UNITS
Address Setup-Up Time	t_{AS}	2			µs
Data Set-Up Time	t_{DS}	2			µs
Data Hold Time	t_{DH}	2			µs
Address Hold Time	t_{AH}	0			µs
Float Delay	t_{DF}	0		130	ns
V_{DD} Set-Up Time	t_{VDS}	2			µs
Program Pulse Width[1]	t_{PW}	0.95	1	1.05	ms
$\overline{CE}$ Set-Up Time	t_{CES}	2			µs
$\overline{OE}$ Set-Up Time	t_{OES}	2			µs
V_{PP} Set-Up Time	t_{VPS}	2			µs
Overprogram Pulse Width[2]	t_{OPW}	2.85		78.75	ms
Data valid from $\overline{OE}$	t_{OE}			100	ns

NOTES: 1. Initial program pulse width tolerance is 1 msec ± 5%.
2. The length of the overprogram pulse may vary from 2.85 to 78.75 msec as a function of the iteration counter value.

PROGRAM MODE



FAST PROGRAMMING ALGORITHM



ORDER INFORMATION

27C128 - 25 M R / K

PACKAGE
- — CERDIP
- D SIDEBRAZED CERAMIC
- KA CERAMIC LEADLESS CHIP CARRIER
- KB CERAMIC LEADLESS CHIP CARRIER, THERMALLY ENHANCED

SCREENING
- — STANDARD COMMERCIAL SCREENING
- R SCREENING PER MIL STD 883C METHOD 5004

TEMPERATURE RANGE
- — 0°C TO 70°C
- I −40°C TO 85°C
- M −55°C TO 125°C

SPEED
- −12 125NS ACCESS
- −15 150NS ACCESS
- −17 170NS ACCESS
- −20 200NS ACCESS
- −25 250NS ACCESS

DEVICE
128K (16K X 8) CMOS EPROM

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