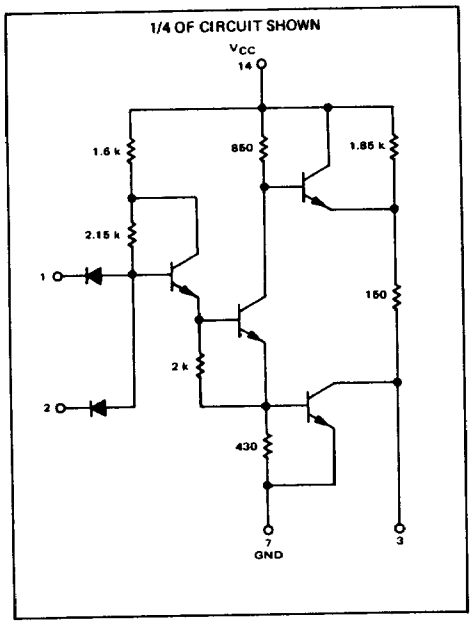
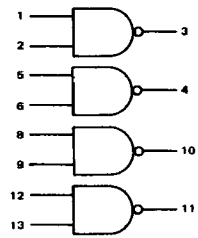
QUAD 2-INPUT
"NAND" BUFFER

MC957F · MC857F,P

This buffer element consists of four 2-input inverting drivers. This unit is designed especially for driving large capacitive loads at high speeds. An output emitter follower in series with a 150-ohm resistor drives the output to the high voltage level. A low saturation resistance transistor is turned on, pulling the output down to the low voltage level, and providing rapid discharge of capacitive loads.





Positive Logic: $3 = \overline{1 \cdot 2}$
Negative Logic: $3 = \overline{1+2}$

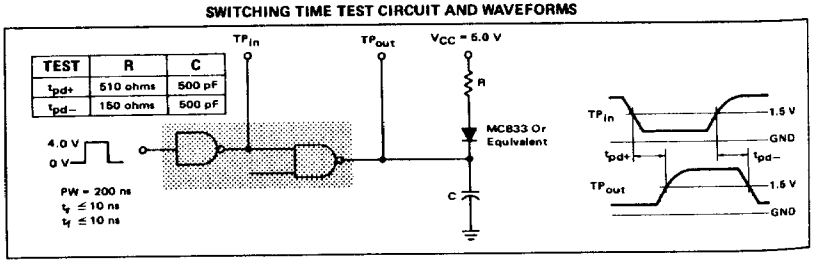
Input Loading Factor = 1
Output Loading Factor = 25
Total Power Dissipation = 170 mW typ/pkg
Propagation Delay Time = 35 ns typ

OPERATING RULES

- The outputs of the Quad Buffer may not be tied together.
- For increased current capability, the inputs and outputs of ¼MC957 and ¼MC958 can be paralleled (up to and including 4 common outputs). The combined output will equal 100 loads while each combined input will equal 4 loads.

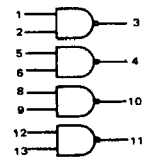
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST	R	C
t_{pd+}	510 ohms	500 pF
t_{pd-}	150 ohms	500 pF



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES										
		mA		Volts								
		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC957 −55°C		34	-2.00	1.40	2.10	0	4.00	-	-	4.50	5.50	-
MC957 +25°C		36	-2.50	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00
MC957 +125°C		32	-4.00	0.80	2.00	0	4.00	-	-	4.50	5.50	-
MC857 0°C		36	-2.00	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
MC857 +25°C		36	-2.50	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
MC857 +75°C		34	-3.00	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC957 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC857 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	-	1,2	-	-	-	-	14	-	-	7
	V_{OH}	3	2.50	-	2.60	-	2.50	-	↓	2.60	-	2.60	-	2.50	-	↓	-	3	1	-	-	-	-	-	↓	-	-	↓
		3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	2	-	-	-	-	-	-	-	-	
Short-Circuit Current	I_{SC}	3	-16	-	-18	-	-16	-	mAdc	-15	-	-16	-	-14	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,3,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,7
		2	-	2.0	-	2.0	-	5.0	μAdc	-	5.0	-	5.0	-	10	μAdc	-	-	-	-	-	2	-	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	3,14	-	-	-	-	1,7
Forward Current	I_F	1	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	1	2	-	-	-	14	-	7
		2	-	-1.60	-	-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33	mAdc	-	-	-	-	2	1	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	53.2	-	-	mAdc	-	-	-	60	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	-	7
	I_{max}	14	-	-	-	12	-	-	mAdc	-	-	-	16	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,5,7,8,12
Switching Times																	Pulse In	Pulse Out										
	t_{pd+}	1,3	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	1	3	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,3	-	-	15	40	-	-	ns	-	-	15	40	-	-	ns	1	3	-	-	-	-	-	14	-	-	-	7

Pins not listed are left open.

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D