Low-Voltage CMOS Octal D-Type Flip-Flop Flow Through Pinout

With 5 V–Tolerant Inputs and Outputs (3–State, Non–Inverting)

The MC74LCX574 is a high performance, non–inverting octal D–type flip–flop operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX574 inputs to be safely driven from 5 V devices.

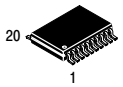
The MC74LCX574 consists of 8 edge–triggered flip–flops with individual D–type inputs and 3–state true outputs. The buffered clock and buffered Output Enable ($\overline{OE}$) are common to all flip–flops. The eight flip–flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW–to–HIGH Clock (CP) transition. With the $\overline{OE}$ LOW, the contents of the eight flip–flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. The $\overline{OE}$ input level does not affect the operation of the flip–flops. The LCX574 flow through design facilitates easy PC board layout.

- Designed for 2.3 to 3.6 V V_{CC} Operation
- 5 V Tolerant – Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V

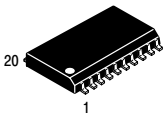
MC74LCX574

LCX

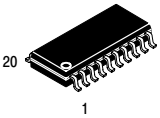
LOW–VOLTAGE CMOS OCTAL D–TYPE FLIP–FLOP



DT SUFFIX
PLASTIC TSSOP
CASE 948E



DW SUFFIX
PLASTIC SOIC
CASE 751D



M SUFFIX
PLASTIC SOIC EIAJ
CASE 967

PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
CP	Clock Pulse Input
D0–D7	Data Inputs
O0–O7	3–State Outputs

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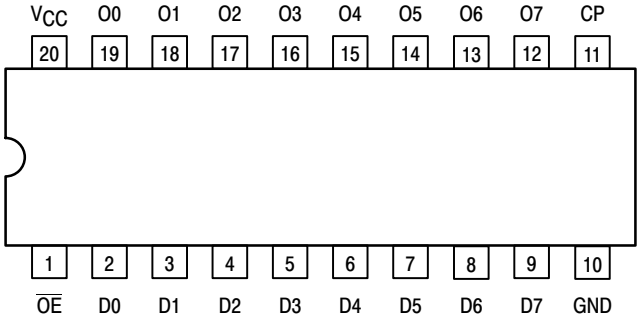


Figure 1. Pinout: 20–Lead (Top View)

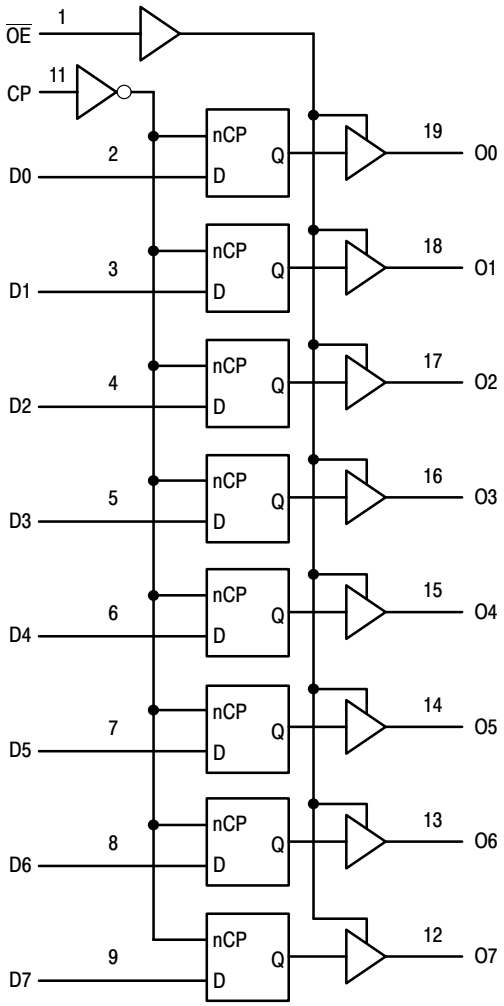


Figure 2. LOGIC DIAGRAM

TRUTH TABLE

INPUTS			INTERNAL LATCHES	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	Q	On	
L L	↑ ↑	l h	L H	L H	Load and Read Register
L	↥	X	NC	NC	Hold and Read Register
H	↥	X	NC	Z	Hold and Disable Outputs
H H	↑ ↑	l h	L H	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
Z = High Impedance State
↑ = Low–to–High Transition
↥ = Not a Low–to–High Transition; For I_{CC} Reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	–0.5 to +7.0		V
V_I	DC Input Voltage	$–0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$–0.5 \le V_O \le +7.0$	Output in 3–State	V
		$–0.5 \le V_O \le V_{CC} + 0.5$	Note 1.	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	–65 to +150		°C

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Output in HIGH or LOW State. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.0 1.5	3.3 3.3	3.6 3.6	V
V_I	Input Voltage		0		5.5	V
V_O	Output Voltage	(HIGH or LOW State) (3–State)	0 0		V_{CC} 5.5	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0 V – 3.6 V				–24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0 V – 3.6 V				24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.7 V – 3.0 V				–12	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.7 V – 3.0 V				12	mA
T_A	Operating Free–Air Temperature		–40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V		0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2.)	$2.7 \le V_{CC} \le 3.6$ V	2.0		V
V_{IL}	LOW Level Input Voltage (Note 2.)	$2.7 \le V_{CC} \le 3.6$ V		0.8	V
V_{OH}	HIGH Level Output Voltage	$2.7 \le V_{CC} \le 3.6$ V; I_{OH} = –100 μA	V_{CC} – 0.2		V
		V_{CC} = 2.7 V; I_{OH} = –12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = –18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = –24 mA	2.2		
V_{OL}	LOW Level Output Voltage	$2.7 \le V_{CC} \le 3.6$ V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 16 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	

2. These values of V_I are used to test DC electrical characteristics only.

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Characteristic	Condition	T_A = –40°C to +85°C		Unit
			Min	Max	
I_I	Input Leakage Current	2.7 V ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_I ≤ 5.5 V		±5.0	μA
I_{OZ}	3–State Output Current	2.7 ≤ V_{CC} ≤ 3.6 V; 0 V ≤ V_O ≤ 5.5 V; V_I = V_{IH} or V_{IL}		±5.0	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0 V; V_I or V_O = 5.5 V		10	μA
I_{CC}	Quiescent Supply Current	2.7 ≤ V_{CC} ≤ 3.6 V; V_I = GND or V_{CC}		10	μA
		2.7 ≤ V_{CC} ≤ 3.6 V; 3.6 ≤ V_I or V_O ≤ 5.5 V		±10	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 ≤ V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} – 0.6 V		500	μA

AC CHARACTERISTICS (t_R = t_F = 2.5 ns; C_L = 50 pF; R_L = 500 Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = –40°C to +85°C				
			V_{CC} = 3.0 V to 3.6 V		V_{CC} = 2.7 V		
			Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	1	150				MHz
t_{PLH} t_{PHL}	Propagation Delay CP to On	1	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time to HIGH and LOW Levels	2	1.5 1.5	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time from HIGH and LOW Levels	2	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns
t_s	Setup TIme, HIGH or LOW Dn to CP	1	2.5		2.5		ns
t_h	Hold TIme, HIGH or LOW Dn to CP	1	1.5		1.5		ns
t_w	CP Pulse Width, HIGH or LOW	3	3.3		3.3		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

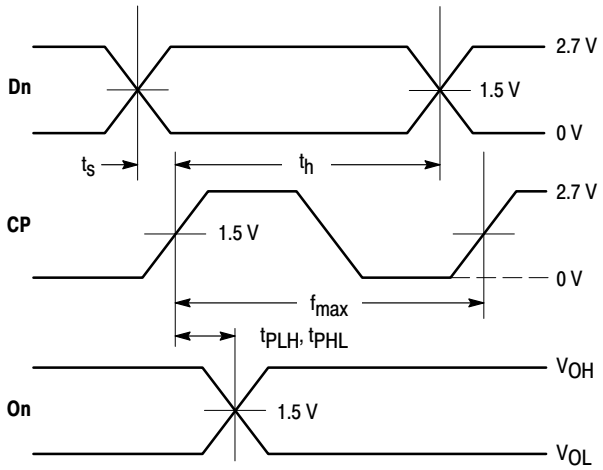
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = +25°C			Unit
			Min	Typ	Max	
V_{OLP}	Dynamic LOW Peak Voltage (Note 4.)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 4.)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V

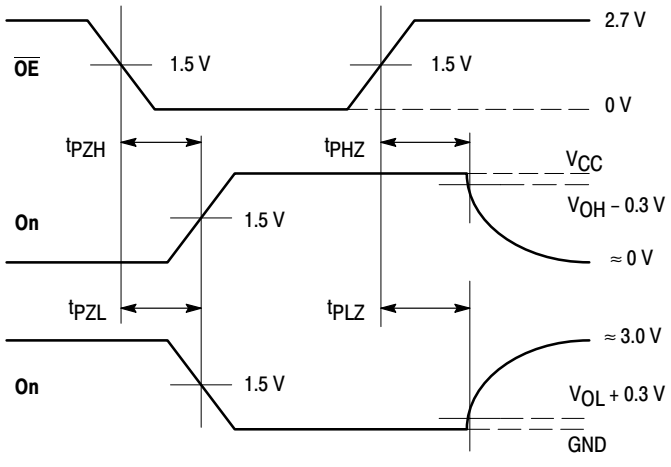
4. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW or LOW–to–HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

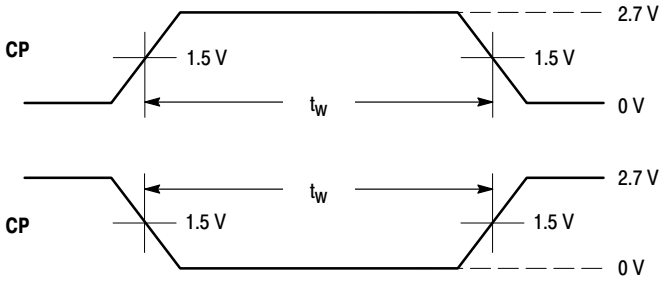
Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

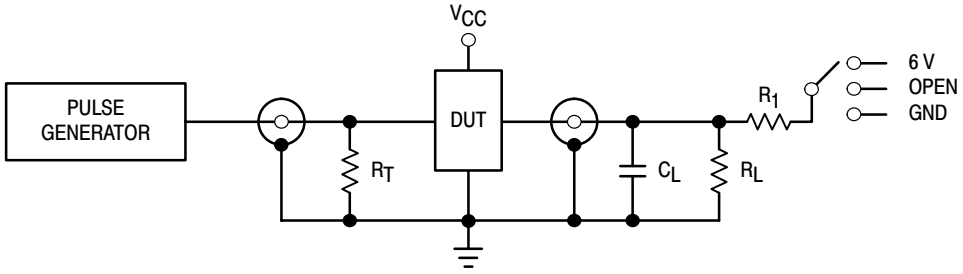


WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F$ = 2.5 ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8$ V, $V_{OH} \geq 2.0$ V

Figure 3. AC Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH}, t_{PHZ}	GND

C_L = 50 pF or equivalent (Includes jig and probe capacitance)
$R_L = R_1$ = 500 Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 4. Test Circuit