# LME49880 Overture®
# E-Series Dual JFET Input Audio Operational Amplifier

**Check for Samples: LME49880**

## FEATURES

- **Easily Drives 600Ω Loads**
- **Output Short Circuit Protection**

## APPLICATIONS

- **Ultra High Quality Audio Signal Processing**
- **Preamplifier**
- **Spectrum Analyzers**
- **Ultrasound Preamplifier**
- **Active Filters**

## KEY SPECIFICATIONS

- **Input Bias Current 5 pA (Typ)**
- **Power Supply Voltage Range ±5V to ±17 V**
- **THD+N ($A_V$ = 1, $V_{OUT}$ = 3$V_{RMS}$, $f_{IN}$ = 1kHz)**
  - **$R_L$ = 2kΩ 0.00003 % (Typ)**
  - **$R_L$ = 600Ω, 0.00003 % (Typ)**
- **Slew Rate ±17 V/µs (Typ)**
- **Gain Bandwidth Product 25 MHz (Typ)**
- **Open Loop Gain ($R_L$ = 600Ω) 115 dB (Typ)**
- **Input Noise Density 7 nV/√Hz (Typ)**
- **Input Offset Voltage 5 mV (Typ)**
- **CMRR 110 dB (Typ)**

## DESCRIPTION

The LME49880 is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity application. The LME49880 is developed in JFET technology and reducing the flicker noise as well as the noise corner frequency significantly. It combines low voltage noise density (7nV/√Hz) with very low THD+N (0.00003%). The LME49880 has a high slew rate of ±17 V/µs and an output current capability of ±22mA. It drives 600Ω loads to within 1.3V of either power supply voltage.

The LME49880 has a wide supply range of ±5V to ±17V. Its outstanding GAIN (120dB), and low input bias current (5pA) give the amplifier excellent operational amplifier DC performance. The LME49880 is unity gain stable and capable of driving complex loads with values as high as 100pF. It is available in an 8-lead narrow body SO PowerPAD.

## TYPICAL APPLICATION

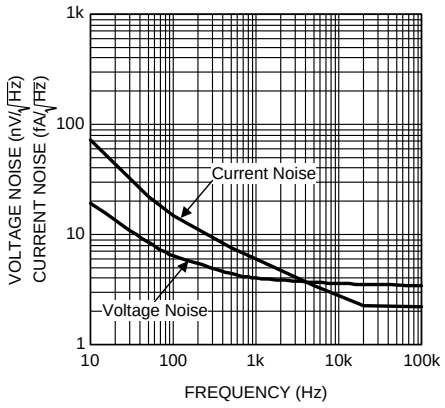


**Figure 1. Current Noise and Voltage Spectral Density**

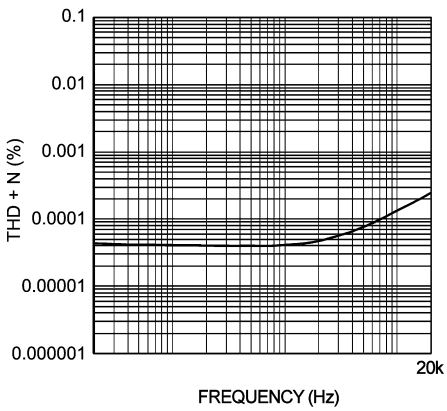


**Figure 2. THD+N vs Frequency $V_{CC}$ = ±15V, $V_O$ = 3$V_{RMS}$, $R_L$ = 600Ω**

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## CONNECTION DIAGRAM

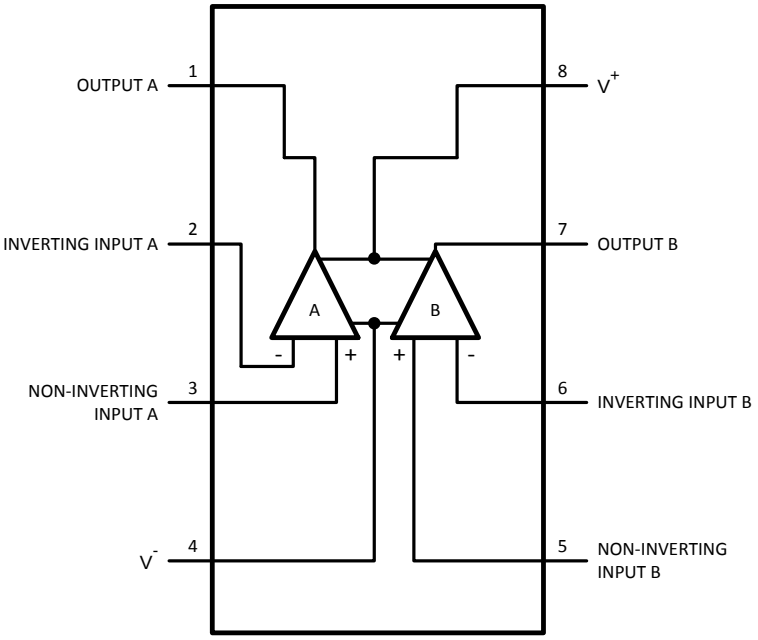



**Figure 3. Connection Diagram**
**See Package Number — DDA0008B**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS(1)(2)

| | | |
|---|---|---|
| Power Supply Voltage ($V_S = V^+ - V^-$) | | 36V |
| Storage Temperature | | −65°C to 150°C |
| Input Voltage | | (V-) - 0.3V to (V+) + 0.3V |
| Output Short Circuit(3) | | Continuous |
| Power Dissipation | | Internally Limited |
| ESD Rating(4) | | 2000V |
| ESD Rating(5) | | 200V |
| ESD Rating(6) | | 1000V |
| Junction Temperature | | 150°C |
| Thermal Resistance | $\theta_{JA}$ (SO PowerPAD) | 55°C/W |
| Solder Information | Infrared or Convection (20 sec) | 260°C |

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Amplifier output connected to GND, any number of amplifiers within a package.
(4) Human body model, applicable std. JESD22-A114C.
(5) Machine model, applicable std. JESD22-A115-A.
(6) Charge device model, applicable std JESD22-C101-A.

## OPERATING RATINGS

| | | |
|---|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ | $-40°C \le T_A \le 85°C$ |
| Supply Voltage Range | | $\pm5V \le V_S \le \pm17V$ |

## ELECTRICAL CHARACTERISTICS (1)

The following specifications apply for $V_S = \pm15V$, $T_A = 25°C$, unless otherwise specified.

| Symbol | Parameter | Conditions | LME49880 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (2) | Limit (3) | |
| THD+N | Total Harmonic Distortion + Noise | $A_V = 1$, $V_{OUT} = 3V_{RMS}$<br>$R_L = 2k\Omega$<br>$R_L = 600\Omega$ | <br>0.00003<br>0.00003 | <br><br>0.00009 | % (max) |
| GBWP | Gain Bandwidth Product | $A_V = 1k$, $R_L = 2k$ | 25 | 19 | MHz (min) |
| SR | Slew Rate | $R_L = 2k$ | ±17 | ±12 | V/µs (min) |
| $t_s$ | Settling time | $A_V = -1$, 10V step, $C_L = 100pF$<br>0.1% error range | 0.8 | | µs |
| $e_N$ | Equivalent Input Noise Voltage | $f_{BW}$ = 20Hz to 20kHz | 0.7 | 1.6 | $\mu V_{RMS}$ (max) |
| | Equivalent Input Noise Density | f = 1kHz<br>f = 10Hz | 7<br>16 | 11 | $nV/\sqrt{Hz}$ (max) |
| $i_N$ | Current Noise Density | f = 1kHz | 6 | | $fA/\sqrt{Hz}$ |
| $V_{OS}$ | Offset Voltage | | ±5 | ±10 | mV (max) |
| $\Delta V_{OS}/\Delta Temp$ | Average Input Offset Voltage Drift vs Temperature | $-40°C \le T_A \le 85°C$ | 3 | | µV/°C |
| PSRR | Power Supply Rejection Ratio | $V_{CC} = \pm5V$ to ±15V | 110 | | dB |
| $I_B$ | Input Bias Current | $V_{CM} = 0V$ | 5 | 150 | pA (max) |
| $I_{OS}$ | Input Offset Current | $V_{CM} = 0V$ | 2 | 100 | pA (max) |
| $V_{IN-CM}$ | Common-Mode Input Voltage Range | CMRR > 55dB | +11.5<br>–11.5 | (V+) –5V<br>(V-) +5V | V (min) |
| CMRR | Common-Mode Rejection | –10V<Vcm<10V | 110 | 90 | dB (min) |
| $A_{VOL}$ | Open Loop Voltage Gain | –10V<Vout<10V, $R_L = 600\Omega$ | 115 | 100 | dB (min) |
| | | –10V<Vout<10V, $R_L = 2k\Omega$ | 120 | 100 | dB (min) |
| | | –10V<Vout<10V, $R_L = 10k\Omega$ | 120 | 100 | dB (min) |
| $V_{OUTMAX}$ | Maximum Output Voltage Swing | $R_L = 600\Omega$ | ±13.2 | ±12.0 | V (min) |
| | | $R_L = 2k\Omega$ | ±13.2 | ±12.5 | V (min) |
| | | $R_L = 10k\Omega$ | ±13.2 | ±12.5 | V (min) |
| $I_{OUT}$ | Output Current | $R_L = 600\Omega$, $V_S = \pm17V$ | ±26 | | mA |
| $I_{OUT-CC}$ | Instantaneous Short Circuit Current | | ±48 | | mA |
| $R_{OUT}$ | Output Impedance | $f_{IN}$ = 10kHz, Open-Loop | 15 | | Ω |
| $I_S$ | Total Quiescent Current | $I_{OUT} = 0mA$ | 14 | 18 | mA (max) |

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at $T_A$ = +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) Datasheet min/max specification limits are specified by test or statistical analysis.

## TYPICAL PERFORMANCE CHARACTERISTICS

**THD+N vs Frequency $V_{CC}$ = 15V, $V_{OUT}$ = 3V $R_L$ = 2kΩ**

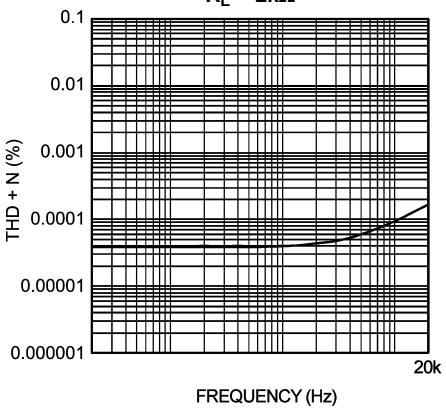



**Figure 4.**

**THD+N vs Frequency $V_{CC}$ = 15V, $V_{OUT}$ = 3V $R_L$ = 600Ω**

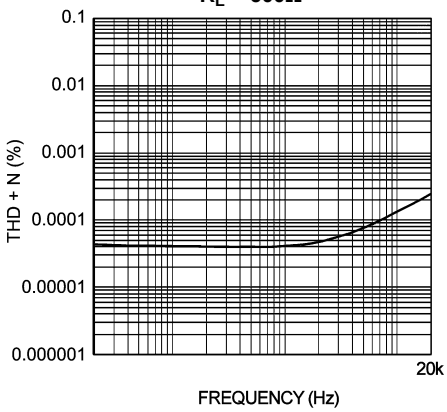



**Figure 5.**

**THD+N vs Frequency $V_{CC}$ = 18V, $V_{OUT}$ = 3V $R_L$ = 2kΩ**

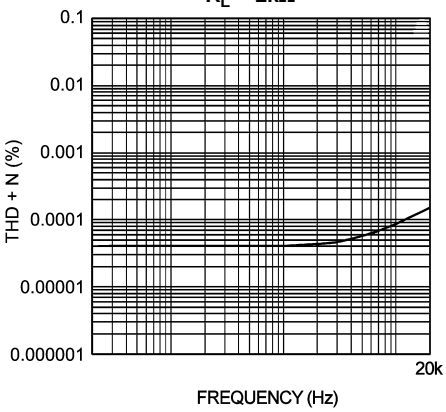



**Figure 6.**

**THD+N vs Frequency $V_{CC}$ = 18V, $V_{OUT}$ = 3V $R_L$ = 600Ω**

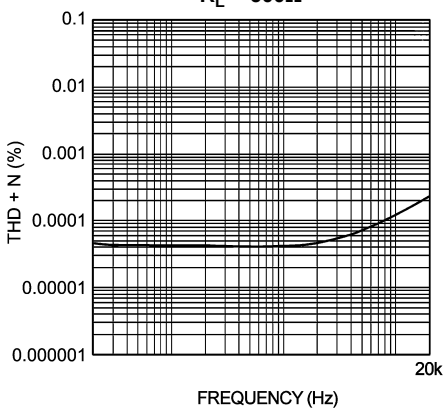



**Figure 7.**

**THD+N vs Output Voltage $V_{CC}$ = 15V $R_L$ = 2kΩ**

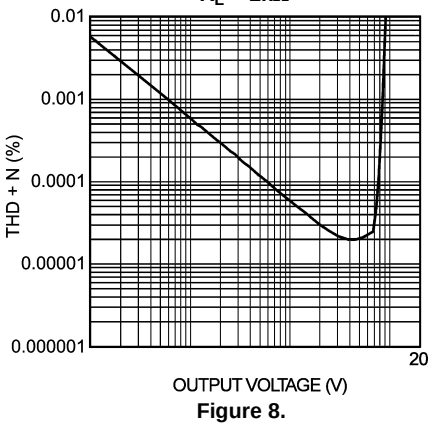



**Figure 8.**

**THD+N vs Output Voltage $V_{CC}$ = 15V $R_L$ = 600Ω**

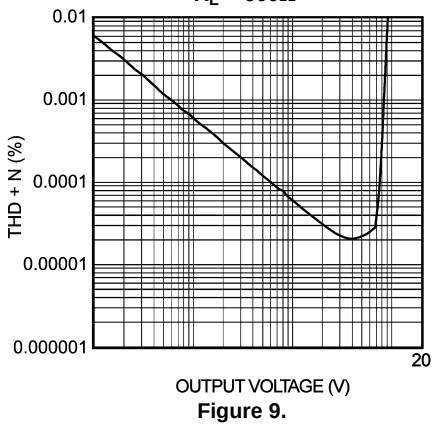



**Figure 9.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**THD+N vs Output Voltage**
**$V_{CC}$ = 18V**
**$R_L$ = 2kΩ**

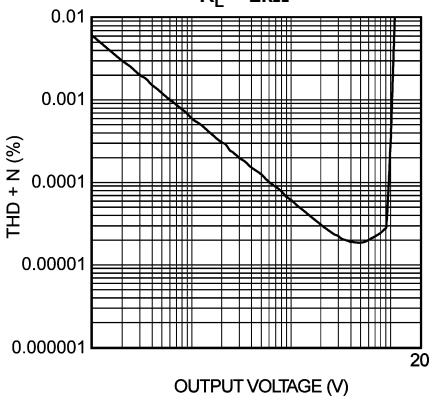



**Figure 10.**

**THD+N vs Output Voltage**
**$V_{CC}$ = 18V**
**$R_L$ = 600Ω**

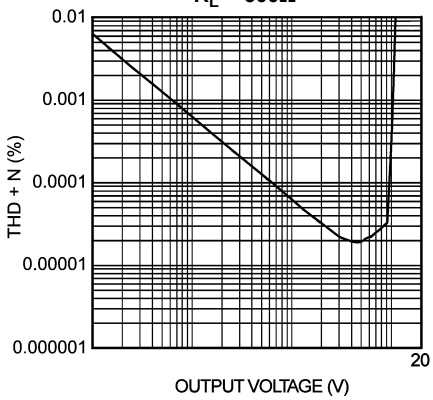



**Figure 11.**

**+PSRR vs Frequency**

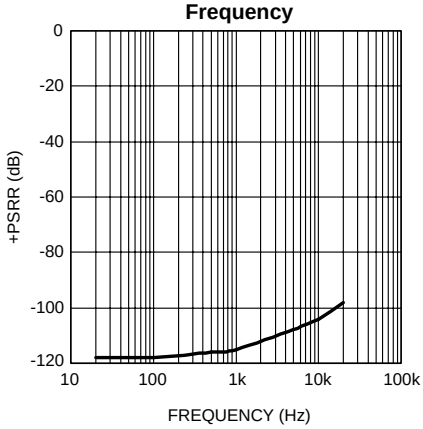



**Figure 12.**

**−PSRR vs Frequency**

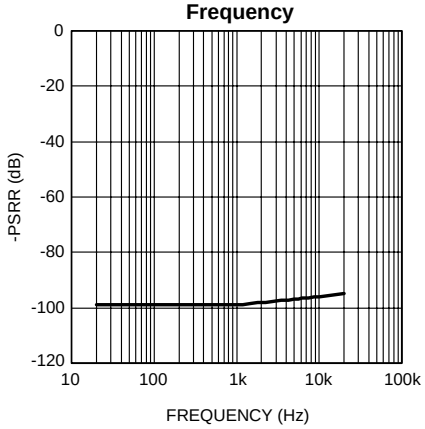



**Figure 13.**

**CMRR vs Frequency**

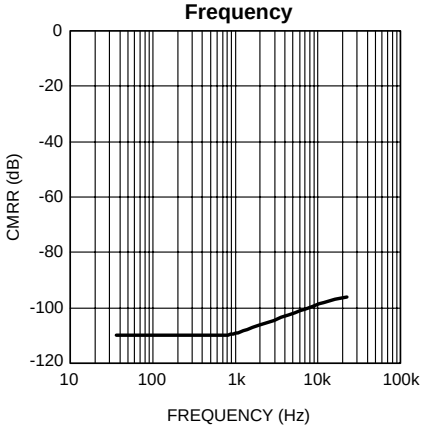



**Figure 14.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**Current Noise vs Frequency**

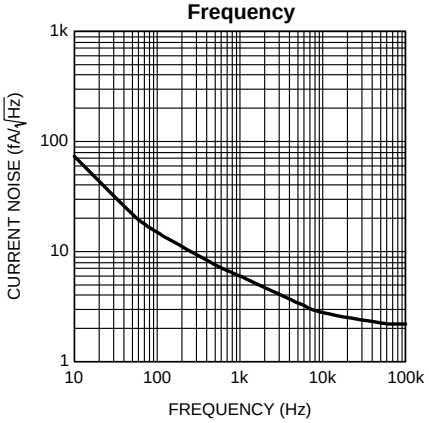



**Figure 15.**

**Voltage Noise vs Frequency**

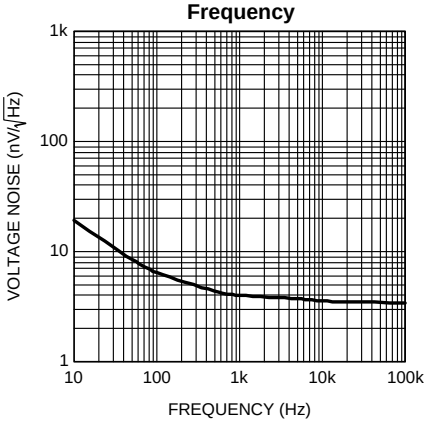



**Figure 16.**

# APPLICATION HINTS

## OUTPUT DRIVE AND STABILITY

The LME49880 is unity gain stable within the part's common-mode range. Some instabilities may occur near the limit of the common-mode range. It can drive resistive load 600Ω with output circuit with a typical 26mA. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straight forward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted. The internal short-circuit protection of LME49880 also prevent the device from damage when the either outputs are being shorted.

The effective load impedance (including feedback resistance) should be kept above 600Ω for fast settling. Load capacitance should also be minimized if good settling time is to be optimized. Large feedback resistors will make the circuit more susceptible to stray capacitance, so in high-speed applications keep the feedback resistors in the 1kΩ to 2kΩ range whenever practical.

## OUTPUT COMPENSATION

In most of the audio applications, the device will be operated in a room temperature and compensation networks are not necessary. However, the consideration of network as shown in Figure 17 may be taken into account for some of the high performance audio applications such as high speed data conversion or when operating in a relatively low junction temperature. The compensation network will also provide a small improvement in settling time for the response time demanding applications.

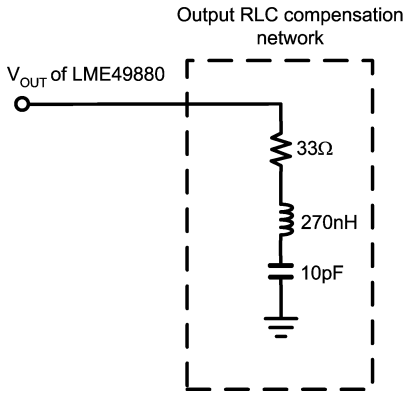



**Figure 17. LME49880 Output Compensation Network**

## SO PowerPAD EXPOSED PAD PACKAGE

The LME49880 has an exposed pad on the bottom side of the IC package. Connect the exposed pad to pin 4 (V-) of the IC. The PCB footprint for the exposed pad should be a open polygon of copper to provide a good thermal path away from the LME49880. Use multiple vias on the exposed pad to create better thermal conductivity. Do not route traces below the exposed pad as they risk shorting to the exposed pad.

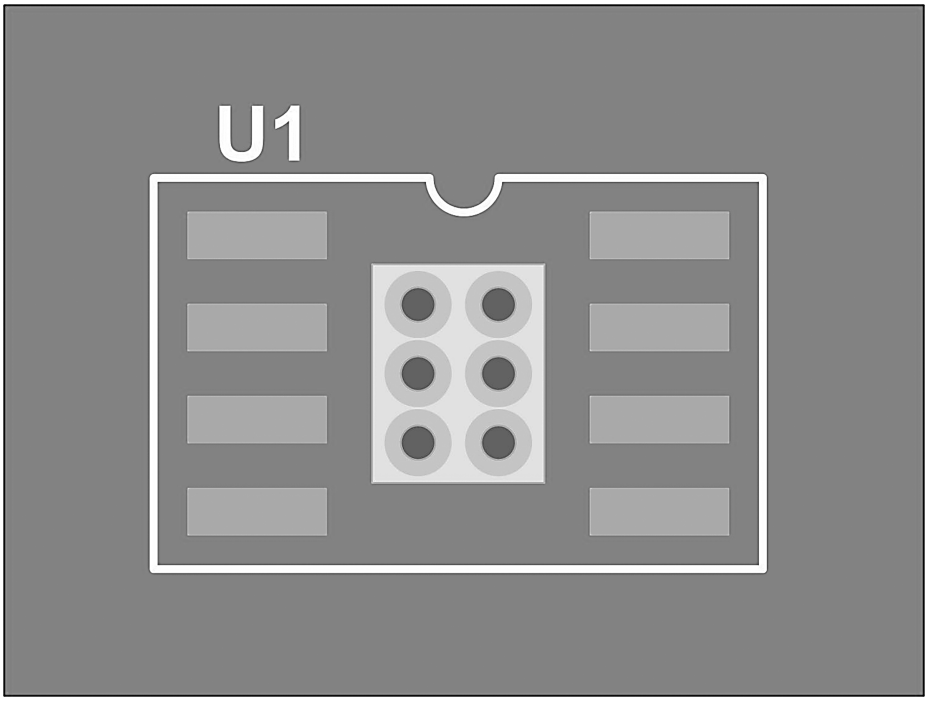



**Figure 18. LME49880 Output Compensation Network**

## SUPPLY BYPASSING

To achieve a low noise and high-speed audio performance, power supply bypassing is extremely important. Applying multiple bypass capacitors is highly recommended. From experiment results, a 10µF tantalum, 2.2µF ceramic, and a 0.47µF ceramic work well. All bypass capacitors leads should be very short. The ground leads of capacitors should also be separated to reduce the inductance to ground. To obtain the best result, a large ground plane layout technique is recommended and it was applied in the LME49880 evaluation board.

## APPLICATION INFORMATION

### SETTLING TIME AND SLEW RATE MEASUREMENTS

The settling time of LME49880 may be verified using the test circuit in Figure 19. The LME49880 is connected for inverting operation, and the output voltage is summed with the input voltage step. When the LME49880's output voltage is equal to the input voltage, the voltage on the PROBE 1 will be zero. Any voltage appearing at this point will represent an error. And the settling time is equal to the time required for the error signal displayed on the oscilloscope to decay to less than one-half the necessary accuracy. For a 10V input signal, settling time to 0.01% (1mV) will occur when the displayed error is less than 0.5mV. Since settling time is strongly dependent on slew rate, settling will be faster for smaller signal swings. The LME49880's inverting slew rate is faster than its non-inverting slew rate, so settling will be faster for inverting applications, as well. It is important to note that the oscilloscope input amplifier may be overdriven during a settling time measurement, so the oscilloscope must be capable of recovering from overdrive very quickly. The signal generator used for this measurement must be able to drive 50Ω with a very clean $\pm 10V_{PP}$ square wave. The Slew Rate of LME49880 tells how fast it responses to a transient or a step input. It may be measured by the test circuit in Figure 20. The Slew Rate of LME49880 is specified in close-loop gain = -1 when the output driving a 1kΩ load at $20V_{PP}$. The LME49880 behaves very stable in shape step response and have a minimal ringing in both small and large signal step response (See TYPICAL PERFORMANCE CHARACTERISTICS). The slew rate typical value reach as high as ±18V/µS was measured when the output reach -20V refer to the start point when input voltage equals to zero.

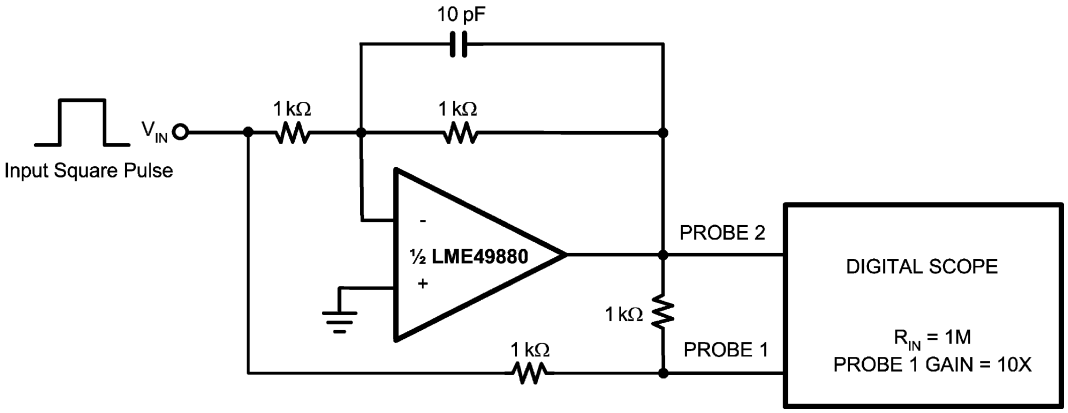



**Figure 19. Settling Time Test Circuit**

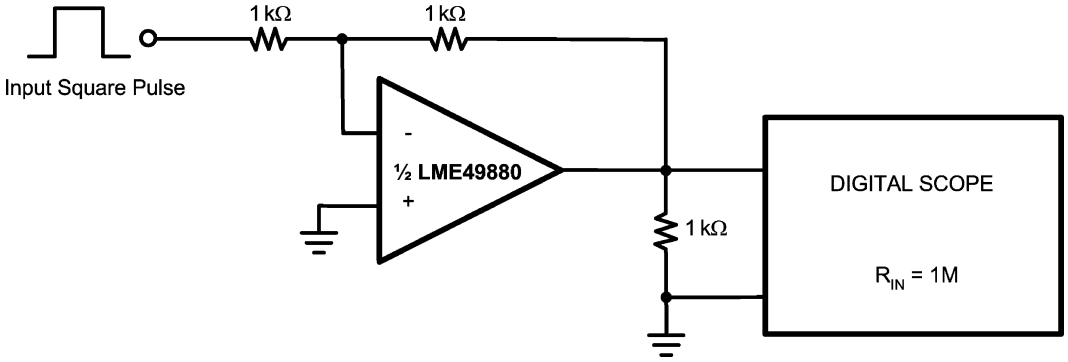



**Figure 20. Slew Rate Test Circuit**

## DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49880 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49880's low residual distortion is an input referred internal error. As shown in Figure 21, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 21.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

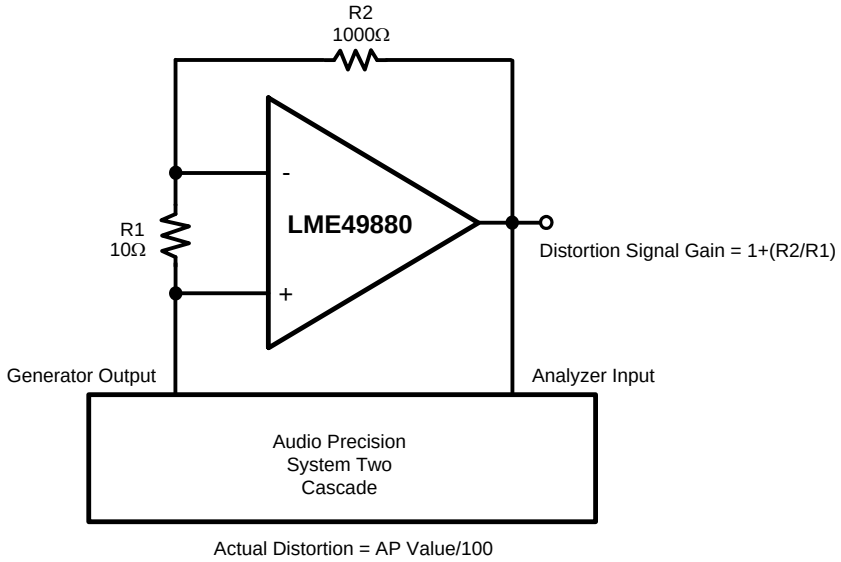
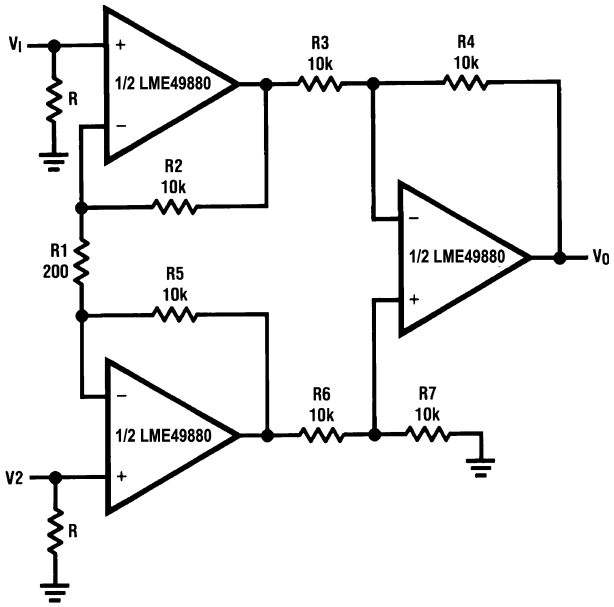



**Figure 21. THD+N and IMD Distortion Test Circuit**

## TYPICAL APPLICATIONS




If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

V0 = 101(V2 − V1)

**Figure 22. Balanced Input Mic Amp**

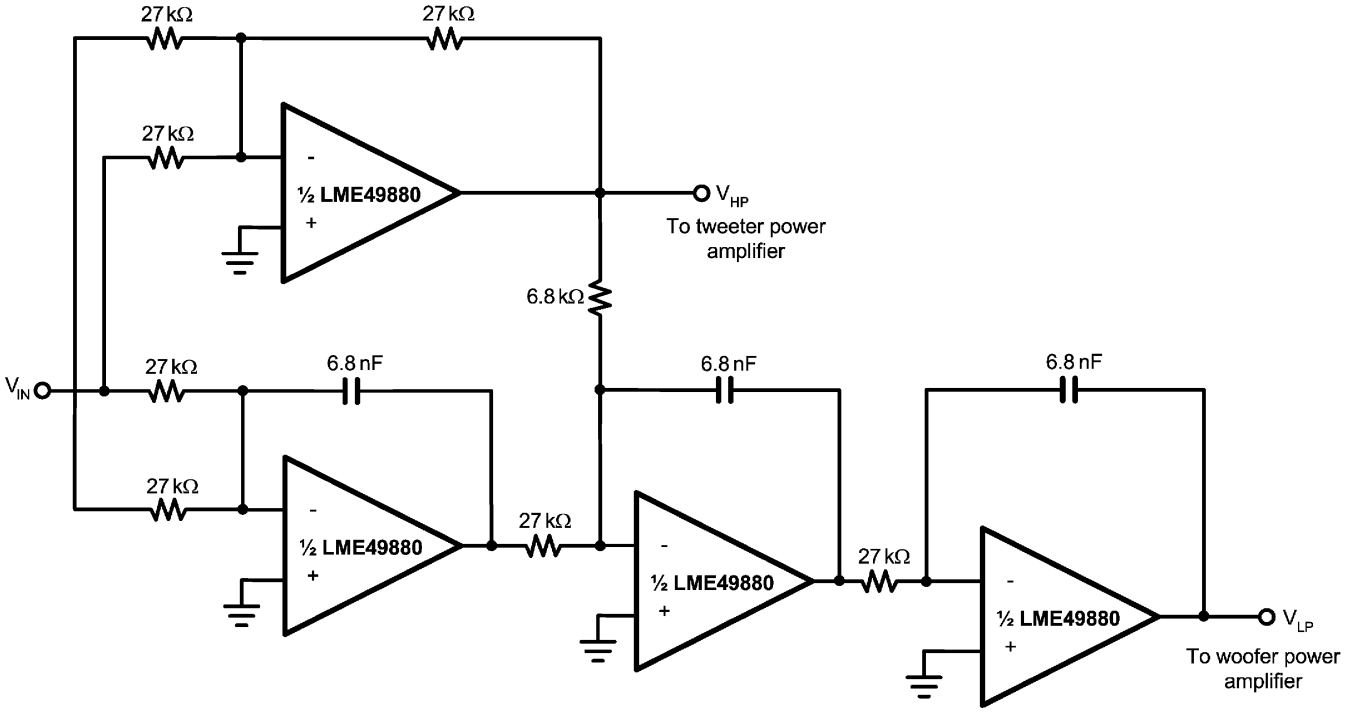



**Figure 23. Active Crossover Network for Loudspeaker**

## REVISION HISTORY

| Rev | Date | Description |
|---|---|---|
| 1.0 | 12/16/09 | Initial released. |
| 1.01 | 01/08/10 | Input text edits. |
| 1.02 | 03/22/10 | Edited the scaling (Y-axis) on the THD+N curves to match the limits described in the datasheet. |
| C | 04/04/13 | Changed layout of National Data Sheet to TI format. |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LME49880MR/NOPB | OBSOLETE | SO PowerPAD | DDA | 8 | | TBD | Call TI | Call TI | -40 to 85 | L49880<br>MR | |
| LME49880MRX/NOPB | OBSOLETE | SO PowerPAD | DDA | 8 | | TBD | Call TI | Call TI | -40 to 85 | L49880<br>MR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

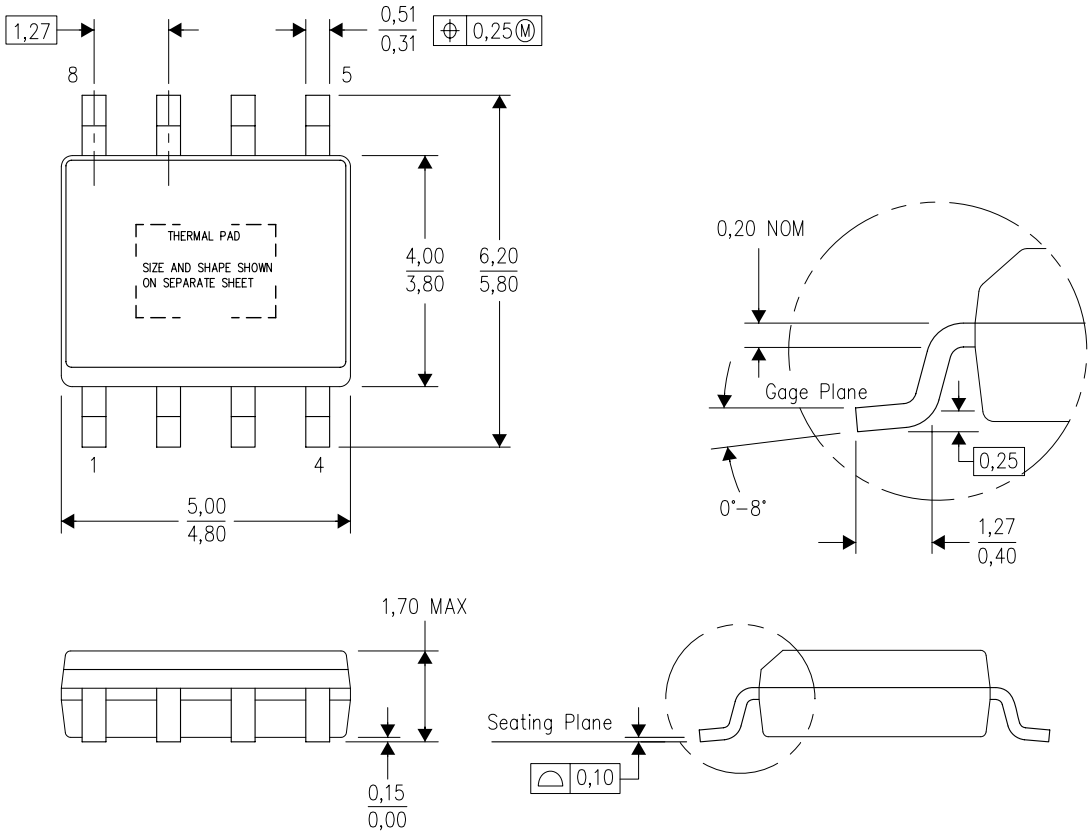
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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