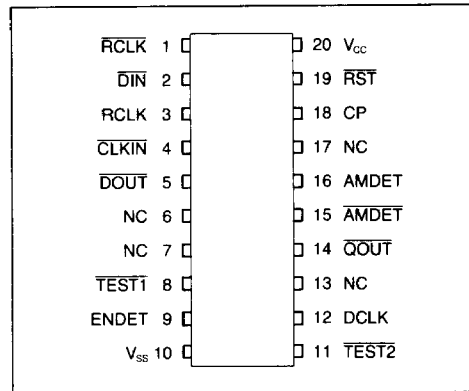


Hard Disk Address Mark Detector

FEATURES

- Single +5 Volt Power Supply
- Decodes A1-0A
- Synchronous Clock/Data Outputs
- 5 MBit Data Rate
- Address Mark Detection
- 20 Pin DIP
- n-Channel COPLAMOS[®] Silicon Gate Technology

PIN CONFIGURATION

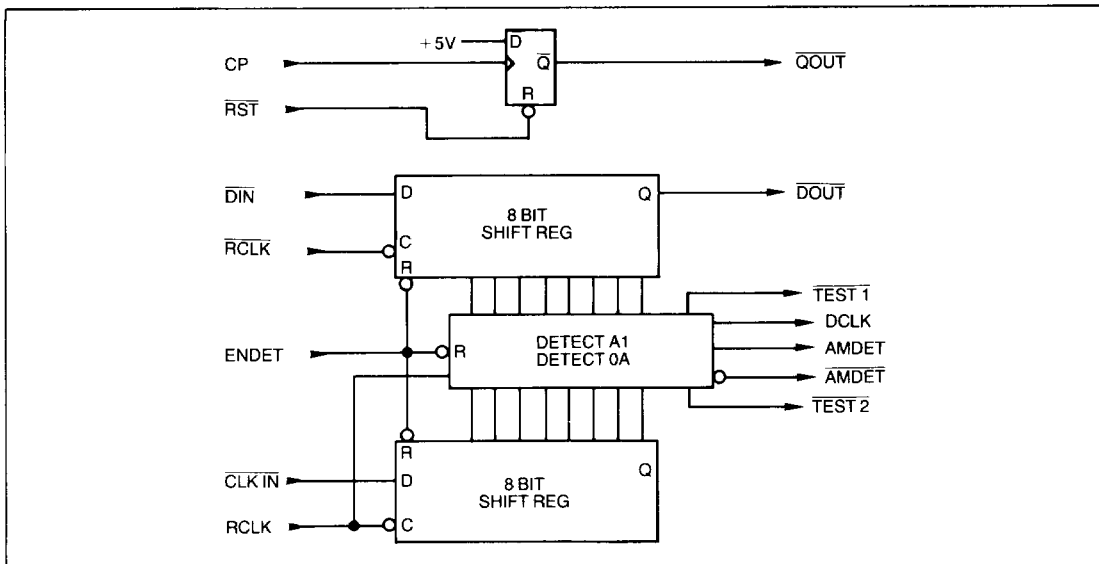


GENERAL DESCRIPTION

The HDC 1100-03 Address Mark Detector Provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM clocks and data are fed to the device along with a window clock generated by an external data separator. The HDC 1100-03 searches the data stream

for a DATA = A1, CLK = 0A pattern and produces an AMDET signal when the pattern has been found. NRZ data is output from the device for driving a serial/parallel converter. An uncommitted latch is also provided for use by the data separator circuitry if required.

SECTION VI



DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	RCLK	READ CLOCK	Complimentary clock inputs used to clock DIN and CLK IN into the AM detector.
3	RCLK	READ CLOCK	
2	DIN	DATA INPUT	MFM data pulses from the external Data Separator are connected on this line.
4	CLK IN	CLOCK INPUT	MFM clock pulses from the external Data Separator are connected on this line.
5	DO \overline{U} T	DATA OUTPUT	Data Output from the internal Data Shift register, synchronized with DCLK.
6, 7, 13, 17	NC	No Connection	To be left open by the user.
8	TEST 1	TEST 1	To be left open by the user.
11	TEST 2	TEST 2	
9	ENDET	ENABLE DETECTION	A logic 1 on this line enables the detection logic to search for a data A _{1,6} and clock.
10	V _{SS}	V _{SS}	GROUND.
12	DCLK	DATA CLOCK	Clock output that is synchronized with DATA OUT (Pin 5).
14	QO \overline{U} T	LATCH OUTPUT	Signal output from the uncommitted latch.
15	AMDET	ADDRESS MARK DETECT	Complimentary Address Mark Detector output. These signals will go active when a Data = A _{1,6} Clock = 0A _{1,6} pattern is detected in the data stream.
16	AMDET	ADDRESS MARK DETECT	
18	CP	CLOCK PULSE	A low-to-high transition on this line will cause the QO \overline{U} T (Pin 14) to be latched at a logic 0.
19	R \overline{S} T	RESET	A logic 0 on this line will cause the QO \overline{U} T (Pin 14) signal to be set at a logic 1.
20	V _{CC}	V _{CC}	+5V power supply input.

OPERATION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and AMDET, AMD \overline{E} T, DCLK, and DATA OUT will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the DIN line (Pin 2) and shifted on the high-to-low transition of RCLK (Pin 1). NRZ clocks are entered on the CLK IN line, and shifted on the high-to-low transition of RCLK (Pin 3). The DO \overline{U} T line (Pin 5) is tied to the last stage of the Internal Data Shift register and will reflect information clocked into the DIN line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = A_{1,6} CLK = 0A_{1,6} pattern. When this pattern is detected, AMDET will be set to a logic 0 and AMD \overline{E} T will be set to a logic 1. AMDET and AMD \overline{E} T will remain latched until the device is re-initialized by forcing

ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the DO \overline{U} T line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high-frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the QO \overline{U} T (Pin 14) to a logic 0. QO \overline{U} T may be reset back to a logic 1 by a low level on the RST line (Pin 19).

TEST1 and TEST2 are output lines. TEST1 is an active low pulse when an A_{1,6} is detected, and TEST2 is an active low pulse when a 0A_{1,6} is detected. These signals are used for test points and therefore should be left open by the user if not required.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +50°C
Storage Temperature Range	-55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+7.0V
Negative Voltage on any I/O Pin, with respect to ground	-0.2V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rat... generation of the device at these or at any other condition above those indicated in the operational sections of...

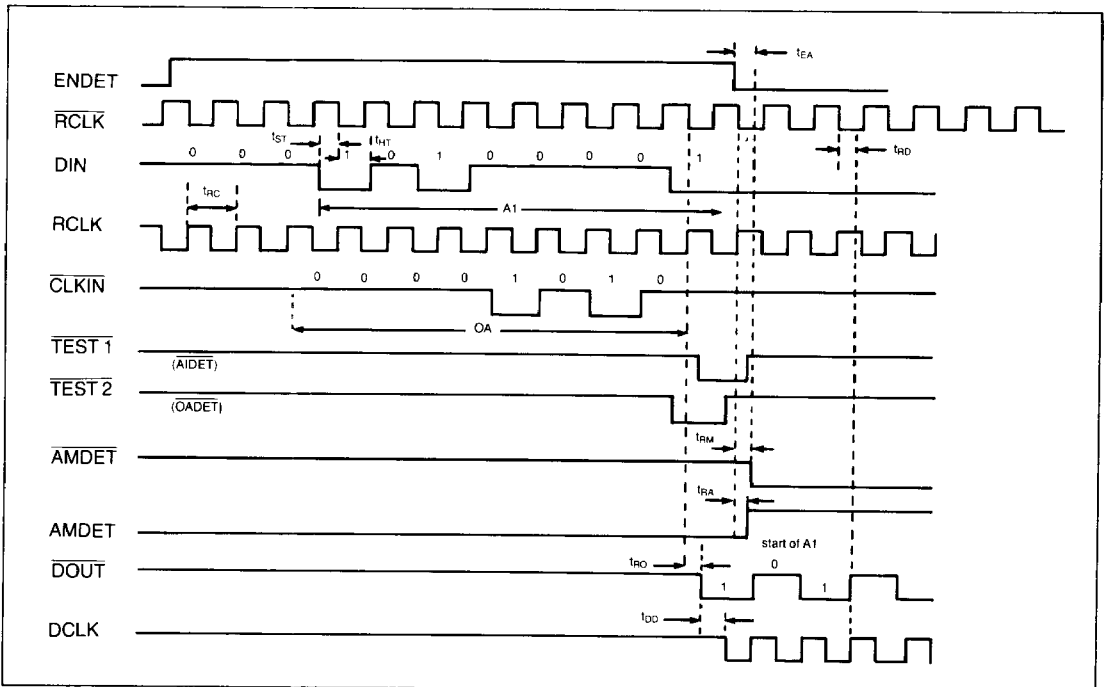
PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP ¹	MAX	UNIT	CONDITION
V _{IL}	Input Low Voltage	-0.2		0.7	V	
V _{IH}	Input High Voltage	2.4			V	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 3.2 mA
V _{OH}	Output High Voltage	2.4			V	I _{OH} = -200µA
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	
I _{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP ¹	MAX	UNIT	CONDITION
f _{RCLK}	RCLK Frequency			5.25	MHZ	
t _{ST}	Data Setup time	40			nsec	
t _{HT}	Data Hold time	10			nsec	
t _{DD}	DOUT to DCLK DELAY			110	nsec	
t _{RD}	↓ RCLK to ↓ DCLK			120	nsec	
t _{RA}	↓ RCLK to ↓ AMDET			115	nsec	
t _{RM}	↓ RCLK to ↓ AMDET			125	nsec	
t _{RO}	↓ RCLK to DOUT			135	nsec	
t _{EA}	↓ ENDET to ↓ AMDET			130	nsec	
t _{RQ}	↓ RST to ↓ QOUT			110	nsec	
t _{RW}	Pulse width of RST	50			nsec	
t _{CW}	CP Pulse width	90			nsec	
t _{CO}	* CP to ↓ QOUT			106	nsec	



SECTION VI