Agilent HDMP-2630B/2631B 2.125/1.0625 GBd Serdes Circuits

Data Sheet

Description

This data sheet describes the HDMP-2630B/2631B serdes devices for 2.125 GBd serial data rates. References to SSTL_2 in the text will also apply to SSTL_3; however, there are separate tables and figures showing voltage values and connection diagrams for these two logic families.

The HDMP-2630B/2631B Serdes are silicon bipolar integrated circuits in a metallized QFP package. They provide a low-cost physical layer solution for 2.125 GBd serial link interfaces including a complete Serialize/Deserialize (Serdes) function with transmit and receive sections in a single device. The HDMP-2630B/2631B are also capable of operating on 1.0625 GBd serial links. Input pins TX_RATE and RX_RATE select the data rates on the transmit and receive sides respectively.

As shown in Figure 1, the transmitter section accepts 10-bit wide parallel SSTL_2 data (TX[0:9]) and a 106.25 MHz SSTL_2 byte clock (TBC) and serializes them into a high-speed serial stream. The parallel data is expected to be "8B/10B" encoded data or equivalent. At the source, TX[0:9] and TBC switch synchronously with respect to a 106.25 MHz clock internal to the sender. New data are emitted on both edges of TBC; this is called Double Data Rate (DDR). The HDMP-2630B/2631B find a sampling window between the two edges of TBC to latch TX[0:9] data into the input register of the transmitter section when TX_RATE =1. If TX_RATE = 0, the user must ensure no data transitions on the falling edge of TBC and this edge is used to latch in parallel data resulting in a 1.0625 GBd serial stream.

The transmitter section's PLL locks to the 106.25 MHz TBC. This clock is then multiplied by 20 to generate the 2125 MHz serial clock for the high-speed serial outputs. The high speed outputs are capable of interfacing directly to copper cables or PCB traces for electrical transmission or to a separate fiber optic module for optical transmission.

Features

- **10-bit wide parallel Tx, Rx busses**
- **106.25 MHz TBC and RBC[0:1]**
- **Option to set Tx and Rx serial data rates separately**
- **Parallel data I/O, clocks and control compatible with SSTL_2 (HDMP-2630B) or SSTL_3 (HDMP-2631B)**
- **Differential PECL or LVTTL REFCLK at 106.25 MHz or 53.125 MHz**
- **Double data rate transfers**
- **Source synchronous clocking of transmit data**
- **Source centered or source synchronous clocking of receive data**
- **Dual or single receive byte clocks**
- **Parallel loopback mode**
- **Differential BLL serial I/O with on-chip source termination**
- **14 mm, 64-pin MQFP package**
- **Single +3.3V power supply**

Applications

- **Fibre channel arbitrated loop and trunks**
- **Fast serial backplanes**
- **Clusters**

Ordering Information

Part Number	Parallel I/O
HDMP-2630B	SSTL_2
HDMP-2631B	SSTL_3

The high-speed outputs include user-controllable skin-loss equalization to improve performance when driving copper lines.

The receiver section accepts a serial electrical data stream at 1.0625 or 2.125 GBd and recovers 10-bit wide parallel data. The receiver PLL locks onto the incoming serial signal and recovers the high-speed incoming clock and data. The serial data is converted back into 10-bit parallel data, optionally recognizing the first seven bits of the K28.5+ comma character to establish byte alignment. If K28.5+ detection is enabled, the receiver section is able to detect comma characters at 1.0625 GBd or 2.125 GBd depending on the value of the RX_RATE pin.

The recovered parallel data is presented at SSTL_2 compatible outputs RX[0:9], along with a pair of 106.25 MHz SSTL_2 clocks, RBC[0] and RBC[1], that are 180 degrees out of phase from one another and which represent the remote clock. Rising edges of RBC[0] and RBC[1] may be used to latch RX[0:9] data at the destination.

For short distances, there may be a need to have ASICs communicate directly using parallel Tx and Rx lines without the serdes intermediary. To enable this, the Tx and Rx parallel timing schemes must be symmetrical. When RBC_SYNC = 1 and RX_RATE = 1 such symmetry is obtained. In this mode, the RX[0:9] lines switch simultaneously with the rising and falling edges of RBC[1] or RBC[0] just as the TX[0:9] lines switch simultaneously with TBC.

If RX_RATE = 0 and RBC_SYNC = 1 then the RX[0:9] lines switch with the rising edges of RBC[1] just as the TX[0:9] lines switch with the rising edges of TBC. If RBC_SYNC = 0 then RX[0:9] data may be latched on the rising edges of RBC[1] and RBC[0]. In this latter mode, the RBC[0:1] clocks operate at a 53.125 MHz rate.

In summary, by setting RBC_SYNC = 0 the timing of transmit and receive parallel data with respect to TBC and RBC[0:1] may be arranged so that the upstream protocol device can generate and latch data very simply. This is the source centered mode of operation (case A and C in Table 1, page 8). Alternatively, setting RBC_SYNC = 1 provides for timing symmetry between Tx and Rx parallel lines at both 1.0625 GBd and 2.125 GBd rates. This is the source synchronous mode of operation (case B and D in Table 1, page 8).

Note when EN_CDET = 1, the first transition of byte 0 of a comma will either coincide with the rising edge of RBC[1] or precede it. This applies regardless of the RX_RATE setting.

Table 1 summarizes the behavior of the Rx parallel section under all values of RX_RATE and RBC_SYNC. For test purposes, the transceiver provides for on-chip parallel to parallel local loopback functionality controlled through the EWRAP pin. Additionally, the byte alignment feature via detection of the first seven bits of the K28.5+ character may be disabled. This may be useful in proprietary applications which use alternative methods to align the parallel data.

The HDMP-2630B/2631B accept either a differential PECL or a LVTTL reference clock input. This input may be full rate (106.25 MHz, REF_RATE = 0) or half rate (53.125 MHz, REF_RATE = 1).

HDMP-2630B/2631B Block Diagram

The HDMP-2630B/2631B (Figure 2) are designed to transmit and receive 10-bit wide parallel data over high-speed serial communication lines. The parallel data applied to the transmitter is expected to be encoded per the 8B/10B encoding scheme with special reserved characters for link management purposes. Other encoding schemes will also work as long as they provide DC balance and a sufficient number of transitions. The HDMP-2630B/2631B incorporate the following:

- SSTL_2 or SSTL_3 Parallel I/O
- High Speed Phase Locked Loops
- Parallel to Serial Converter
- High Speed Serial Clock and Data Recovery Circuitry
- Comma Character Recognition per Fibre Channel Specifications
- Byte Alignment Circuitry
- Serial to Parallel Converter

INPUT LATCH

The transmitter accepts 10-bit wide single ended SSTL_2 parallel data at inputs TX[0:9]. The SSTL_2 TBC clock provided by the sender of the transmit data is used as the transmit byte clock. The TX[0:9] and TBC signals must be properly aligned as shown in Figure 3. If TX_RATE = 1, TX[0:9] data are latched between both edges of TBC. If TX_RATE = 0, TX[0:9] data are latched on the falling edge of TBC. The TX[0:9] and TBC inputs are unterminated SSTL_2 inputs per section 4.1 of the SSTL_2 standard and section 3.3.1 of the SSTL_3 standard (Figure 11).

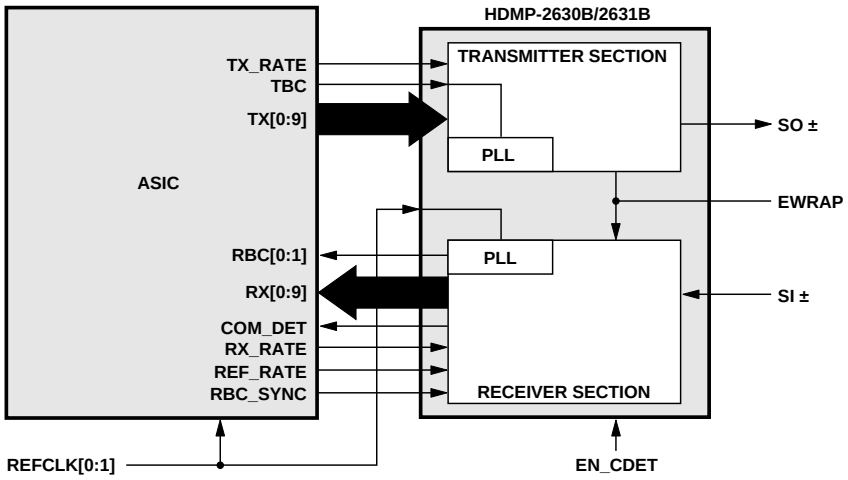


Figure 1. Typical application using HDMP-2630B/2631B.

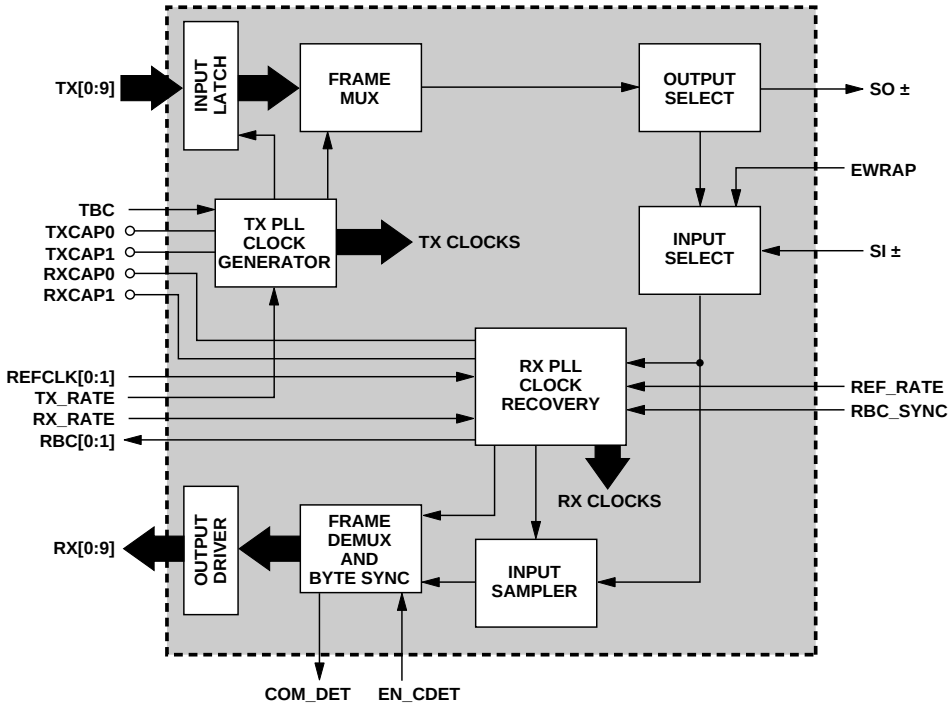


Figure 2. Block diagram of HDMP-2630B/2631B.

TX PLL/CLOCK GENERATOR

The Transmitter Phase Locked Loop and Clock Generator block is responsible for generating all internal clocks needed by the transmitter section to perform its functions. These clocks are based on the supplied transmit byte clock (TBC). Incoming data must be synchronous with TBC (Figures 3a-3b). Use of TBC to determine sampling points to latch data obviates the need for PLLs in the data source.

FRAME MUX

The FRAME MUX accepts 10-bit wide parallel data from the INPUT LATCH. Using internally generated high-speed clocks, this parallel data is multiplexed into a 2.125 GBd serial data stream. The data bits are transmitted sequentially from TX[0] to TX[9]. The leftmost bit of K28.5+ is on TX[0].

OUTPUT SELECT

The OUTPUT SELECT block picks the serial data to drive on to the serial output line. In normal operation, the serialized TX[0:9] data is placed at SO± . In parallel loopback (EWRAP=1) mode, the SO± pins are held static at logic 1 and the internal serial output signal going to the INPUT SELECT block of the receiver section is used to generate RX[0:9]. In addition, the OUTPUT SELECT block allows the user to control the amount of pre-emphasis used on the SO± pins. If pre-emphasis is used, 0→1 and 1→0 transitions on SO± have greater amplitude than 0→0 and 1→1 transitions. This increased amplitude is used to offset the effects of skin loss and dispersion on long PCB transmission lines. Pre-emphasis is controlled by the EQAMP pin (Table 2 and Figure 9).

INPUT SELECT

The INPUT SELECT block picks the serial data that will be parallelized to drive RX[0:9]. In normal operation, serial data is accepted at SI± . In parallel loopback (EWRAP = 1) mode, the internal serial output signal from the OUTPUT SELECT block of the transmitter section is used to generate RX[0:9].

RX PLL/CLOCK RECOVERY

The Receiver Phase Locked Loop and Clock Recovery block is responsible for frequency and phase locking onto the incoming serial data stream and recovering the bit and byte clocks. An automatic locking feature allows the Rx PLL to lock onto the input data stream without external PLL training controls. It does this by continually frequency locking onto the 106.25 MHz reference clock, and then phase locking onto the selected input data stream. An internal signal detection circuit monitors the presence of the input and invokes the phase detection as the data stream appears. Once bit locked, the receiver generates the high speed sampling clock for the input sampler.

INPUT SAMPLER

The INPUT SAMPLER is responsible for converting the serial input signal into a retimed bit stream. To accomplish this, it uses the high-speed serial clock generated from the RX PLL/ CLOCK RECOVERY block. This serial bit stream is sent to the FRAME DEMUX AND BYTE SYNC block.

FRAME DEMUX AND BYTE SYNC

The FRAME DEMUX AND BYTE SYNC block is responsible for restoring the 10-bit parallel data from the high-speed serial bit stream. This block is also responsible for recognizing the first seven bits of the K28.5+ positive disparity comma character (0011111xxx). When recognized, the FRAME DEMUX AND BYTE SYNC block works with the RX PLL/CLOCK RECOVERY block to select the proper parallel data edge out of the bit stream so that the next comma character starts at RX[0]. When a comma character is detected and realignment of the receive byte clock RBC[0:1] is necessary, these clocks are stretched (never slivered) to the next correct alignment position. RBC[0:1] will be aligned by the start of the next ordered set (four-byte group) after K28.5+ is detected. The start of the next ordered set will be aligned with the rising edge of RBC[1], independent of the RX_RATE pin setting. Per the Fibre Channel encoding scheme, comma characters must not be transmitted in consecutive bytes so that the receive byte clocks may maintain their proper recovered frequencies.

OUTPUT DRIVERS

The OUTPUT DRIVERS present the 10-bit parallel recovered data (RX[0:9]) properly aligned to the receive byte clock (RBC[0:1]) as shown in Figures 5a-5d and Table 1. These output drivers provide single ended SSTL_2 compatible signals.

RECEIVER LOSS OF SIGNAL

The RECEIVER LOSS OF SIGNAL block examines the peak-to-peak differential amplitude at the SI± input. When this amplitude is too small, RX_LOS is set to 1, and RX[0:9] are set to logic one (1111111111). This prevents generation of random data at the RX[0:9] pins when the serial input lines are disconnected. When the signal at SI± is a valid amplitude, RX_LOS is set to logic 0, and the output of the INPUT SELECT block is passed through.

SSTL_2 COMPATIBILITY

The HDMP-2630B works with protocol (FC-1 or MAC) devices whose VDDQ voltage is nominally 2.5 V. Note that the HDMP-2630B works with a single V_{CC} supply of 3.3 V. Nonetheless, RX[0:9] and RBC[0:1] generate output voltages that are compatible with section 4.1 of the SSTL_2 standard and are not meant to be terminated in 50 Ω. In addition, the HDMP-2630B provides a VREFR output pin which may be used at the protocol IC in order to differentially detect a high or a low on RX[0:9]. Alternatively, this voltage may be generated on the PCB using a resistor divider from VDDQ or V_{CC} while ignoring the VREFR output of the HDMP-2630B. The HDMP-2630B expects SSTL_2 compatible signals at the TX[0:9] and TBC pins. These pins are unterminated per section 4.1 of the SSTL_2 standard (Figure 11). The VREFT input pin is used by the HDMP-2630B to differentially detect a high or low on TBC and TX[0:9]. VREFT may be generated by the protocol device or on the PCB using a resistor divider from V_{DDQ} or V_{CC}.

SSTL_3 COMPATIBILITY

The HDMP-2631B works with protocol (FC-1 or MAC) devices whose VDDQ voltage is nominally 3.3V. RX[0:9] and RBC[0:1] generate output voltages that are compatible with section 3.3.1 of the SSTL_3 standard and are not meant to be terminated in 50 Ω. In addition, the HDMP-2631B provides a VREFR output pin which may be used at the protocol IC in order to differentially detect a high or a low on RX[0:9]. Alternatively, this voltage may be generated on the PCB using a resistor divider from VDDQ or V_{CC} while ignoring the VREFR output of the HDMP-2631B. The HDMP-2631B expects SSTL_3 compatible signals at the TX[0:9] and TBC pins. These pins are unterminated per section 3.3.1 of the SSTL_3 standard (Figure 11). The VREFT input pin is used by the HDMP-2631B to differentially detect a high or low on TBC and TX[0:9]. VREFT may be generated by the protocol device or on the PCB using a resistor divider from VDDQ or V_{CC}.

MULTI-RATE OPERATION

The HDMP-2630B/2631B provide hooks for initializing multi-rate links. A possible algorithm operates as follows. In a point to point link, each node sets its TX_RATE input pin high to transmit at the highest possible data rate. At the same time, each node tries different values of RX_RATE to see at which data rate intelligible data is received. Once this data rate is found, TX_RATE is set to enable this rate. For example, suppose a node that is capable of operating at 1.0625 GBd and 2.125 GBd rates is establishing a link with a node that is capable of only 2.125 GBd. Both nodes will start emitting at 2.125 GBd because this is their highest rate. The first node will try receiving at 1.0625 GBd rate. It will not succeed and will therefore try 2.125 GBd reception, which will succeed. The second node is set to 2.125 GBd and has been receiving correct data. These two nodes will settle to 2.125 GBd.

If the second node in the example above operated at 1.0625 GBd only, then the first node would see intelligible 1.0625 GBd data and set its TX_RATE = 0, at which time the second node would also start seeing intelligible data. These nodes would settle to 1.0625 GBd. If both nodes are 1.0625/2.125 GBd capable, then they will settle to 2.125 GBd. With this algorithm, nodes need not have a common lowest common denominator data rate to interoperate.

HDMP-2630B/2631B Transmitter Section Timing Characteristics

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{TXCT}	TX[0:9] Input Data and TBC Clock Transition Range (TX_RATE = 1)	ps			1880
t_{TXCV}	TX[0:9] Input Data and TBC Clock Valid Time (TX_RATE = 1)	ps	2820		
$t_{TXSETUP}$	TX[0:9] Setup Time to Falling Edge of TBC (TX_RATE = 0)	ps	1400		
t_{TXHOLD}	TX[0:9] Hold Time from Falling Edge of TBC (TX_RATE = 0)	ps	1400		
t_txlat[1]	Transmitter Latency	ns bits		0.8+ 8.5	

Note:

1. The transmitter latency, as shown in Figure 4, is defined as the time between the leading edge of a parallel data word and the leading edge of the first transmitted serial output bit of that data word.

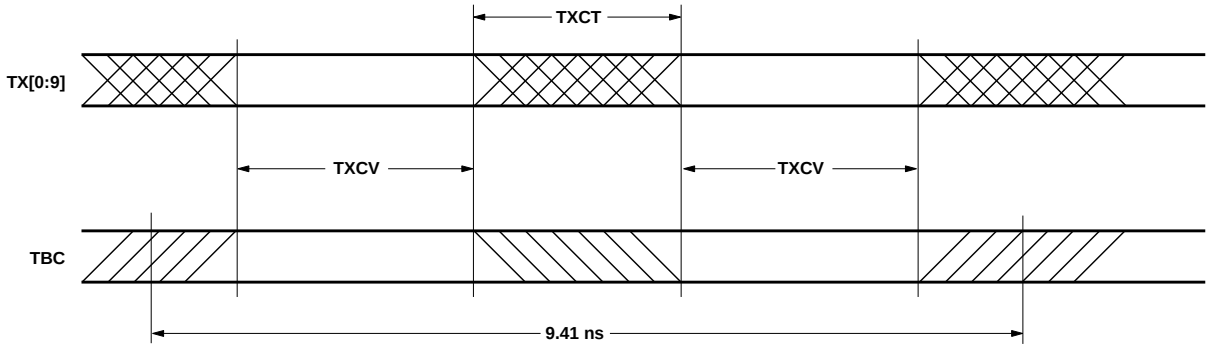


Figure 3a. Parallel transmitter section timing. TX_RATE = 1.

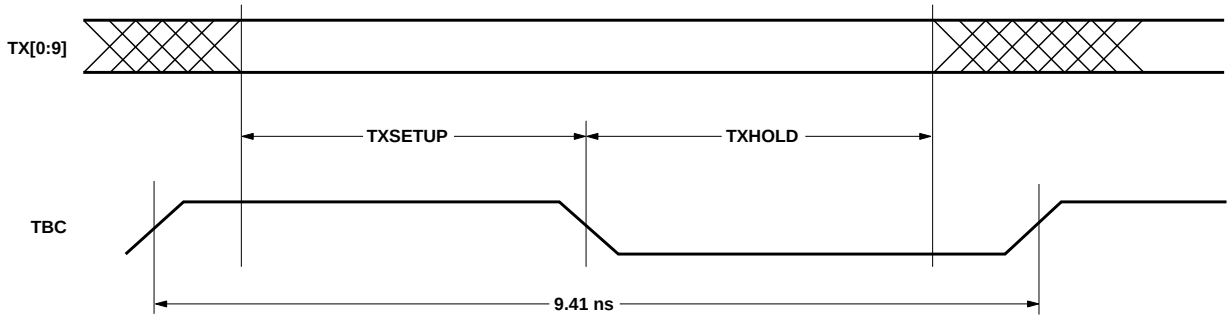


Figure 3b. Parallel transmitter section timing. TX_RATE = 0.

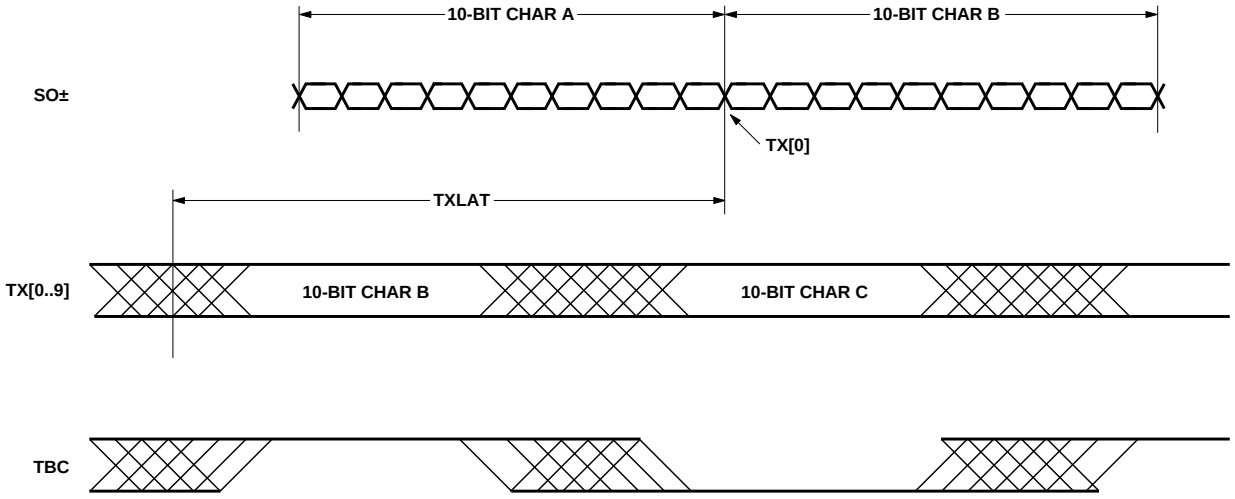


Figure 4. Transmitter latency. TX[0] is first bit on SO±.

HDMP-2630B/2631B Receiver Section Timing Characteristics

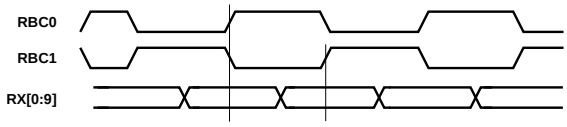
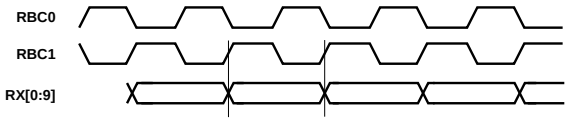
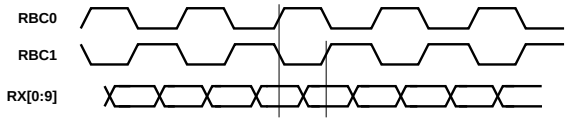
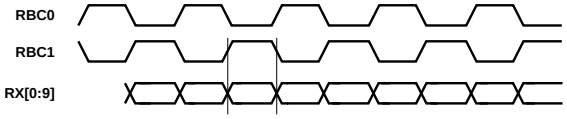
T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
f_lock	Frequency Lock at Powerup with REFCLK Active	µs			500
B_sync[1,2]	Bit Sync Time	bits		200	2500
t_rxlat[3]	Receiver Latency	ns bits		13.5 +2.5	

Notes:

1. This is the recovery time for input phase jumps, per the Fibre Channel Specification X3.230-1994 FC-PH Standard, Sec 5.3.
2. Tested using C_{PLL} = 0.1 µF.
3. The receiver latency, as shown in Figure 6, is defined as the time between the leading edge of the first received serial bit of a parallel data word and the leading edge of the corresponding parallel output word.

Table 1. HDMP-2630B/2631B RX, RBC[0:1]
Timing Dependence on RX_RATE and RBC_SYNC.

Input Settings			Resulting Behaviors		
Case	**RX_RATE**	**RBC_SYNC**	**SI Rate (GBd)**	**RBC Rate (MHz)**	**Timing Diagrams for RBC0, RBC1, RX[0:9]**
A	0	0	1.0625	53.125	
B	0	1	1.0625	106.25	
C	1	0	2.125	106.25	
D	1	1	2.125	106.25	

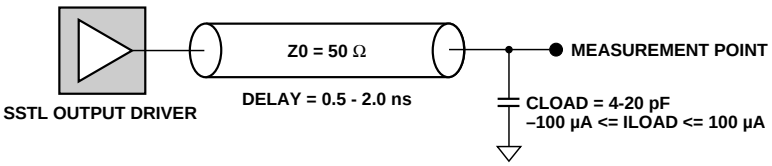


Figure 5. Test conditions for SSTL_2 and SSTL_3 output drivers.

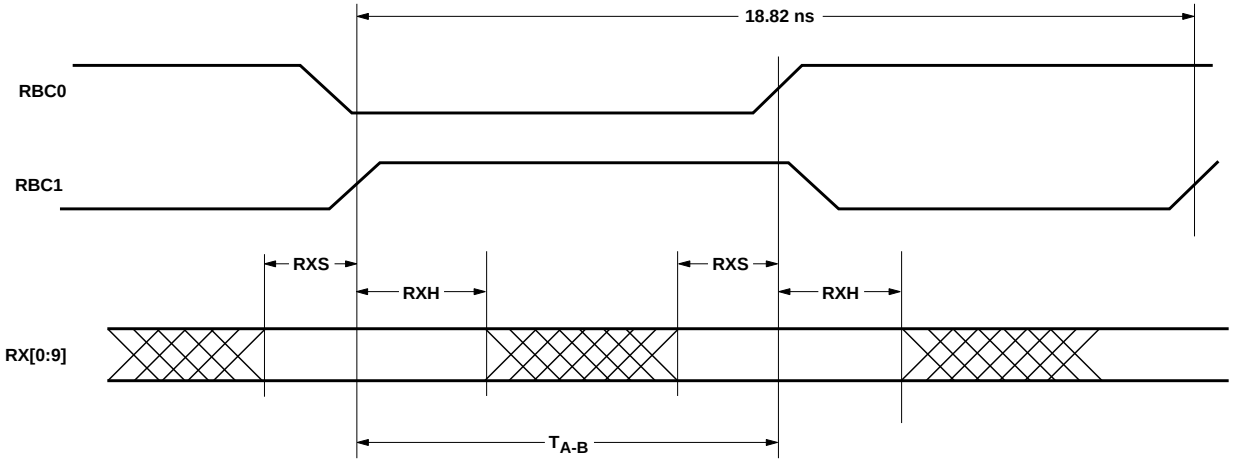


Figure 5a. Receiver section timing – case A.

Case A of Table 1. (RX_RATE = 0, RBC_SYNC = 0)
T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{RXS}	RX[0:9] Setup Time to RBC1 or RBC0 (Data Valid Before)	ps	2700		
t_{RXH}	RX[0:9] Hold Time from RBC1 or RBC0 (Data Valid After)	ps	1500		
t_{A-B}	RBC1 Rising Edge to RBC0 Rising Edge Skew	ns	8.9		9.9
t_{DUTY}	RBC[0:1] Duty Cycle	%	40		60

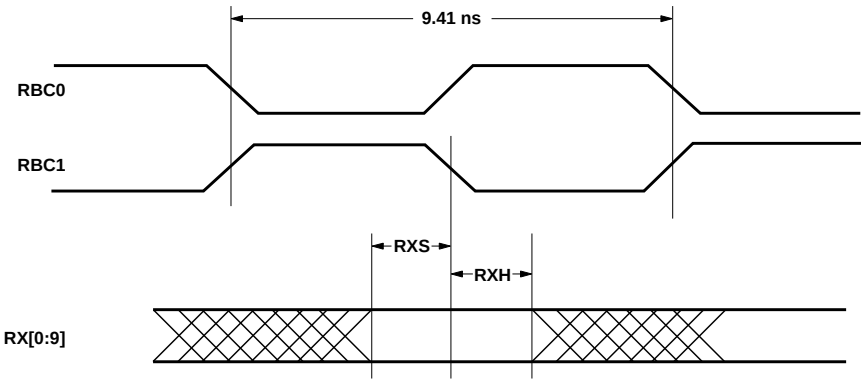


Figure 5b. Receiver section timing – case B.

Case B of Table 1. (RX_RATE = 0, RBC_SYNC = 1)
T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{RXS}	RX[0:9] Setup Time to RBC1 or RBC0 (Data Valid Before)	ps	1700		
t_{RXH}	RX[0:9] Hold Time from RBC1 or RBC0 (Data Valid After)	ps	1700		

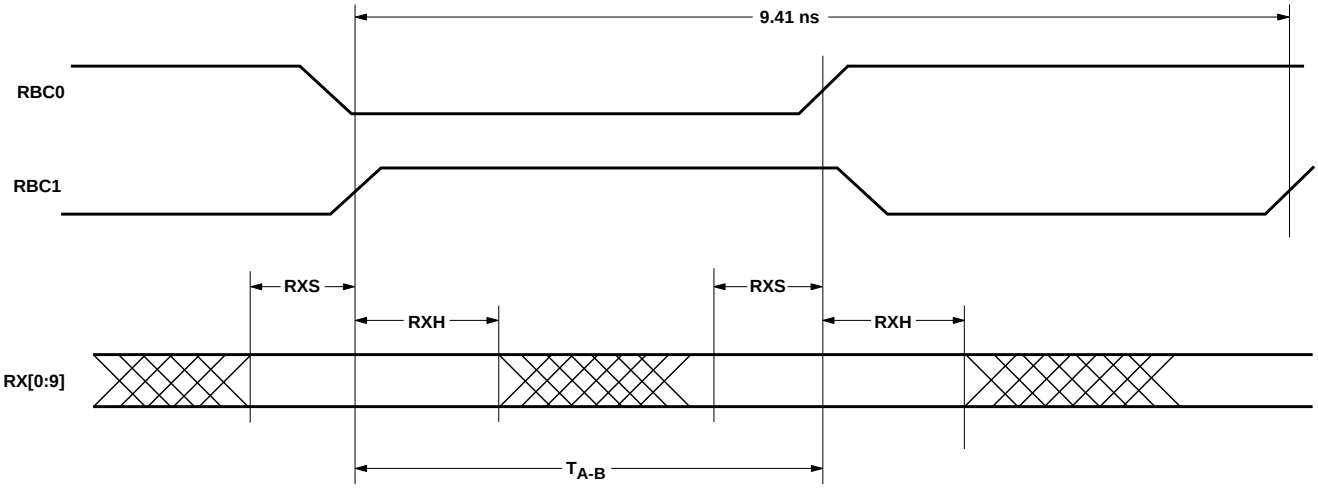


Figure 5c. Receiver section timing – case C.

Case C of Table 1. (RX_RATE = 1, RBC_SYNC = 0)
T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{RXS}	RX[0:9] Setup Time to RBC1 or RBC0 (Data Valid Before), HDMP-2630B RX[0:9] Setup Time to RBC1 or RBC0 (Data Valid Before), HDMP-2631B	ps	1400 1200		
t_{RXH}	RX[0:9] Hold Time from RBC1 or RBC0 (Data Valid After), HDMP-2630B RX[0:9] Hold Time from RBC1 or RBC0 (Data Valid After), HDMP-2631B	ps	1400 1200		
t_{A-B}	RBC1 Rising Edge to RBC0 Rising Edge Skew	ns	4.5		4.9
t_{DUTY}	RBC[0:1] Duty Cycle	%	40		60

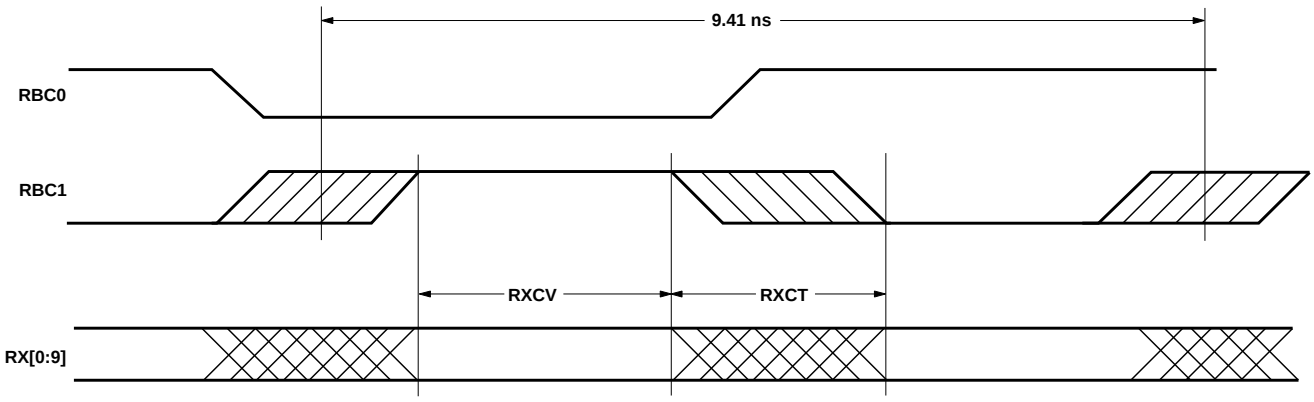


Figure 5d. Receiver section timing – case D.

Case D of Table 1. (RX_RATE = 1, RBC_SYNC = 1)
T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{RXCT}	RX[0:9] Output Data and RBC Clock Transition Range	ps			1700
t_{RXCV}	RX[0:9] Output Data and RBC Clock Valid Time	ps	3000		

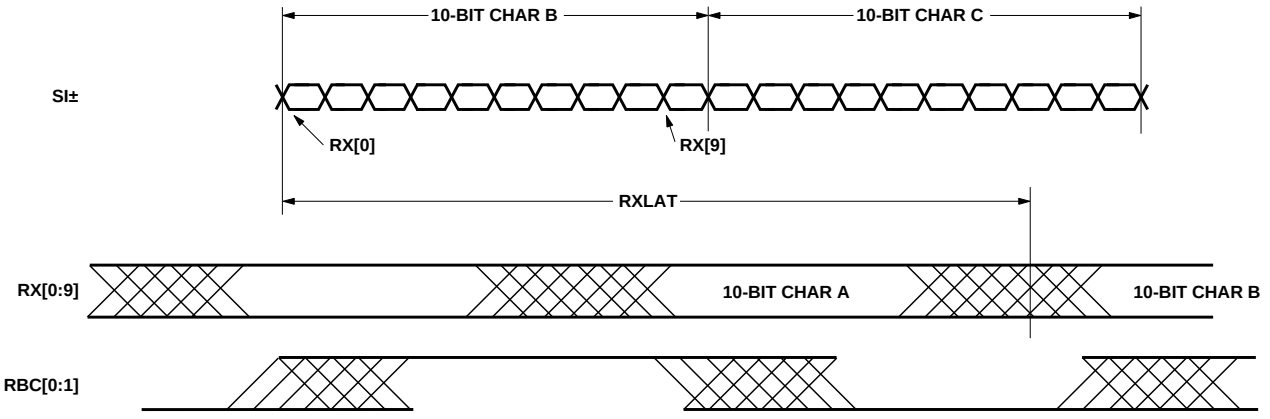


Figure 6. Receiver latency. First bit on SI± drives RX[0].

HDMP-2630B/2631B Absolute Maximum Ratings

Sustained operation at or beyond any of these conditions may result in long-term reliability degradation or permanent damage, and is not recommended.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.5	4.0
T_{stg}	Storage Temperature	°C	–65	150
T_C	Case Temperature	°C	0	95
T_j	Junction Temperature	°C	0	125
$V_{IN,PECL}$	LVPECL Input Voltage	V	–0.5	V_{CC} + 0.5[1]
$V_{IN,SSTL}$	SSTL_2 or SSTL_3 Input Voltage	V	–0.5	V_{CC} + 0.5[1]

Note:

1. Must remain less than or equal to absolute maximum V_{CC} voltage of 4.0 V.

HDMP-2630B/2631B Guaranteed Operating Rates

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Parallel Clock Rate (MHz)		Serial Baud Rate (GBd)		Serial Baud Rate (GBd)	
Min.	Max.	Min.	Max.	Min.	Max.
106.20	106.30	1.062	1.063	2.124	2.126

HDMP-2630B/2631B Transceiver REFCLK and TBC Requirements

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
f	Nominal Frequency	MHz		106.25	
F_{tol}	Frequency Tolerance	ppm	–100		100
Symm	Symmetry (Duty Cycle)	%	40		60

HDMP-2630B/2631B DC Electrical Specifications

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$I_{CC, TRx}$[1]	Transceiver Supply Current (total of all supplies)	mA		580	750
$P_{D, TRx}$[1]	Transceiver Total Power Dissipation	mW		1900	2600

Note:

1. Measurement Conditions: Tested sending 2.125 GBd 2^7-1 PRBS sequence from a serial BERT with SO± outputs differentially terminated using a 150 Ω resistor.

HDMP-2630B/2631B LVPECL DC Electrical Specifications for REFCLK[0:1]

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$V_{IH,PECL}$	LVPECL Input High Voltage Level	V	2.10		2.60
$V_{IL,PECL}$	LVPECL Input Low Voltage Level	V	1.30		1.80

HDMP-2630B/2631B LVTTL DC Electrical Specifications for REFCLK[1]

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$V_{IH,LVTTL}$	LVTTL Input High Voltage Level	V	2.00		
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Level	V			0.80

SSTL_2 I/O Parameters

HDMP-2630B Recommended DC Operating Conditions and DC Electrical Characteristics

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V, VDDQ = 2.30 V to 2.70 V. VDDQ is the FC-1/MAC device I/O supply voltage. SSTL-2 inputs can receive LVTTL signals successfully. SSTL-2 outputs do not output LVTTL compliant levels.

Symbol	Parameter	Units	Min.	Typ.	Max.
VREFT	SSTL_2 Input Reference Voltage	V	1.15	1.25	1.35
V_{IH}	Input High Voltage	V	VREFT +0.35		VDDQ +0.30
V_{IL}	Input Low Voltage	V	–0.30		VREFT –0.35
VREFR	SSTL_2 Output Reference Voltage	V	1.15	1.25	1.35
V_{OH}	Output High Voltage	V	VREFR +0.38		VDDQ
V_{OL}	Output Low Voltage	V	GND		VREFR –0.38

SSTL_3 I/O Parameters

HDMP-2631B Recommended DC Operating Conditions and DC Electrical Characteristics

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V, VDDQ = 3.00 V to 3.60 V. VDDQ is the FC-1/MAC device I/O supply voltage. SSTL-3 inputs can receive LVTTL signals successfully. SSTL-3 outputs do not output LVTTL compliant levels.

Symbol	Parameter	Units	Min.	Typ.	Max.
VREFT	SSTL_3 Input Reference Voltage	V	1.30	1.50	1.70
V_{IH}	Input High Voltage	V	VREFT +0.40		VDDQ +0.30
V_{IL}	Input Low Voltage	V	–0.30		VREFT –0.40
VREFR	SSTL_3 Output Reference Voltage	V	1.30	1.50	1.70
V_{OH}	Output High Voltage	V	VREFR +0.43		VDDQ
V_{OL}	Output Low Voltage	V	GND		VREFR –0.43

HDMP-2630B/2631B AC Electrical Specifications

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
$t_{r,REFCLK}$	REFCLK[0:1] PECL Input Rise Time, $V_{IL,PECL}$ to $V_{IH,PECL}$	ns			1.5
$t_{f,REFCLK}$	REFCLK[0:1] PECL Input Fall Time, $V_{IH,PECL}$ to $V_{IL,PECL}$	ns			1.5
$t_{rd,\ HS\_OUT}$	HS_OUT Differential Rise Time, 20% - 80%	ps		160	
$t_{fd,\ HS\_OUT}$	HS_OUT Differential Fall Time, 20% - 80%	ps		160	
$t_{r,SSTL}$	SSTL Input Rise Time, $V_{IL,SSTL}$ to $V_{IH,SSTL}$	ns			1.5
$t_{f,SSTL}$	SSTL Input Fall Time, $V_{IH,SSTL}$ to $V_{IL,SSTL}$	ns			1.5
V_{IP,HS_IN}	HS_IN Input Peak-To-Peak Differential Voltage	mV	200		2000
V_{OP,HS_OUT}[1]	HS_OUT Output Pk-Pk Diff. Voltage (Z0 = 50 Ω, Fig.9)	mV	800	1050	2000
V_{OP,HS_OUT}[1]	HS_OUT Output Pk-Pk Diff. Voltage (Z0 = 75 Ω, Fig.9)	mV	1100	1400	2000

Note:

1. Output Differential Voltage defined as (SO+ – SO–). Measurement made with Tx pre-emphasis off (EQAMP tied to V_{CC} with a 100 Ω resistor).

HDMP-2630B/2631B Transmitter Section Output Jitter Characteristics

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Typ.
RJ[1]	Random Jitter at SO± (1 σ deviation of the 50% crossing point)	ps	6.2
DJ[2]	Deterministic Jitter at SO± (peak-to-peak), K28.5+/K28.5– Pattern	ps	22
DJ	Deterministic Jitter at SO± (peak-to-peak), CRPAT[3] Pattern	ps	31

Notes:

1. Defined by Fibre Channel Specification X3.230-1994 FC-PH, Annex A, Section A.4.4 (oscilloscope method) and tested using the setup shown in Figure 8b.
2. Defined by Fibre Channel Specification X3.230-1994 FC-PH, Annex A, Section A.4.3 and tested using the setup shown in Figure 8a.
3. Defined in the Fibre Channel Technical Report "Methodologies for Jitter Specification," Annex B, and tested using the setup shown in Figure 8a.

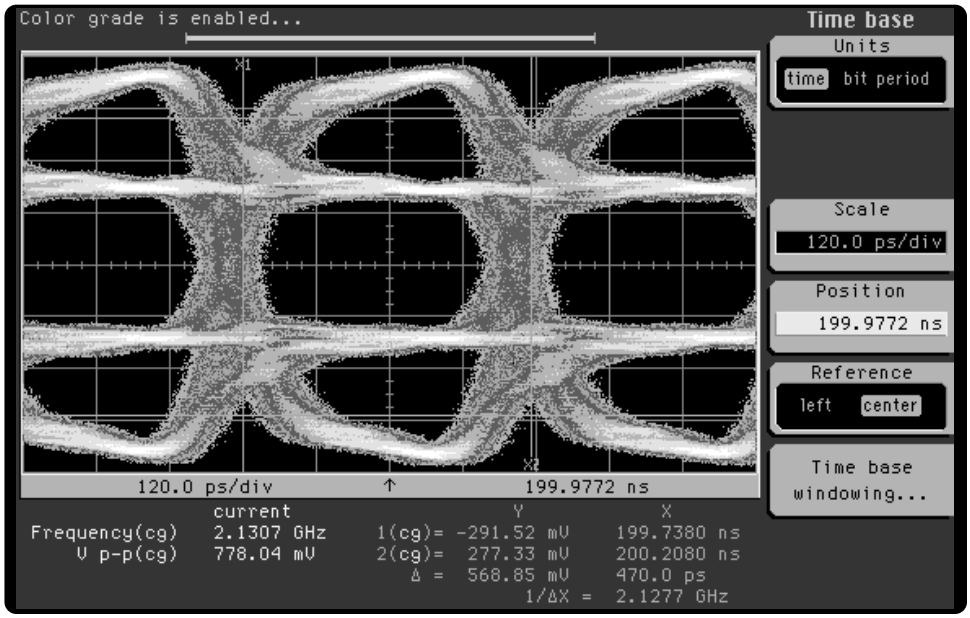


Figure 7a. Serial output eye diagram with nominal Tx pre-emphasis.

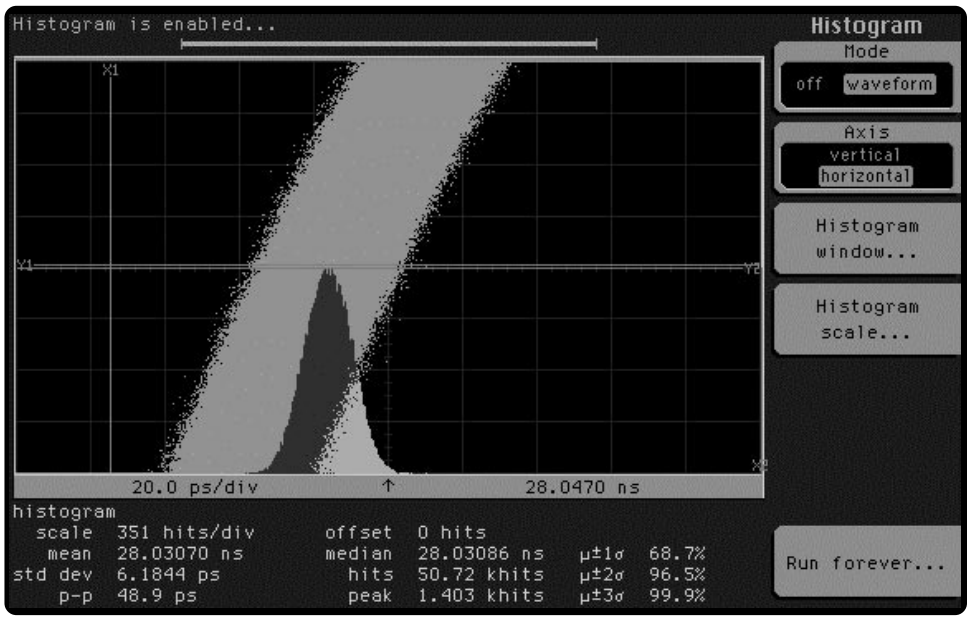


Figure 7b. Serial output random jitter with Tx pre-emphasis off.

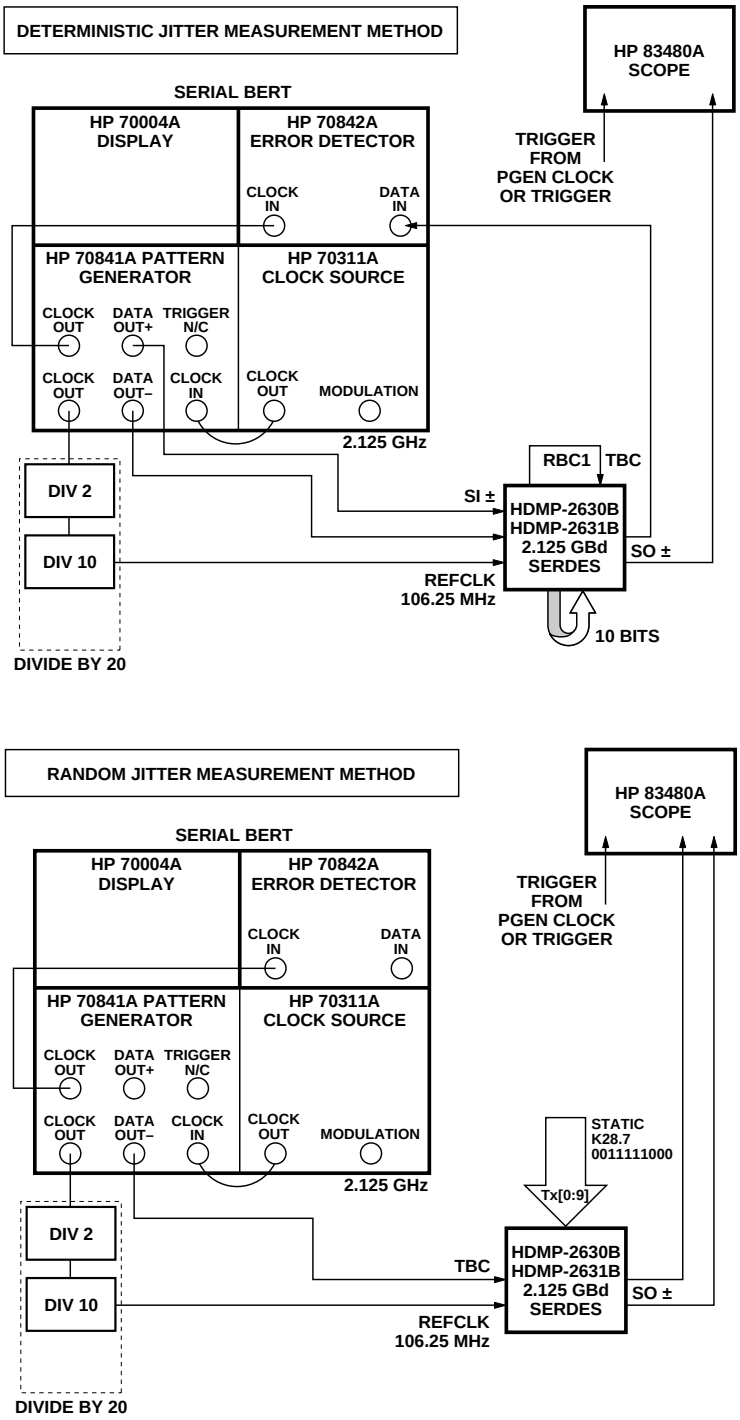


Figure 8a-b. Transmitter deterministic and random jitter measurement method.

HDMP-2630B/2631B Thermal Characteristics

T_A = 0°C to T_C = 85°C, V_{CC} = 3.15 V to 3.45 V

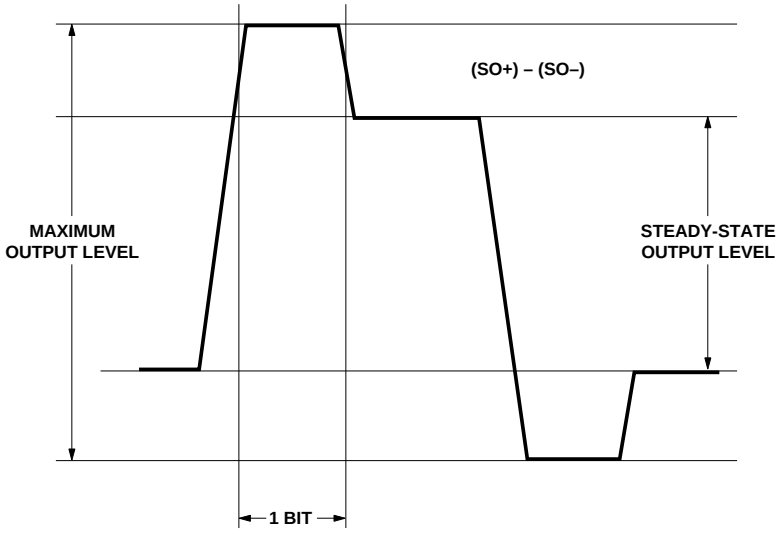
Symbol	Parameter	Units	Typ.
Θ_{jc}[1]	Thermal Resistance, Junction to Case	°C/W	9.3

Note:

1. Based on independent package testing by Agilent. Θ_{ja} for these devices is 38°C/W for the HDMP-2630B and HDMP-2631B. Θ_{ja} is measured on a standard 3x3" FR4 PCB in a still air environment. To determine the actual junction temperature in a given application, use the following equation:
   $T_j = T_c + (\Theta_{jc} \times P_D)$, where Tc is the case temperature measured on the top center of the package and P_D is the power being dissipated.

HDMP-2630B/2631B Pin Input Capacitance

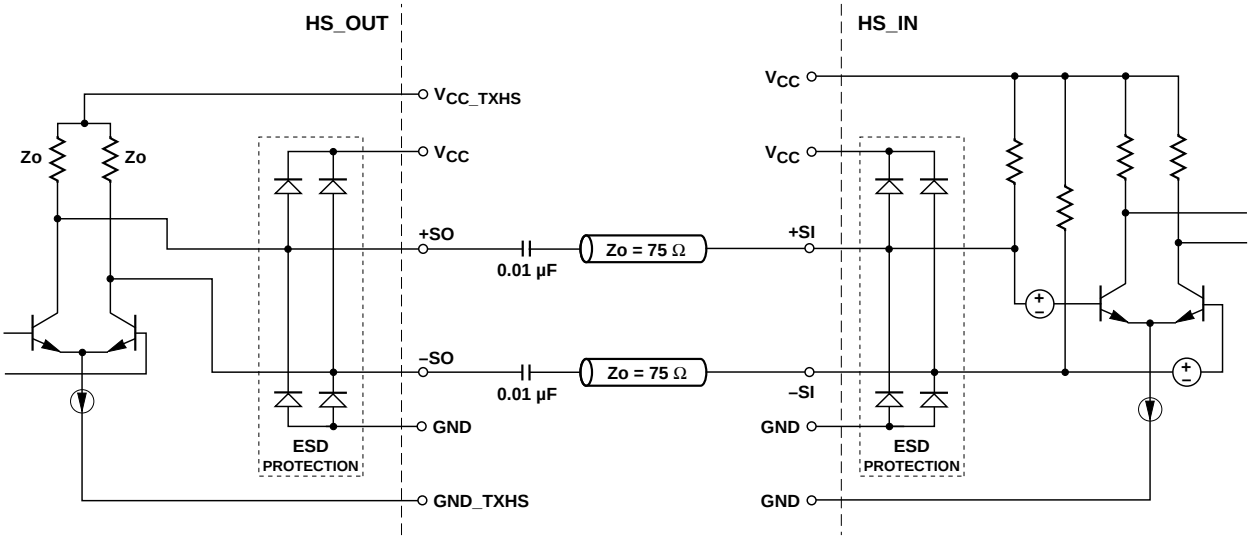
Symbol	Parameter	Units	Typ.
C_{INPUT}	Input Capacitance on SSTL input pins	pF	1.6



STEADY-STATE OUTPUT LEVEL	MAXIMUM OUTPUT LEVEL	EQAMP SETTING
1.11 V	1.11 V	100 Ω to V_{CC} (NO PRE-EMPHASIS)
820 mV	1.28 V	FLOATING (NOMINAL PRE-EMPHASIS)
570 mV	1.44 V	SHORTENED TO GND (MAXIMUM PRE-EMPHASIS)

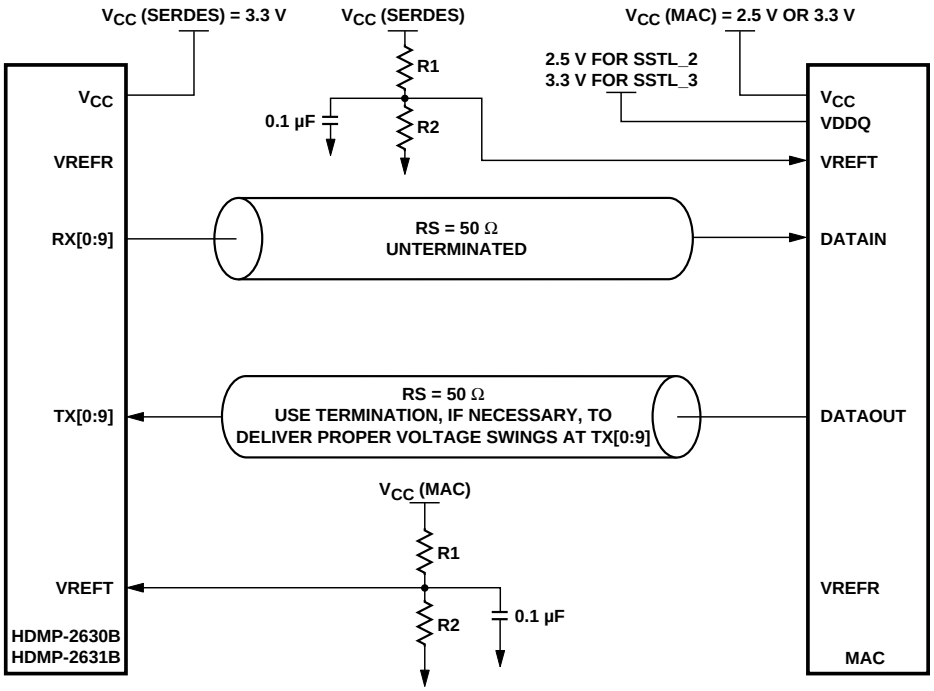
ALL VALUES MEASURED IN A 50 Ω ENVIRONMENT WITH V_{CC} = 3.3 V AND T_A = 25°C.

Figure 9. Tx pre-emphasis control using EQAMP pin.



NOTE:
HS_IN INPUTS SHOULD NEVER BE CONNECTED TO GROUND AS PERMANENT DAMAGE TO THE DEVICE MAY RESULT.
Z0 = 50 Ω MAY ALSO BE USED.

Figure 10. HS_OUT and HS_IN simplified circuit schematic for HDMP-2630B/1B.



NOTE: VREFR ON EACH DEVICE MAY BE USED TO DRIVE VREFT ON THE OTHER DEVICE INSTEAD OF USING THE CONFIGURATION ABOVE. VREFR SHOULD BE BYPASSED WITH 0.1 µF IN THIS CASE. IF USED, R1 + R2 SHOULD BE 500-1000 Ω. 1% RESISTORS SHOULD BE USED FOR R1 AND R2. WHEN USING THE CONFIGURATION ABOVE, VREFT TO THE MAC DEVICE SHOULD BE SET TO 1.25 V NOMINAL (HDMP-2630B) AND 1.5 V NOMINAL (HDMP-2631B). USING THESE VALUES CENTERS VREFR RELATIVE TO THE RX[0:9] OUTPUT SWINGS PROVIDED BY THE HDMP-2630B AND HDMP-2631B.

Figure 11. I-SSTL2/I-SSTL3 and O-SSTL2/O_SSTL3 simplified circuit schematic.

I/O Type Definitions

I/O Type	Definition
I-SSTL2 or I-SSTL_3	Input SSTL_2 or SSTL_3. These inputs will receive LVTTL-compliant signals successfully.
O-SSTL2 or O-SSTL_3	Output SSTL_2 or SSTL_3. These outputs will not produce LVTTL-compliant signals.
HS_OUT	High Speed Output, ECL Compatible
HS_IN	High Speed Input
C	External Circuit Node
S	Power Supply or Ground

Table 2. Pin Definitions for HDMP-2630B/2631B

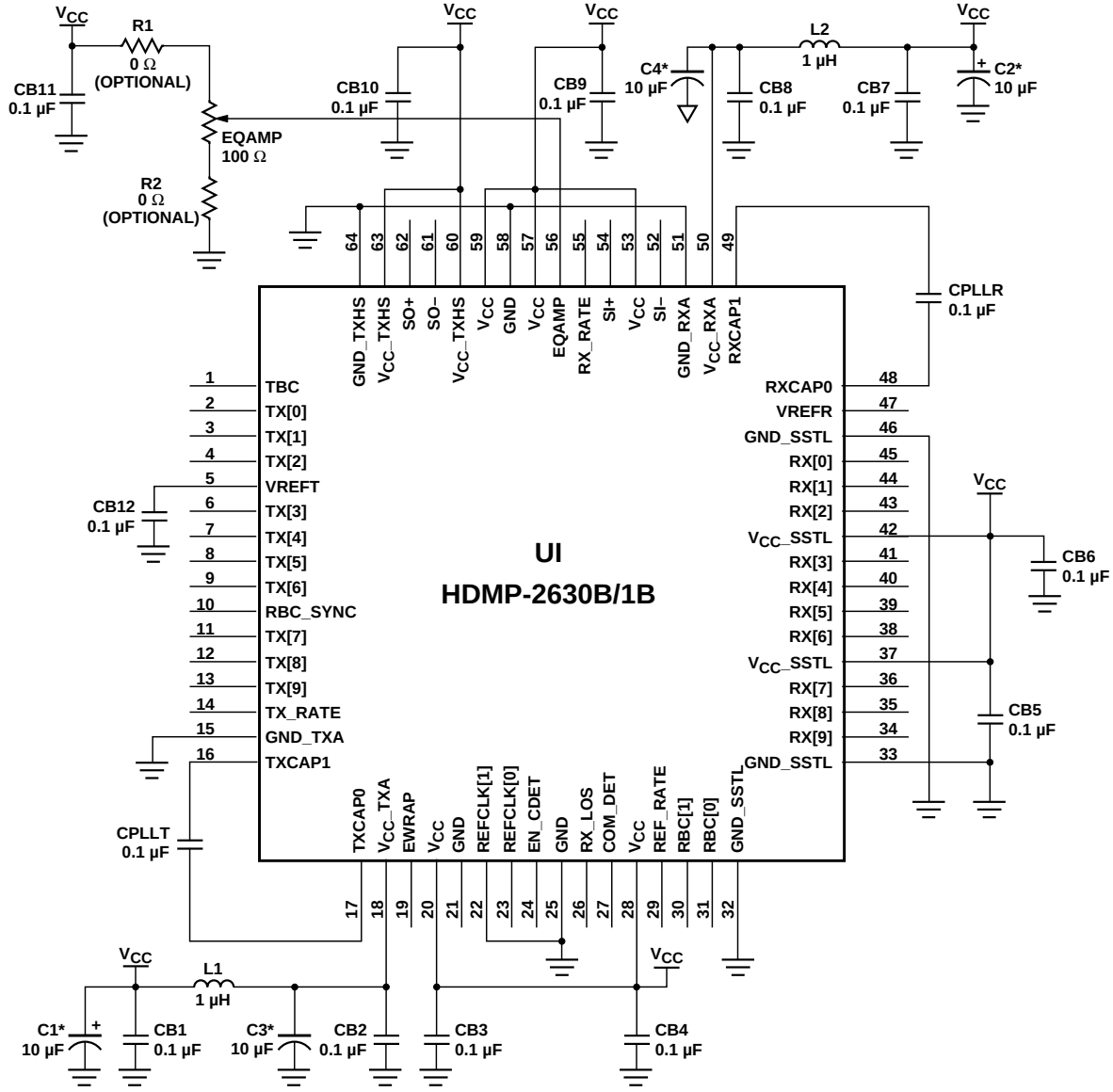
Name	Pin	Type	Signal
EQAMP	56	C	**Output Equalization Amplitude Control:** Controls the relative amount of equalization on the high-speed serial data outputs. Equalization is disabled by connecting a 100 Ω resistor from EQAMP to V_{CC}. The amount of equalization can be increased by either increasing the value (above 100 Ω) of a resistor connected from EQAMP to V_{CC}, or decreasing the value of a resistor connected from EQAMP to GND. Maximum equalization is obtained by connecting EQAMP directly to GND. See Figure 9.
EWRAP	19	I-SSTL2	**Loop Enable:** When high, the high speed serial output data is internally connected directly to the receiver circuit, bypassing the high-speed input and output buffers. The external high-speed data outputs SO± are set high and SI± inputs are ignored.
EN_CDET	24	I-SSTL2	**Comma Detect Enable:** When high, enables detection of comma character.
COM_DET	27	O-SSTL2	**Comma Detect Indicator:** When high, indicates that a comma character of positive disparity (0011111xxx) has been detected on the high speed serial input line.
TX_RATE falling to	14	I-SSTL2	**Transmit Rate Set:** If set to low, the HDMP-2630B/2631B read TX[0:9] data on the edge of TBC and serializes it. This corresponds to a 1.0625 GBd serial stream. If set high, the HDMP-2630B/2631B read TX[0:9] data between both edges of TBC and serializes it. This corresponds to a 2.125 GBd serial stream.
RX_RATE If and	55	I-SSTL2	**Receive Rate Set:** If set to low, the HDMP-2630B/2631B sample the incoming serial stream at 1.0625 GBd and drives it on the RX[0:9] lines with the rising edge of RBC1. set to high, the HDMP-2630B/2631B sample the incoming serial stream at 2.125 GBd drives it on the RX[0:9] lines with the rising edges of RBC1 and RBC0. (Table 1.)
REF_RATE	29	I-SSTL2	**RefClk Rate:** Set this pin to low when using full rate (106.25 MHz) REFCLK[0:1] inputs. Set this pin high when using half rate (53.125 MHz) REFCLK[0:1] inputs. REF_RATE applies for both differential PECL or LVTTL reference clock inputs.
RBC_SYNC	10	I-SSTL2	**Receive Byte Clock Synchronization Control:** When RBC_SYNC=1, RX[0:9] data has the same relation to RBC[0:1] as TX[0:9] data has to TBC. ASICs designed using this mode have the option of avoiding a SERDES driven serial link and communicating directly on parallel lines, for short distances.
RX_LOS	26	O-SSTL2	**Loss of Signal at the Receiver Detect:** Indicates a loss of signal on the high-speed differential inputs, SI±, as in the case where the transmission cable becomes disconnected. If SI± >= 200mV peak-to-peak differential, RX_LOS = logic 0. If SI± < 200mV and SI± > 75mV, RX_LOS = undefined. If SI± =< 75mV, RX_LOS = logic 1, RX[0:9]=1111111111.
SO+ SO–	62 61	HS_OUT	**Serial Data Outputs:** High speed outputs. These lines are active when not in parallel loop mode (EWRAP=0). When EWRAP is high, these outputs are held static at logic 1.
SI+ SI–	54 52	HS_IN	**Serial Data Inputs:** High speed inputs. Serial data is accepted from SI± inputs when EWRAP is low.
TBC	01	I-SSTL2	**Transmit Clock:** Both edges of this input are used to determine the sampling window for transmit parallel data.
REFCLK[1] REFCLK[0]	22 23	I-PECL or I-LVTTL I-PECL	**Reference Clock:** A 106.25 MHz (REF_RATE = 0) or 53.125 MHz (REF_RATE = 1) clock supplied by the host system. It serves as the reference clock for the receive portion of the transceiver. These pins may be driven by a differential PECL clock source or a single ended LVTTL clock source. In the LVTTL case, REFCLK[1] is to be driven and REFCLK[0] is to be bypassed to GND via a 0.1 µF capacitor.
RBC[1] RBC[0]	30 31	O-SSTL2	**Receive Byte Clocks:** The receiver section recovers two receive byte clocks. These two clocks are 180 degrees out of phase. See Table 1 for timing relationships.

Table 2. Pin Definitions for HDMP-2630B/2631B, continued

Name	Pin	Type	Signal
TX[0] TX[1] TX[2] TX[3] TX[4] TX[5] TX[6] TX[7] TX[8] TX[9]	02 03 04 06 07 08 09 11 12 13	I-SSTL2	**Data Inputs:** One 10-bit, encoded character to the SO± serial outputs. TX[0] is the first bit transmitted. TX[0] is the least significant bit.
RX[0] RX[2] RX[3] RX[4] RX[5] RX[6] RX[7] RX[8] RX[9]	45 43 41 40 39 38 36 35 34	O-SSTL2	**Data Outputs:** One 10-bit encoded character from one of the SI± serial inputs. RX[0] is the first bit received. When RX_LOS =1, there is a loss of input signal at SI±, and these outputs are held static at logic 1. Refer to RX_LOS pin definition for more details.
TXCAP0 TXCAP1	17 16	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal transmit PLL must be connected across the TXCAP0 and TXCAP1 pins. (typical value is 0.1 μF)
RXCAP0 RXCAP1	48 49	C	**Loop Filter Capacitor:** A loop filter capacitor for the internal receive PLL must be connected across the RXCAP0 and RXCAP1 pins. (typical value is 0.1 μF)
V_{CC}	20 28 57 59 53	S	**Logic Power Supply:** Normally 3.3 volts. Used for internal PECL logic.
V_{CC}_TXA	18	S	**Analog Power Supply**: Normally 3.3 volts. Used to provide a clean supply line for transmit PLL and high speed analog cells.
V_{CC}_RXA	50	S	**Analog Power Supply:** Normally 3.3 volts. Used to provide a clean supply line for receive PLL and high speed analog cells.
V_{CC}_TXHS	60 63	S	**High Speed Supply:** Normally 3.3 volts. Used only for the high speed transmit cell (HS_OUT). Noise on this line should be minimized for best operation.
VREFT	05	S	**Voltage Reference Input:** Used with I-SSTL2 and I-SSTL3 inputs to the HDMP-2630B/2631B. (Figure 11.)
VREFR	47	S	**Voltage Reference Output:** Used with O-SSTL2 and O-SSTL3 outputs from the HDMP-2630B/2631B. (Figure 11.)
V_{CC}_SSTL	37 42	S	**SSTL I/O Supply Voltage** for SSTL_2 and SSTL_3 I/O. Normally 3.3 V. All necessary voltages for SSTL_2 and SSTL_3 operation are internally generated.
GND	21 25 58	S	**Logic Ground:** Normally 0 volts. This ground is used for internal PECL logic.

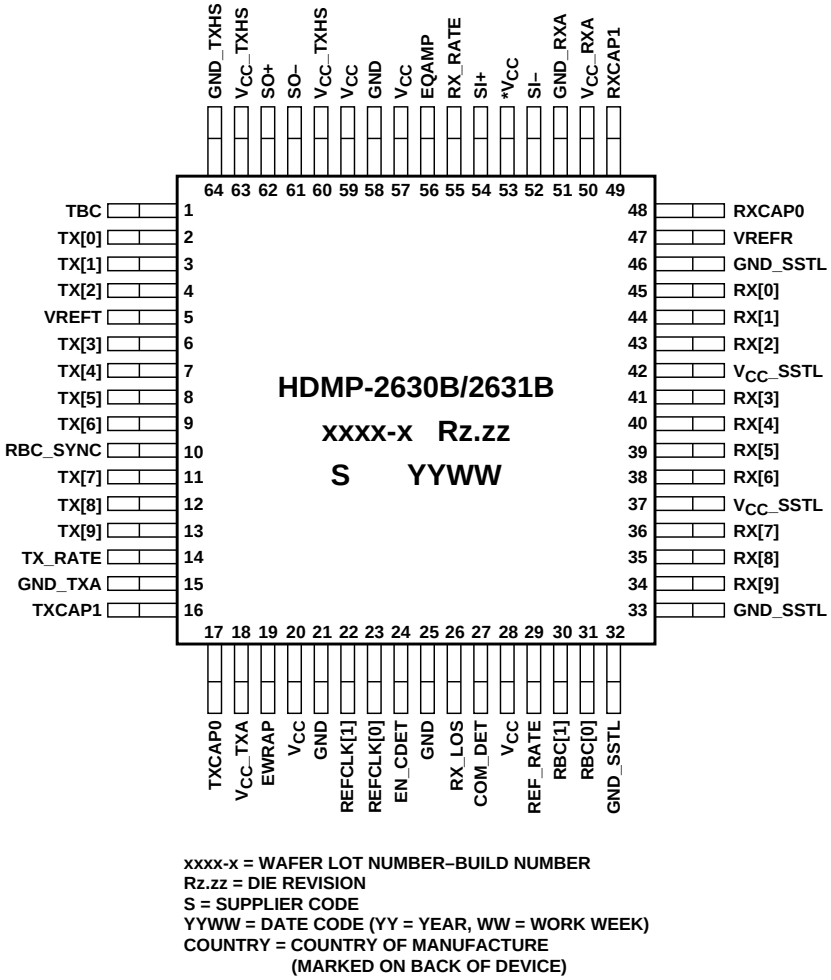
Table 2. Pin Definitions for HDMP-2630B/2631B, continued

Name	Pin	Type	Signal
GND_TXA	15	S	**Analog Ground:** Normally 0 volts. Used to provide a clean ground plane for the PLL and high-speed analog cells.
GND_RXA	51	S	**Analog Ground:** Normally 0 volts. Used to provide a clean ground plane for the receiver PLL and high-speed analog cells.
GND_TXHS	64	S	**High Speed Ground:** Normally 0 volts. Used for HS_IN cell.
GND_SSTL	32 33 46	S	**SSTL Ground:** Normally 0 volts. Used for SSTL_2 and SSTL_3 I/O.



NOTES:
1. C1*-C4* FOR LOW-FREQUENCY BYPASS.
2. VENKEL PART NUMBER C0603X7R160-104KNE, OR SIMILAR, CAN BE USED FOR 0.1 µF CAPACITORS.
3. TDK P/N NL322522T-1R0J, OR SIMILAR, CAN BE USED FOR 1 µH INDUCTORS.

Figure 12. Recommended power supply filtering arrangement.



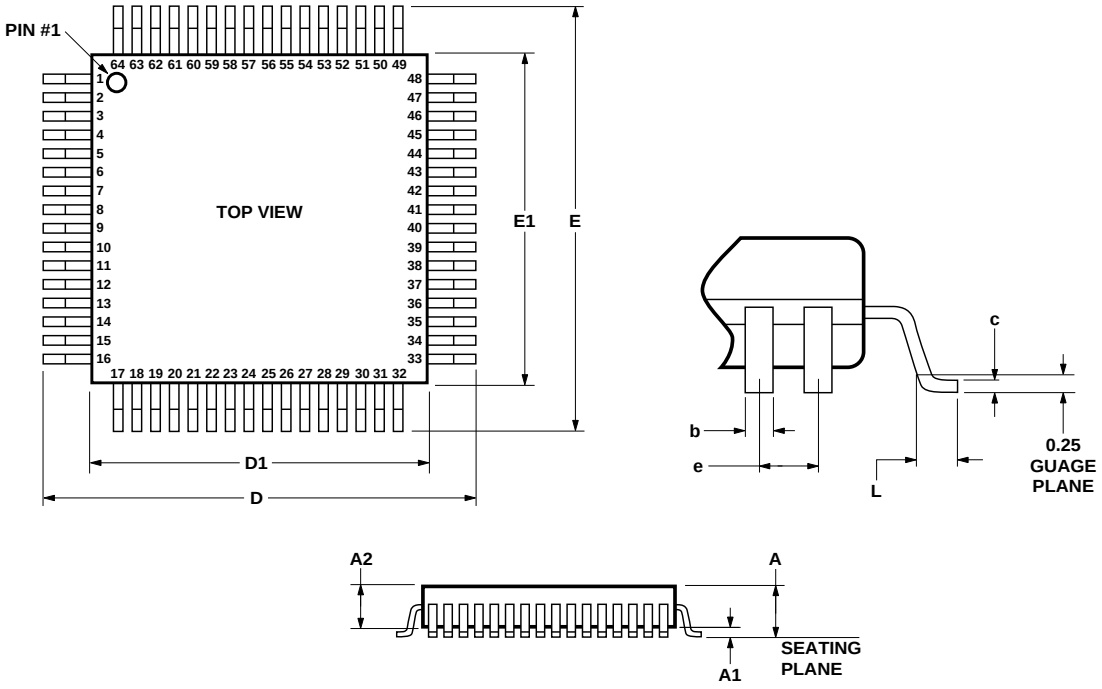
xxxx-x = WAFER LOT NUMBER–BUILD NUMBER
Rz.zz = DIE REVISION
S = SUPPLIER CODE
YYWW = DATE CODE (YY = YEAR, WW = WORK WEEK)
COUNTRY = COUNTRY OF MANUFACTURE
(MARKED ON BACK OF DEVICE)

Figure 13. HDMP-2630B/2631B package layout and marking, top view.

Package Information

Item	Details
Package Material	Metric Metal QFP
Lead Finish Material	85% Tin, 15% Lead
Lead Finish Thickness	200-800 micro-inches
Lead Skew	0.20 mm max.
Lead Coplanarity (Seating Plane Method)	0.08 mm max.

Mechanical Dimensions of HDMP-2630B/2631B



DIMENSIONAL PARAMETER (MILLIMETERS)	A	A1	A2	D/E	D1/E1	L	b	c	e
VALUE	2.35	0.25	2.00	17.20	13.80	0.88	0.37	0.20	0.80
TOLERANCE	MAX.	MAX.	± 0.10	± 0.25	± 0.05	± 0.15	+ 0.08/ – 0.03	MAX.	BASIC

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