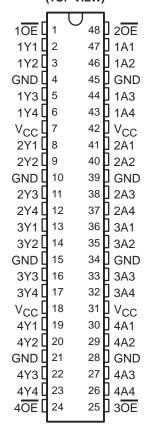
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- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25- $\Omega$  Series Resistors, So No External Resistors Are Required
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- High-Impedance State During Power Up and Power Down
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

#### description

The 'ABT162244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low outputenable  $(\overline{OE})$  inputs.

SN54ABT162244...WD PACKAGE SN74ABT162244...DGG, DGV, OR DL PACKAGE (TOP VIEW)



The outputs, which are designed to source or sink up to 12 mA, include equivalent 25- $\Omega$  series resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT162244 is characterized for operation from –40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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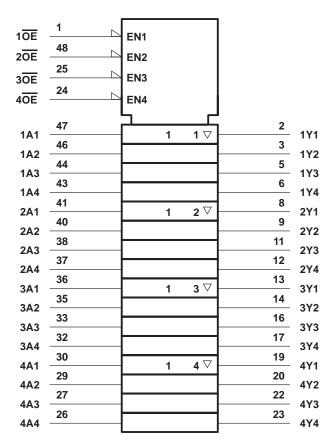
## SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS238D - JUNE 1992 - REVISED MAY 1997

## FUNCTION TABLE (each 4-bit buffer)

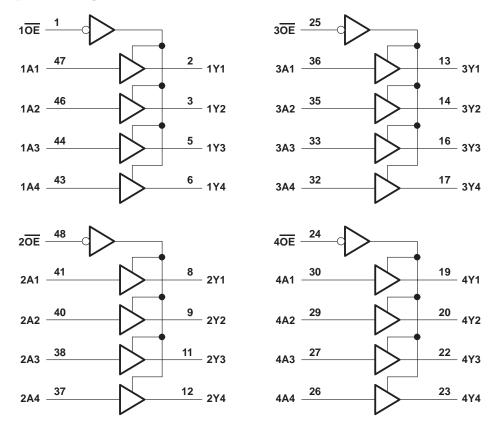
INPU	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

## logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	or power-off state, V <sub>O</sub>	0.5 V to 7 V 0.5 V to 5.5 V
Current into any output in the low state, I <sub>O</sub>		
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		
Package thermal impedance, $\theta_{\text{JA}}$ (see Note 2):		
<b>3</b> , , , , , , , , , , , , , , , , , , ,	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, T <sub>stg</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



## SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS238D – JUNE 1992 – REVISED MAY 1997

#### recommended operating conditions (see Note 3)

			SN54ABT	162244	SN74ABT	162244	UNIT
		MIN	MAX	MIN	MAX	UNII	
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V	
VI	Input voltage	0	Vcc	0	Vcc	V	
IOH	High-level output current			-12		-12	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SCBS238D - JUNE 1992 - REVISED MAY 1997

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CON	IDITIONS	Т	A = 25°0	;	SN54ABT	162244	SN74ABT	162244	UNIT	
PAI	RAMETER	TEST CON	IDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII	
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$			-1.2		-1.2		-1.2	V	
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -1 \text{ mA}$	3.35			3.35		3.35			
V <sub>OH</sub>		$V_{CC} = 5 V$ ,	$I_{OH} = -1 \text{ mA}$	3.85			3.85		3.85		V	
<sup>V</sup> OH		V <sub>CC</sub> = 4.5 V	$I_{OH} = -3 \text{ mA}$	3.1			3.1		3.1		v	
		VCC = 4.5 V	$I_{OH} = -12 \text{ mA}$	2.6*					2.6			
VOL		V <sub>CC</sub> = 4.5 V	$I_{OL} = 8 \text{ mA}$		0.4	8.0		0.8		0.65	V	
VOL		VCC = 4.5 V	I <sub>OL</sub> = 12 mA							8.0	V	
V <sub>hys</sub>					100						mV	
Ц		$V_{CC} = 0 \text{ to } 5.5 \text{ V, V}_{I}$	= V <sub>CC</sub> or GND			±1		±1		±1	μΑ	
lozpu <sup>‡</sup>	:	$V_{CC} = 0 \text{ to } 2.1 \text{ V},$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V}, \overline{OE} = X$				±50		±50		±50	μΑ	
I <sub>OZPD</sub> ‡	:	$V_{CC} = 2.1 \text{ V to 0},$ $V_{O} = 0.5 \text{ V to 2.7 V},$	OE = X			±50	±50 ±50 ±50				μΑ	
lozh	$V_{CC} = 2.1 \text{ V to } 5.5 \text{ V},$ $V_{O} = 2.7 \text{ V}, \overline{OE} \ge 2 \text{ V}$					10		10		10	μΑ	
lozL		$V_{CC} = 2.1 \text{ V} \text{ to } 5.5 \text{ V}$ $V_{O} = 0.5 \text{ V}, \overline{OE} \ge 2 \text{ V}$				-10		-10		-10	μΑ	
I <sub>off</sub>		$V_{CC} = 0$ , $V_I$ or $V_O \le$	4.5 V			±100				±100	μΑ	
ICEX		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Ouptputs high			50		50		50	μΑ	
ΙΟ§		$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 2.5 V	-25	-55	-100	-25	-100	-25	-100	mA	
		V <sub>CC</sub> = 5.5 V,	Outputs high			2		2		2		
ICC		$I_{O} = 0$ ,	Outputs low			30		30		30	mA	
		$V_I = V_{CC}$ or GND	Outputs disabled			2		2		2		
	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V,	Outputs enabled			50		50		50		
ΔICC¶	Data Iliputs	Other inputs at VCC or GND	Outputs disabled			50		50		50	μΑ	
	Control inputs	$V_{CC} = 5.5 \text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}$ or GND				50		50		50		
Ci	i V <sub>I</sub> = 2.5 V or 0.5 V 3							pF				
Co		V <sub>O</sub> = 2.5 V or 0.5 V			8						pF	

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter does not apply.



<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V. ‡ This parameter is characterized, but not production tested.

<sup>§</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

## SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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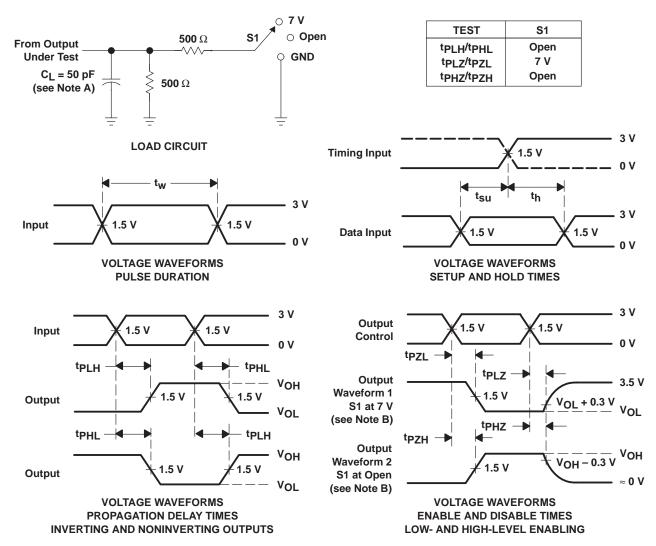
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	1 00 7 1				MIN	MAX	UNIT
			MIN	TYP	MAX	1		
t <sub>PLH</sub>	А	V	1	2.5	3.6	1	4.1	nc
t <sub>PHL</sub>	A	1	1	3.1	4.7	1	5.3	ns
<sup>t</sup> PZH	ŌĒ		1	3.2	4.8	1	5.6	ns
tPZL	OE	1	1	3.2	4.7	1	5.5	115
t <sub>PHZ</sub>	ŌĒ	V	1	3.2	5.3	1	6.3	nc
t <sub>PLZ</sub>	OE .	ſ	1	3.1	4.6	1	4.9	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L$  = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C MI			MIN	MAX	UNIT
			MIN	TYP	MAX			
<sup>t</sup> PLH	А	V	1	2.5	3.2	1	3.9	ns
<sup>t</sup> PHL	A	,	1	3.1	4	1	4.8	115
<sup>t</sup> PZH	ŌĒ	V	1	3.2	4.2	1	5.4	ns
t <sub>PZL</sub>	OE .	ī	1	3.2	4.1	1	5.1	115
<sup>t</sup> PHZ	ŌĒ	V	1	3.2	4	1	4.6	no
t <sub>PLZ</sub>	OE	ī	1	3.1	3.9	1	4.5	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z  $_{O}$  = 50  $\Omega$ ,  $t_{f}$   $\leq$  2.5 ns,  $t_{f}$   $\leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Product Folder: SN54ABT162244, 16-Bit Buffers/Drivers With 3-State Outputs

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#### SN54ABT162244, 16-Bit Buffers/Drivers With 3-State Outputs

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54ABT162244	SN74ABT162244
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.5 to 5.5
Input Level	TTL	TTL
Output Level	TTL	TTL
No. of Outputs	16	
Output Drive (mA)		-12/12
tpd max (ns)		4.8
Static Current		16
Logic	True	

FEATURES ▲Back to Top

- Members of the Texas Instruments Widebus<sup>TM</sup> Family
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**DESCRIPTION**■Back to Top

The 'ABT162244 are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low output-enable (OE\) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25- series resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, OE\ should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT162244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABT162244 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

▲Back to Top

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DATASHEET ▲Back to Top

Full datasheet in Acrobat PDF: sn54abt162244.pdf (117 KB,Rev.D) (Updated: 05/01/1997)

APPLICATION NOTES ▲Back to Top

View Application Notes for Digital Logic

- Advanced BiCMOS Technology (ABT) Logic Characterization Information (Rev. B) (SCBA008B Updated: 06/01/1997)
- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 Updated: 10/01/1996)
- Live Insertion (SDYA012 Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB Updated: 10/07/2002)

**USER GUIDES** 

▲Back to Top

• LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

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ORDERABLE DEVICE	<u>STATUS</u>	PACKAGE TYPE   PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY   \$US	STD PACK QTY	IN STOCK	<u>IN PROGRESS</u> QTY   DATE	LEAD TIME	<u>DISTRIBUTOR</u> COMPANY   REGION	IN STOCK	PURCHASE
5962-9458701QXA	ACTIVE	<u>CFP</u> (WD)   48	-55 TO 125		View Contents	1KU   22.39	1	<u>2</u> *	81   12 May	8 WKS	<u>Avnet</u>   Americas	66	BUY NOW
									33   19 May				
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SNJ54ABT162244WD	ACTIVE	<u>CFP</u> (WD)   48	-55 TO 125	5962- 9458701QXA	View Contents	1KU   22.39	1	<u>0</u> *	94   21 Apr	8 WKS	None Reported <u>View Distributors</u>		
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