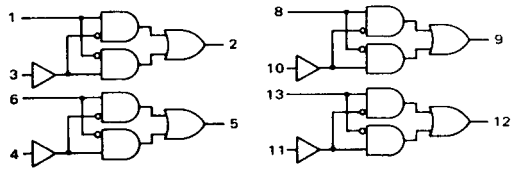
QUAD EXCLUSIVE "OR" GATES

MC1030
MC1230

Four gate arrays designed to provide four Exclusive OR functions. The output is high if and only if one input is high and all other inputs are low.

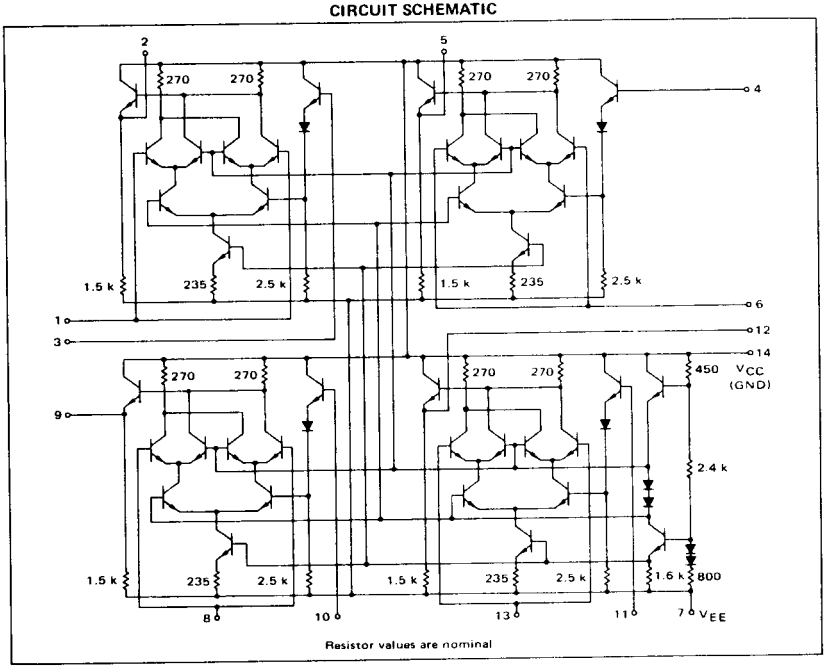
POSITIVE LOGIC



$2 = 1 \cdot \overline{3} + \overline{1} \cdot 3$

DC Input Loading Factor: Pins 1, 6, 8, 13 = 1.5
Pins 3, 4, 10, 11 = 1
DC Output Loading Factor = 25
Power Dissipation = 130 mW typical

CIRCUIT SCHEMATIC



Resistor values are nominal

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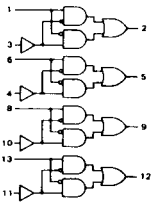


ELECTRICAL CHARACTERISTICS

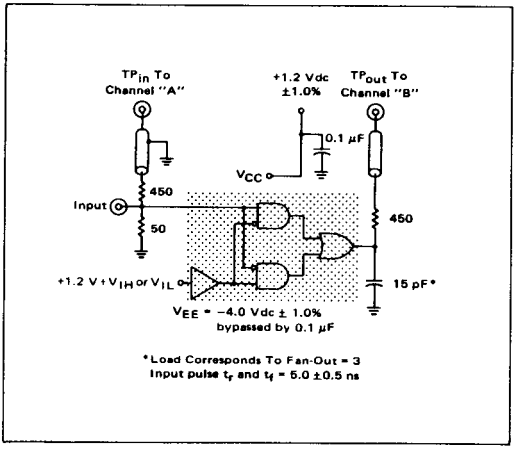
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1230 Test Limits							MC1030 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7	-	--	-	33	-	-	mAdc	-	-	-	33	-	-	mAdc
Input Current	I_{in}	1	-	-	-	150	-	-	μAdc	-	-	-	150	-	-	μAdc
		3	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
Input Leakage Current	I_R	1	-	-	-	0.4	-	2.0	μAdc	-	-	-	0.4	-	2.0	μAdc
		3	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
Logical "1" Output Voltage	V_{OH} ‡	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
		2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
Logical "0" Output Voltage	V_{OL}	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
		2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{1+2-}	2	5.0	8.5	5.0	8.5	6.0	10	ns	5.0	8.5	5.0	8.5	6.0	9.0	ns
	t_{1-2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{1+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{1-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
	t_{3+2-}		5.0	8.5	5.0	8.5		10		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{3-2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3+2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
	t_{3-2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	
Rise Time	t_{2+}		5.0	8.5	5.0	8.5		9.5		5.0	8.5	5.0	8.5	6.0	9.0	
	t_{2+}			8.0		8.0		9.0			8.0		8.0	5.0	8.5	
Fall Time	t_{2-}			8.5		8.5		10			8.5		8.5	6.0	9.0	
	t_{2-}		6.0	9.0	6.0	9.0		10		6.0	9.0	6.0	9.0	6.0	9.5	

‡V_{OH} limits apply from no load (0 mA) to full load (−2.5 mA).

*V_{IL} or V_{IH} value as given plus +1.2 V

SWITCHING TIME TEST CIRCUIT @ 25°C



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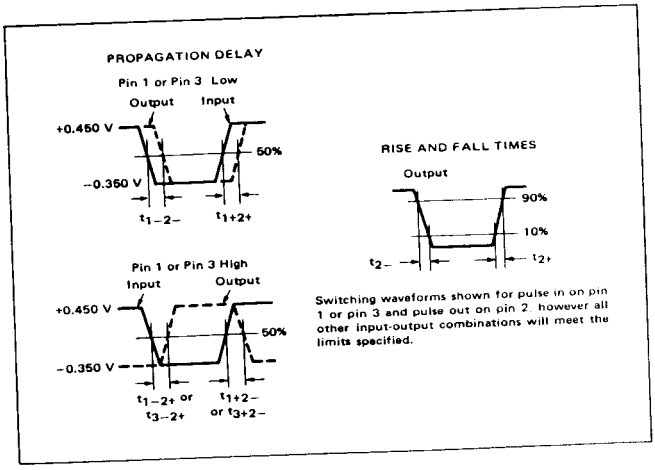
Characteristic	Symbol	Pin Under Test	@Test Temperature	V_{IL}	V_{IH}	$V_{IH\ max}$	V_{EE}	I_L mAdc	V_{CC} (Gnd)
				TEST VOLTAGE/CURRENT VALUES					
				Vdc ±1.0%				mAdc	
			−55°C	-1.580	-0.990	-	-5.2	-2.5	
			MC1230 +25°C	-1.500	-0.850	-0.700	-5.2	-2.5	
			+125°C	-1.380	-0.700	-	-5.2	-2.5	
			0°C	-1.525	-0.895	-	-5.2	-2.5	
			MC1030 +25°C	-1.500	-0.850	-0.700	-5.2	-2.5	
			+75°C	-1.435	-0.775	-	-5.2	-2.5	
				TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
Power Supply Drain Current	I_E	7		-	-	-	1, 3, 4, 6, 7, 8, 10, 11, 13	-	14
Input Current	I_{in}	1		-	-	1	3, 7	-	14
		3		-	-	3	1, 7	-	14
Input Leakage Current	I_R	1		-	-	-	1, 3, 7	-	14
		3		-	-	-	1, 3, 7	-	14
Logical "1" Output Voltage	V_{OH} ‡	2		1	3	-	7	2	14
		2		3	1	-	7	2	14
Logical "0" Output Voltage	V_{OL}	2		1, 3	-	-	7	-	14
		2		-	1, 3	-	7	-	14
Switching Times (Fan-Out = 3)				V_{IL}*	V_{IH}*	Pulse In	V_{EE} = −4.0 Vdc	Pulse Out	(+1.2 Vdc)
Propagation Delay	t_{1+2-}	2		-	3	1	7	2	14
	t_{1-2+}			-	3				
	t_{1+2+}			3	-				
	t_{1-2-}			3	-	↓			
	t_{3+2-}			-	1	3			
	t_{3-2+}			-	1				
	t_{3+2+}			1	-				
	t_{3-2-}			1	-	↓			
Rise Time	t_{2+}			-	3	1			
	t_{2+}			1	-	3			
Fall Time	t_{2-}			-	3	1			
	t_{2-}	↓		1	-	3	↓	↓	↓



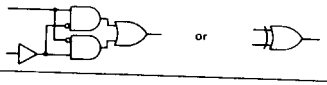
SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

SAMPLE TRUTH TABLE

Pin No.	Inputs 1	Inputs 3	Output 2
	0	0	0
	0	1	1
	1	0	1
	1	1	0

The Exclusive OR may be symbolized as:



The MC1030/MC1230 quad Exclusive OR gate is a high-speed device employing the series gating technique. The quad Exclusive OR (⊕) is useful in many applications such as data comparison, parity generation and checking, frequency mixing, decision circuitry, and code conversion circuitry. The output of each Exclusive OR is high if the two inputs are at different logic levels, while it is low if the inputs are at the same level.

Figure 1 illustrates the comparison of two 8-bit words. The OR output goes high if any Source "A" bit is not the same as the corresponding Source "B" bit. The comparison of two 16-bit words is possible by using two more MC1030/MC1230's, the other half of the MC1004/MC1204, and ORing the two OR outputs together. Note that the MC1030/MC1230 gates are paired together (in Wired-OR configuration) to save extra inputs on the MC1004/MC1204. Typical propagation delay time from inputs to the output of the MC1004/MC1204 is 10 ns.

Figure 2 illustrates checking the bits of a word for odd parity; if the sum of the inputs is odd, the output will be high. (It is also possible to mix MC1030/MC1230 quad Exclusive OR gates and MC1031/MC1231 quad Exclusive NOR gates to obtain the same function.)

FIGURE 1 – DATA COMPARATOR

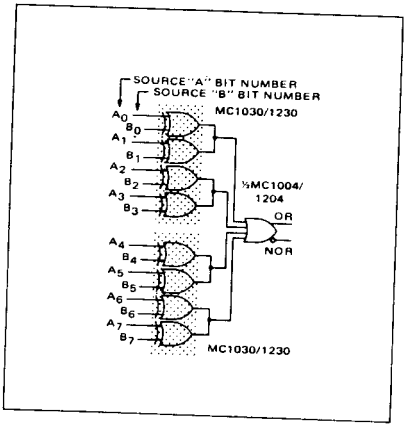
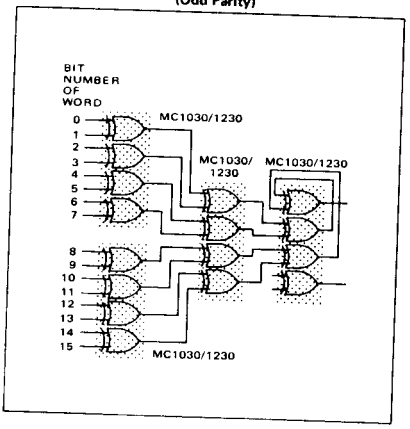


FIGURE 2 – 25 ns 16-BIT PARITY CHECKER (Odd Parity)



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