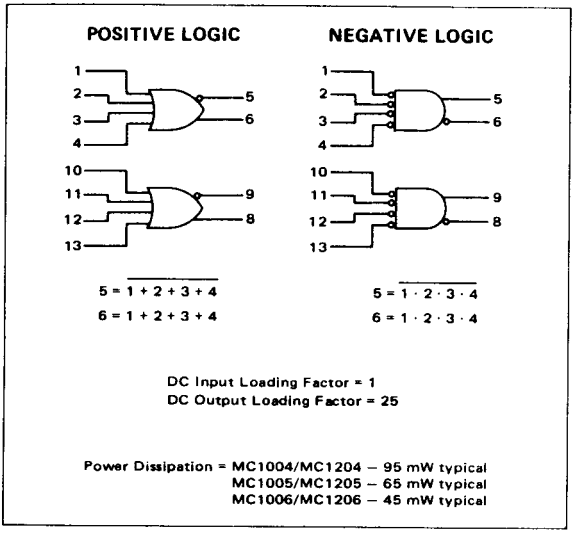
MC1004 thru MC1006
MC1204 thru MC1206

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

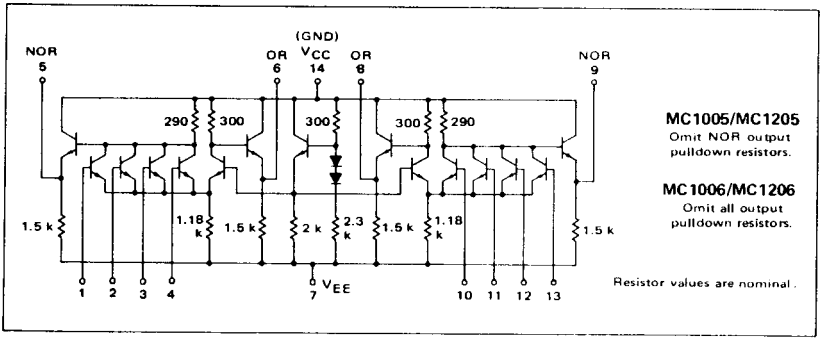
Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



DC Input Loading Factor = 1
DC Output Loading Factor = 25

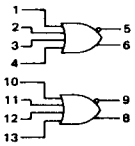
Power Dissipation = MC1004/MC1204 – 95 mW typical
MC1005/MC1205 – 65 mW typical
MC1006/MC1206 – 45 mW typical

MC1004/MC1204 CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gate is tested in the same manner. Outputs without pulldown resistors are tested with a 1.5 kΩ resistor to V_{EE}.



Characteristic	Symbol	Pin Under Test	MC1204-1206 Test Limits							MC1004-1006 Test Limits						
			−55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit
Power Supply Drain Current	I_E	7														
MC1204, MC1004			-	-	-	26	-	-	mAdc	-	-	-	26	-	-	mAdc
MC1205, MC1005			-	-	-	18	-	-		-	-	-	18	-	-	
MC1206, MC1006			-	-	-	12	-	-		-	-	-	12	-	-	
Input Current	I_{in}	1	-	-	-	100	-	-	μAdc	-	-	-	100	-	-	μAdc
		2	-	-	-		-	-		-	-	-		-	-	
		3	-	-	-		-	-		-	-	-		-	-	
		4	-	-	-		-	-		-	-	-		-	-	
Input Leakage Current	I_R	Inputs*	-	-	-	0.2	-	1.0	μAdc	-	-	-	0.2	-	1.0	μAdc
"NOR" Logical "1" Output Voltage‡	V_{OH}‡	5	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"NOR" Logical "0" Output Voltage	V_{OL}	5	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"OR" Logical "1" Output Voltage‡	V_{OH}‡	6	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"OR" Logical "0" Output Voltage	V_{OL}	6	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay (Fan-Out = 3)	t_{1+5-}	5	5.0	7.0	5.0	7.0	6.5	9.0	ns	5.0	7.0	5.0	7.0	6.0	8.0	ns
	t_{1-5+}	5	4.0	7.5	4.0	7.5	5.5	9.0		4.0	7.5	4.0	7.5	5.0	8.5	
	t_{1+6+}	6	4.0	7.5	4.0	7.0	5.5	8.5		4.0	7.0	4.0	7.0	5.0	8.0	
	t_{1-6-}	6	4.0	7.0	4.0	7.0	5.5	9.0		4.0	7.0	4.0	7.0	5.0	8.0	
(Fan-Out = 15)	t_{1+5-}	5	14	-	14	-	18	-		14	-	14	-	16	-	
	t_{1-5+}	5	5.0	-	5.0	-	7.0	-		5.0	-	5.0	-	6.0	-	
	t_{1+6+}	6	6.0	-	6.0	-	8.0	-		6.0	-	6.0	-	7.0	-	
	t_{1-6-}	6	13	-	13	-	17	-		13	-	13	-	15	-	
Rise Time (Fan-Out = 3)	t_{5+}	5	5.0	7.5	5.0	7.5	6.0	9.0		5.0	7.5	5.0	7.5	5.0	8.0	
	t_{6+}	6	4.0	7.0	4.0	6.5	5.5	8.0		4.0	6.5	4.0	6.5	5.0	7.0	
Fall Time (Fan-Out = 3)	t_{5-}	5	5.0	8.5	5.0	8.0	6.0	10		5.0	8.0	5.0	8.0	5.5	9.0	
	t_{6-}	6	5.0	8.0	5.0	8.0	7.0	10		5.0	8.0	5.0	8.0	6.0	9.0	

* Individually test each input using the pin connections shown. ‡ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).

@Test Temperature		TEST VOLTAGE/CURRENT VALUES Vdc ±1.0% $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	mAdc I_L
MC1204-1206	−55°C	-5.2 to -1.405	-1.165 to -0.625	-0.700	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700		-5.2	-2.5
	+125°C	-5.2 to -1.205	-0.875 to -0.550		-5.2	-2.5
MC1004-1006	0°C	-5.2 to -1.350	-1.070 to -0.740	-0.700	-5.2	-2.5
	+25°C	-5.2 to -1.325	-1.025 to -0.700		-5.2	-2.5
	+75°C	-5.2 to -1.260	-0.950 to -0.615		-5.2	-2.5

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IL\ min}$ to $V_{IL\ max}$	$V_{IH\ min}$ to $V_{IH\ max}$	$V_{IH\ max}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	7						
MC1204, MC1004			-	-		1, 2, 3, 4, 7, 10, 11, 12, 13		14
MC1205, MC1005			-	-				
MC1206, MC1006			-	-				
Input Current	I_{in}	1	-	-	1	2, 3, 4, 7, 10, 11, 12, 13	-	14
		2	-	-	2	1, 3, 4, 7, 10, 11, 12, 13		
		3	-	-	3	1, 2, 4, 7, 10, 11, 12, 13		
		4	-	-	4	1, 2, 3, 7, 10, 11, 12, 13		
Input Leakage Current	I_R	Inputs*	-	-	-	1, 2, 3, 4, 7, 10, 11, 12, 13		14
"NOR" Logical "1" Output Voltage†	V_{OH}‡	5	1	-	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
			2	-	-	1, 3, 4, 7, 10, 11, 12, 13		
			3	-	-	1, 2, 4, 7, 10, 11, 12, 13		
			4	-	-	1, 2, 3, 7, 10, 11, 12, 13		
"NOR" Logical "0" Output Voltage	V_{OL}	5	-	1	-	2, 3, 4, 7, 10, 11, 12, 13		14
			-	2	-	1, 3, 4, 7, 10, 11, 12, 13		
			-	3	-	1, 2, 4, 7, 10, 11, 12, 13		
			-	4	-	1, 2, 3, 7, 10, 11, 12, 13		
"OR" Logical "1" Output Voltage†	V_{OH}‡	6	-	1	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
			-	2	-	1, 3, 4, 7, 10, 11, 12, 13		
			-	3	-	1, 2, 4, 7, 10, 11, 12, 13		
			-	4	-	1, 2, 3, 7, 10, 11, 12, 13		
"OR" Logical "0" Output Voltage	V_{OL}	6	1	-	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
			2	-	-	1, 3, 4, 7, 10, 11, 12, 13		
			3	-	-	1, 2, 4, 7, 10, 11, 12, 13		
			4	-	-	1, 2, 3, 7, 10, 11, 12, 13		
Switching Times Propagation Delay			Pulse In	Pulse Out		V_{EE} = −4.0 Vdc		(+1.2 V)
(Fan-Out = 3)	t_{1+5-}	5	1	5	-	2, 3, 4, 7, 10, 11, 12, 13	-	14
	t_{1-5+}	5		5	-			
	t_{1+6-}	6		6	-			
	t_{1-6+}	6		6	-			
(Fan-Out = 15)	t_{1+5-}	5		5	-			
	t_{1-5+}	5		5	-			
	t_{1+6-}	6		6	-			
	t_{1-6+}	6		6	-			
Rise Time (Fan-Out = 3)	t_{5+}	5		5	-			
	t_{6+}	6		6	-			
Fall Time (Fan-Out = 3)	t_{5-}	5		5	-			
	t_{6-}	6		6	-			

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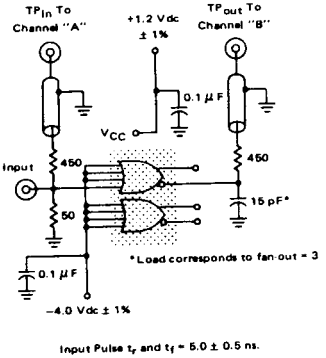
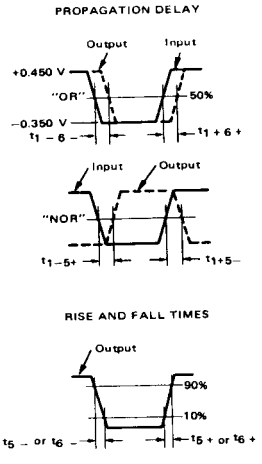
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse t_r and t_f = 5.0 ± 0.5 ns.

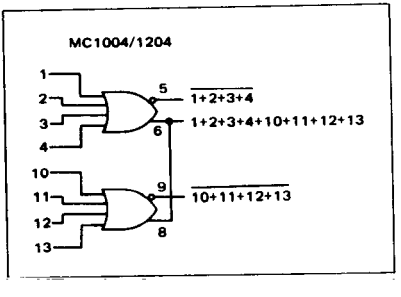


Switching waveforms shown for pulse in on pin 1 and pulse out on pins 5 and 6, however all other input-output combinations will meet the limits specified.

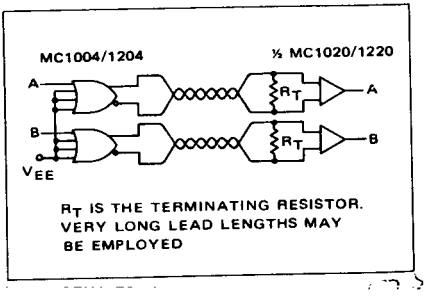
APPLICATIONS INFORMATION

The MC1004-1006/MC1204-1206 dual 4-input OR/NOR gates are very useful in generating system logic due to their flexibility. By employing negative logic on the inputs (low level of − 1.6 V is considered true), the AND/NAND logic function is obtained from the basic gate. Since complementary inputs are available in MECL system, OR/NOR-AND/NAND logic may be employed, reducing the package count in the system. An 8-input OR or AND gate is obtained by tying the OR outputs together and using positive or negative logic. The dual 4-input gate is also useful for driving two twisted pair lines where the lines must carry independent information. For a further discussion of twisted pair driving and receiving, refer to MC1020/MC1220 Line Receiver.

8-INPUT "OR" GATE (positive logic) or 8-INPUT "AND" GATE (negative logic)



DUAL 4-INPUT GATE USED TO DRIVE TWO BALANCED TWISTED PAIR LINES



R_T IS THE TERMINATING RESISTOR. VERY LONG LEAD LENGTHS MAY BE EMPLOYED