LM10692 Power Management Unit for SandForce SF3700 SSD Controllers

1 Features

- Six High-efficiency Programmable Buck Regulators:
  - Integrated FETs with Low RDSon
  - Bucks Operate Phase Shifted to Reduce the Input
  - Current ripple And Capacitor Size
  - Output Voltage Programmable via Serial interface
  - Under and Over Voltage Lock-out
  - Automatic Internal Soft Start
  - Output Current Overload and Thermal Shutdown Protection
  - Active Discharge for Fast Discharge of Output Voltage When Buck is Disabled
- I2C Compatible Serial Interface, up to 1 MHz
- Power-On-Reset Output with Delay and Input Voltage Trigger
- Independent Enable Input Pins and Power Good output Pins for Control of Always-On (AON) and Core Power (CPE) Rails
- RMY Package Size 5.00 mm x 5.00 mm x 0.9 mm (NOM)
- **Key Specifications**
  - Single Input Rail with Wide Range: 2.5 V to 4.0 V
  - Programmable Output Voltage:
    - Buck1: 1.75 V to 3.3 V, 2.5 A
    - Buck2: 1.0 V to 2.55 V, 200 mA
    - Buck3: 0.8 V to 2.35 V, 200 mA
    - Buck4: 0.8 V to 2.35 V, 2.5 A
    - Buck5: 0.8 V to 1.575 V, 0.8 A
    - Buck6: 0.8 V to 1.575 V, 2.5 A
  - Buck1 Configurable as Bypass Switch (No Inductor)
  - ±1% Feedback Voltage Accuracy
  - Up to 95% Peak efficiency Buck Regulators
  - 2 MHz Switching Frequency For Smaller Inductor Size

2 Applications

- Optimized for Use in SSDs
- Embedded Systems: SoCs, ASICs, and Processors

3 Description

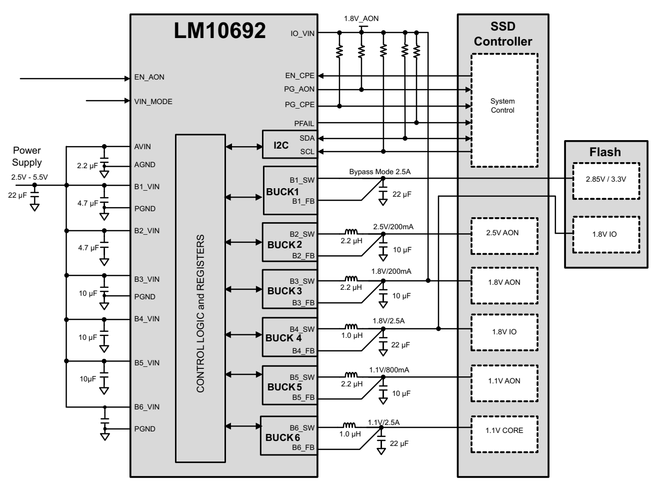
The LM10692 is an advanced PMU containing six configurable, buck regulators for supplying power to advanced Flash Controllers in solid-state drives (SSDs). The device is ideal for use in solid state drive designs. The LM10692 communicates with the SF3700 Flash Controller via an I2C compatible interface and digital I/O pins to optimize power consumption with power saving modes.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM10692	QFN (36)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



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4 Revision History

DATE	REVISION	NOTES
June 2014	*	Initial release.

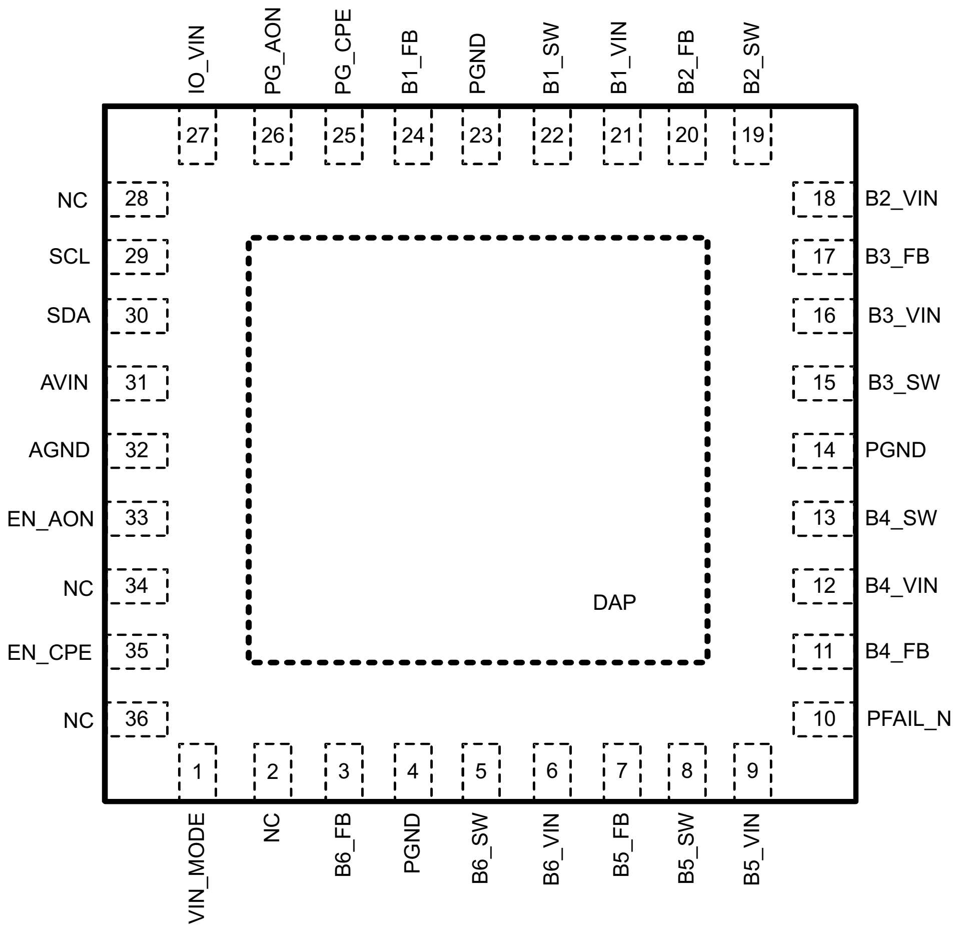
5 Device Comparison Table

Variants

	1.1V PCIe / SATA	1.15V PCIe
	LM10692	**LM10692B**
Buck1	2.85V	2.85V
Buck2	2.5V	2.5V
Buck3	1.8V	1.8V
Buck4	1.8V	1.8V
Buck5	1.1V	1.15V
Buck6	1.1V	1.15V

6 Pin Configuration and Functions

36 Pin
LLP Package
Top View



Pin Functions

PIN		I/O	TYPE (1)	DESCRIPTION
NUMBER	NAME			
1	VIN_MODE	I	D	Leave floating for the LM10692. Input pin defines Buck1 mode operation.
2	NC	-	-	Leave Floating
3	B6_FB	I	A	Buck Switcher Regulator 6 – Voltage output feedback for Buck Regulator 6
4	PGND	G	P	Power ground for Buck Regulator –Return Input and Output Cap to this pin
5	B6_SW	O	P	Buck Switcher Regulator 6 – Power Switching node, connect to inductor
6	B6_VIN	I	P	Buck Switcher Regulator 6 – Power supply voltage input for power stage PFET.
7	B5_FB	I	A	Buck Switcher Regulator 5 – Voltage output feedback for Buck Regulator 5
8	B5_SW	O	P	Buck Switcher Regulator 5 – Power Switching node, connect to inductor
9	B5_VIN	I	P	Buck Switcher Regulator 5-Power supply voltage input for power stage PFET.
10	PFAIL_N	O	D	Provides reset function to controller. Monitors VIN. Digital Output. Open Drain.
11	B4_FB	I	A	Buck Switcher Regulator 4 – Voltage output feedback for Buck Regulator 4
12	B4_VIN	I	P	Buck Switcher Regulator 4 – Power supply voltage input for power stage PFET.
13	B4_SW	O	P	Buck Switcher Regulator 4 – Power Switching node, connect to inductor
14	PGND	G	P	Power ground for Buck Regulator – Return Input and Output Cap to this pin

(1) **A**: Analog Pin; **D**: Digital Pin; **G**: Ground Pin; **P**: Power Pin; **I**: Input Pin; **O**: Output Pin

Pin Functions (continued)

PIN		I/O	TYPE (1)	DESCRIPTION
NUMBER	NAME			
15	B3_SW	O	P	Buck Switcher Regulator 3 – Power Switching node, connect to inductor
16	B3_VIN	I	P	Buck Switcher Regulator 3 – Power supply voltage input for power stage PFET
17	B3_FB	I	A	Buck Switcher Regulator 3 – Voltage output feedback for Buck Regulator 3
18	B2_VIN	I	P	Buck Switcher Regulator 2 – Power supply voltage input for power stage PFET
19	B2_SW	O	P	Buck Switcher Regulator 2 – Power Switching node, connect to inductor
20	B2_FB	I	A	Buck Switcher Regulator 2 – Voltage output feedback for Buck Regulator 2
21	B1_VIN	I	P	Buck Switcher Regulator 1 – Power supply voltage input for power stage PFET
22	B1_SW	O	P	Buck Switcher Regulator 1 – Power Switching node, connect to inductor
23	PGND	G	P	Power ground for Buck Regulator – Return Input and Output Cap to this pin
24	B1_FB	I	A	Buck Switcher Regulator 1 – Voltage output feedback for Buck Regulator 1
25	PG_CPE	O	D	Power good output for core power rails – Buck 1, Buck 4, and Buck 6, open drain
26	PG_AON	O	D	Power good pin for always on rails – Buck 2, Buck 3, and Buck 5, open drain
27	IO_VIN	I	P	Reference supply for digital interface to controller.
28	NC	-	-	Leave Floating
29	SCL	I	D	Digital interface for I2C Clock signal. Open Drain.
30	SDA	IO	D	Digital interface for I2C Data signal. Open Drain.
31	AVIN	I	P	Power Supply input Voltage. Must be present for device to work.
32	AGND	G	P	Power Supply Ground. Must be grounded for device to work.
33	EN_AON	I	D	Enable pin for always on rails – Buck 2, Buck 3, and Buck 5
34	NC	-	-	Leave Floating
35	EN_CPE	I	D	Enable for core power rails – Buck 1, Buck 4, and Buck 6
36	NC	-	-	Leave Floating
DAP	PGND	-	-	Thermally bonded. Needs low-impedance thermal connection to PCB

7 Specifications

7.1 Absolute Maximum Ratings[(1)(2)(3)(4)]

over operating free-air temperature range (unless otherwise noted) [(5)]

	MIN	MAX	UNIT
Any supply pin, VIN to GND	-0.3	6	V
Any signal pin	-0.3	+(VIN+0.3)V but not over 6.0V	V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are measured with respect to the potential at the GND pins.
(3) VIN refers to these power pins connected together: VIN_B1 = VIN_B2=VI_B3 = VIN_B4 = VIN_B5 = VIN_B6 = VIN
(4) GND Pins means all ground pins must be connected together.
(5) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]		1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions[(1)(2)(3)(4)]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN, VIN_B2, VIN_B3, VIN_B4, VIN_B5	2.5	5.5	V
VIN_B1, VIN_B6	2.5	4	V
Junction Temperature, T_J	-40	125	°C
Ambient Temperature, T_A	-40	85	°C
Storage Temperature	-65	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are measured with respect to the potential at the GND pins.
(3) VIN refers to these power pins connected together: VIN_B1 = VIN_B2=VI_B3 = VIN_B4 = VIN_B5 = VIN_B6 = VIN
(4) GND Pins means all ground pins must be connected together.

7.4 Thermal Information

THERMAL METRIC[(1)]		LM10692 RMY 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.2	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	6.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics[1][2]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2= VIN_B3=VIN_B4=VIN_B5= VIN_B6.

PARAMETER		TEST CONDITIONS	–40°C ≤ T_A ≤ T_J ≤ +85°C			T_A = 25°C			UNIT
			MIN	TYP [3]	MAX	MIN	TYP [3]	MAX	
I_{Q_OFF}	Quiescent supply current.	All Bucks OFF					8		µA
I_{Q_AON}	Quiescent supply current	All Bucks unloaded, EN_CPE low					250		µA
I_Q	Quiescent supply current.	All Bucks unloaded and in PFM mode					320		µA
I_{Q_ALLON}	Quiescent supply current	All Bucks unloaded, Buck6 in FPWM mode (default operating mode)					6		mA
UNDER/OVER VOLTAGE LOCK OUT									
V_{UVLO_RISING}		Factory pre-set			2.50		2.4		V
$V_{UVLO\_FALLING}$		Factory pre-set			2.40		2.3		V
V_{OVLO_RISING}		Factory pre-set					6.1	6.25	V
$V_{OVLO\_FALLING}$		Factory pre-set					5.8		V
THERMAL SHUTDOWN									
T_{SD}	Thermal Shutdown Temperature		145		160				°C
DIGITAL INTERFACE									
V_{IL-IO}	Logic Input Low	SDA, SCL			0.4				V
V_{IH-IO}	Logic Input High	SDA, SCL	1.05						V
V_{OL-IO}	Logic Output Low	SDA			0.4				V
V_{DDIO} Range	External Logic pullup voltage for IO_VIN		1.2		V_{IN}				V
I_{IL}	Input Current, pin driven low					-2			µA
						-5			
I_{IH}	Input Current, pin driven high	VIN_MODE						2	µA
								5	
f_{I2C_MAX}	I^2C max frequency	IO_VIN = 1.8 V Max frequency is application specific						1000	kHz
V_{IL-VIN_MODE}	VIN_MODE input low	(See [3])						GND +0.3	V
V_{IH-VIN_MODE}	VIN_MODE input high	(See [3])				VIN-0.3			V
PFAIL THRESHOLD and BYPASS THRESHOLD									
$V_{PFAIL-falling}$	PFAIL_N falling threshold voltage	VIN_MODE = GND or FLOATING				2.3	2.6	3.3	V
$V_{PFAIL-rising}$	PFAIL_N rising threshold voltage	VIN_MODE = GND or FLOATING				2.3	2.7	3.3	V
T_{PFAIL}	PFAIL_N rise delay time	Active High[3], default trim					4		ms
V_{BYPASS}	Bypass Mode threshold (transitions from PWM to Bypass mode when input voltage falls below V_{BYPASS}).	VIN_MODE = GND					2.9		V

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25MC. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

7.6 Buck 1 Electrical Characteristic[(1)][(2)]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2, VIN_B3=VIN_B4=VIN_B5= VIN_B6.
The application circuit used is the one shown in “Typical Application Circuit"

PARAMETER		TEST CONDITIONS	T_A = 25°C MIN	TYP[(3)]	MAX	UNIT
V_{OUT}	Output Voltage default value		2.76	2.85	2.93	V
$I_{OUT-MAX}$	Continuous maximum load current	Buck 1 enabled, (see [(3)])		2.5		A
I_{PEAK}	Peak switching current limit	Buck 1 enabled		4.2		A
η_{SW1-5V}	Efficiency, Buck 1[(3)]	I_{OUT} = 5mA to 1A, V_{IN} = 3.3 V	80%		95%	
F_{SW}	Switching Frequency	PWM operation		2		MHz
C_{IN}	Input Capacitor[(3)]	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		22		µF
C_{OUT}	Output Filter Capacitor[(3)]			22		µF
	Output Capacitor ESR[(3)]			10		mΩ
L	Output Filter Inductance[(3)]			1		µH
V_{FB1}	Feedback Voltage	V_{OUT} = 2.85 V (default), PWM Mode, No Load (%)		2.85		V
ΔV_{OUT}	DC Line regulation[(3)]	2.5 V ≤ V_{IN} ≤ 5V, I_{OUT} = $I_{OUT-MAX}$	-1%		1%	
	DC Load regulation[(3)]	Vin = 3.3 V , 0.1 × $I_{OUT-MAX}$ ≤ Iout ≤ $I_{OUT-MAX}$	-1%		1%	
I_{FB}	Feedback pin input bias current	V_{FB} = 2.85 V			7	µA
$R_{DS-ON-HS}$	High Side Switch On Resistance	Measured pin-to-pin, Vin = 3.3 V		80		mΩ
$R_{DS-ON-LS}$	Low Side Switch On Resistance			115		mΩ
$R_{DISCHARGE}$	Active Discharge Resistance	Measured from FB to GND		20		Ω
T_{start}	Internal soft-start (turn on time)	Start up from shutdown, V_{OUT} = 0 V, no load, V_{OUT} = 95% of 3.3 V in bypass mode[(3)], Cout = 22µF		470		µs
		Start up from shutdown, V_{OUT} = 0 V, no load, VOUT = 95% of 3.3 V in bypass mode[(3)], Cout = 66µF		530		µs

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25MC. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

7.7 Buck 2 Electrical Characteristic[(1)(2)]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2, VIN_B3=VIN_B4=VIN_B5= VIN_B6.
The application circuit used is the one shown in “Typical Application Circuit"

PARAMETER		CONDITIONS	T_A = 25°C			UNIT
			MIN	TYP[(3)]	MAX	
V_{OUT}	Output Voltage default value		2.42	2.5	2.57	V
$I_{OUT-MAX}$	Continuous maximum load current	Buck 2 enabled[(3)]		0.2		A
I_{PEAK}	Peak switching current limit	Buck 2 enabled		1.9		A
η_{SW2-5V}	Efficiency, Buck 2[(3)]	I_{OUT} = 100 µA to 0.2 A, V_{OUT} = 2.5 V, L= 2.2 µH, ESRL = 220 mΩ	80%		90%	
F_{SW}	Switching Frequency	PWM operation		2		MHz
C_{IN}	Input Capacitor[(3)]	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor[(3)]			10		µF
	Output Capacitor ESR[(3)]			10		mΩ
L	Output Filter Inductance[(3)]			2.2		µH
V_{FB2}	Feedback Voltage	V_{OUT} = 2.5 V (default), PWM Mode, No Load		2.5		V
ΔV_{OUT}	DC Line regulation[(3)]	2.9 V ≤ VIN ≤5.0V, I_{OUT} = $I_{OUT-MAX}$	-1%		1%	
	DC Load regulation[(3)]	Vin = 3.3, 0.1 × $I_{OUT-MAX}$ ≤ I_{out} ≤ $I_{OUT-MAX}$	-1%		1%	
I_{FB}	Feedback pin input bias current	V_{FB} = 2.5 V			5	µA
$R_{DS-ON-HS}$	High Side Switch On Resistance	Measured pin-to-pin, Vin = 3.3 V		135		mΩ
$R_{DS-ON-LS}$	Low Side Switch On Resistance			105		mΩ
$R_{DISCHARGE}$	Active Discharge Resistance	Measured from FB to GND		18		Ω
T_{start}	Internal soft-start (turn on time)	Start up from shutdown, V_{OUT}= 0 V, no load, VOUT = 95% of 2.5 V[(3)], Cout=22µF		275		µs

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25MC. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

7.8 Buck 3 Electrical Characteristics[(1)(2)]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2, VIN_B3=VIN_B4=VIN_B5= VIN_B6.
The application circuit used is the one shown in “Typical Application Circuit".

PARAMETER		TEST CONDITIONS	T_A = 25°C			UNIT
			MIN	TYP[(3)]	MAX	
V_{OUT}	Output Voltage default value		1.75	1.8	1.85	V
$I_{OUT\text{-}MAX}$	Continuous maximum load current	Buck 3 enabled,[(3)]		0.2		A
I_{PEAK}	Peak switching current limit	Buck 3 enabled		0.8		A
ηSW3-5V	Efficiency, Buck 3[(3)]	I_{OUT} = 5mA to 0.2 A, 1.8 V_{out}, L = 2.2 µH, ESRL = 200 mΩ	80%		90%	
F_{SW}	Switching Frequency	PWM operation		2		MHz
C_{IN}	Input Capacitor[(3)]	0 mA ≤ I_{OUT} ≤ $I_{OUT\text{-}MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor[(3)]			10		µF
	Output Capacitor ESR[(3)]			10		mΩ
L	Output Filter Inductance[(3)]			2.2		µH
VFB3	Feedback Voltage	V_{OUT} = 1.8 V (default), PWM Mode, No Load		1.8		V
ΔV_{OUT}	DC Line regulation[(3)]	2.9V ≤ VIN ≤ 5.0 V, I_{OUT} = $I_{OUT\text{-}MAX}$	-1%		+1%	
	DC Load regulation[(3)]	Vin = 3.3 V, 0.1 × $I_{OUT\text{-}MAX}$ ≤ Iout ≤ $I_{OUT\text{-}MAX}$	-1%		+1%	
I_{FB}	Feedback pin input bias current	V_{FB} = 1.8 V			3.5	µA
$R_{DS\text{-}ON\text{-}HS}$	High Side Switch On Resistance	Measured pin-to-pin, Vin = 3.3 V		220		mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low Side Switch On Resistance			105		mΩ
$R_{DISCHARGE}$	Active Discharge Resistance	Measured from FB to GND		18		Ω
T_{start}	Internal soft-start (turn on time)	Start up from shutdown, V_{OUT} = 0 V, no load, V_{OUT} = 95% of 1.8 V[(3)], C_{out} = 22 µF		190		µs

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25MC. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

7.9 Buck 4 Electrical Characteristic[1][2]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2, VIN_B3=VIN_B4=VIN_B5= VIN_B6.
The application circuit used is the one shown in “Typical Application Circuit".

PARAMETER		TEST CONDITIONS	T_A = 25°C			UNIT
			MIN	TYP[3]	MAX	
V_{OUT}	Output Voltage default value		1.75	1.8	1.85	V
$I_{OUT-MAX}$	Continuous maximum load current	Buck 4 enabled,[4]		2.5		A
I_{PEAK}	Peak switching current limit	Buck 4 enabled		3.6		A
ηSW4-5V	Efficiency, Buck 4[4]	I_{OUT} = 5mA to 1A, V_{OUT} = 1.8 V, L = 1 µH, ESRL = 50 mΩ	80%		90%	
F_{SW}	Switching Frequency	PWM operation		2		MHz
C_{IN}	Input Capacitor[4]	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		22		µF
C_{OUT}	Output Filter Capacitor[4]			22		µF
	Output Capacitor ESR[4]			10		mΩ
L	Output Filter Inductance[4]			1		µH
V_{FB4}	Feedback Voltage	V_{OUT} = 1.8V (default), PWM Mode, No Load		1.8		V
ΔV_{OUT}	DC Line regulation[4]	2.9 ≤ VIN ≤ 5.0 V, I_{OUT} = $I_{OUT-MAX}$	-1%		+1%	
	DC Load regulation[4]	Vin = 3.3 V, 0.1 × $I_{OUT-MAX}$ ≤ I_{out} ≤ $I_{OUT-MAX}$	-1%		+1%	
I_{FB}	Feedback pin input bias current	V_{FB} = 1.8 V			3.5	µA
$R_{DS-ON-HS}$	High Side Switch On Resistance	Measured pin-to-pin, Vin = 3.3 V		85		mΩ
$R_{DS-ON-LS}$	Low Side Switch On Resistance			60		mΩ
$R_{DISCHARGE}$	Active Discharge Resistance	Measured from FB to GND		18		Ω
T_{start}	Internal soft-start (turn on time)	Start up from shutdown, V_{OUT} = 0 V, no load, V_{OUT} = 95% of 1.8 V,[4] Cout = 22µF		165		µs

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25MC. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.
(4) Specification ensured by design. Not tested during production.

7.10 Buck 5 Electrical Characteristic[1][2]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2, VIN_B3=VIN_B4=VIN_B5= VIN_B6.
The application circuit used is the one shown in “Typical Application Circuit".

PARAMETER		TEST CONDITIONS	T_A = 25°C MIN	TYP[3]	MAX	UNIT
V_{OUT}	Output Voltage default value		1.07	1.1	1.13	V
$I_{OUT-MAX}$	Continuous maximum load current	Buck 5 enabled,[4]		0.8		A
I_{PEAK}	Peak switching current limit	Buck 5 enabled		2		A
ηSW5-5V	Efficiency, Buck 5[4]	I_{OUT} = 5mA to 600 mA, V_{OUT} = 1.1V, L = 2.2 µH, ESRL = 200 mΩ	80%		90%	
F_{SW}	Switching Frequency	PWM operation		2		MHz
C_{IN}	Input Capacitor[4]	0 mA ≤ I_{OUT} ≤ $I_{OUT-MAX}$		4.7		µF
C_{OUT}	Output Filter Capacitor[4]			10		µF
	Output Capacitor ESR[4]			10		mΩ
L	Output Filter Inductance[4]			2.2		uH
VFB5	Feedback Voltage	V_{OUT} = 1.1V (default), PWM Mode, No Load		1.1		V
Δ_{VOUT}	DC Line regulation[4]	2.9 V ≤ VIN ≤ 5 V, I_{OUT} = $I_{OUT-MAX}$	-1%		+1%	
	DC Load regulation[4]	Vin = 3.3 V , 0.1 × $I_{OUT-MAX}$ ≤ I_{out} ≤ $I_{OUT-MAX}$	-1%		+1%	
I_{FB}	Feedback pin input bias current	V_{FB}=1.1V			2.5	µA
$R_{DS-ON-HS}$	High Side Switch On Resistance	Measured pin-to-pin, Vin = 3.3 V		120		mΩ
$R_{DS-ON-LS}$	Low Side Switch On Resistance			85		mΩ
$R_{DISCHARGE}$	Active Discharge Resistance	Measured from FB to GND		18		Ω
T_{start}	Internal soft-start (turn on time)	Start up from shutdown, V_{OUT} = 0 V, no load, V_{OUT} = 95% of 1.05 V[4], Cout = 22 µF		145		µs

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25M C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.
(4) Specification ensured by design. Not tested during production.

7.11 Buck 6 Electrical Characteristic[1][2]

over operating free-air temperature range (unless otherwise noted)
Unless otherwise noted, VIN = 3.3V, where: VIN =VIN_B1=VIN_B2, VIN_B3=VIN_B4=VIN_B5= VIN_B6.
The application circuit used is the one shown in “Typical Application Circuit".

PARAMETER		TEST CONDITIONS	T_A = 25°C			UNIT
			MIN	TYP[3]	MAX	
V_{OUT}	Output Voltage default value		1.07	1.1	1.07	V
I_Q	DC Bias Current in Vin	No Load, PFM Mode				mA
$I_{OUT\text{-}MAX}$	Continuous maximum load current	Buck 6 enabled,[3]		2.5		A
I_{PEAK}	Peak switching current limit	Buck 6 enabled		4.1		A
$\eta_{SW6\text{-}5V}$	Efficiency, Buck 6[3]	I_{OUT} = 100 mA – 1 A , V_{OUT} = 1.1 V, L = 1 µH, ESRL = 50 mΩ	80%		90%	
F_{SW}	Switching Frequency	PWM operation		2		MHz
C_{IN}	Input Capacitor[3]	0 mA ≤ I_{OUT} ≤ $I_{OUT\text{-}MAX}$		22		µF
C_{OUT}	Output Filter Capacitor[3]			22		µF
	Output Capacitor ESR[3]			10		mΩ
L	Output Filter Inductance[3]			1		µH
V_{FB6}	Feedback Voltage Accuracy	V_{OUT} = 1.05 V (default), PWM Mode, No Load (%)		1.1		V
ΔV_{OUT}	DC Line regulation[3]	2.9V ≤ V_{IN} ≤ 4.0 V, I_{OUT} = $I_{OUT\text{-}MAX}$	-1%		1%	
	DC Load regulation[3]	V in = 3.3V, 0.1 × $I_{OUT\text{-}MAX}$ ≤ I_{out} ≤ $I_{OUT\text{-}MAX}$	-1%		1%	
I_{FB}	Feedback pin input bias current	V_{FB}=1.1V			2.5	µA
$R_{DS\text{-}ON\text{-}HS}$	High Side Switch On Resistance	Vin = 3.3 V		70		mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low Side Switch On Resistance			65		mΩ
$R_{DISCHARGE}$	Active Discharge Resistance	Measured from FB to GND		18		Ω
T_{start}	Internal soft-start (turn on time)	Start up from shutdown, V_{OUT} = 0 V, no load, V_{OUT} = 95% of 1.1 V[3], Cout=22µF		145		µs

(1) All limits are guaranteed by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with TA = 25MC. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

7.12 Typical Characteristics, Efficiency

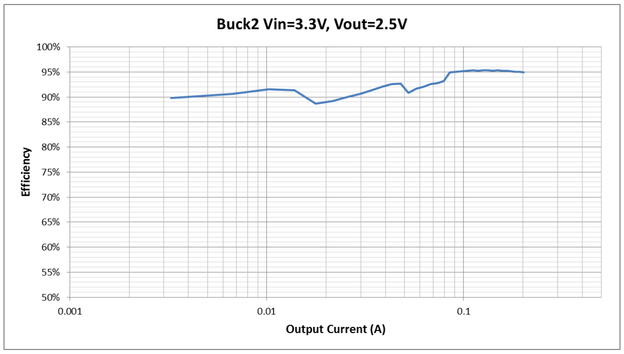


Figure 1. Buck 2, Vin = 3.3 V, Vout = 1.8 V, Inductor: IFSC0806AZER2R2M01

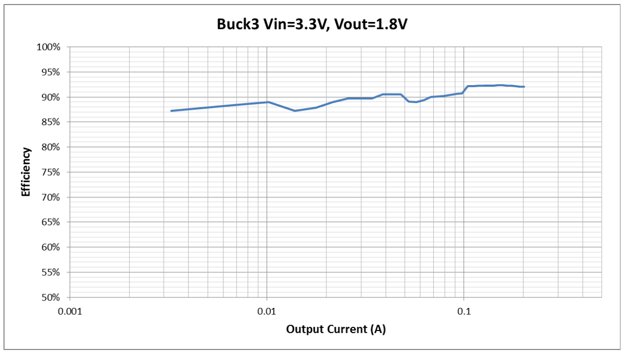


Figure 2. Buck 3, Vin = 3.3 V, Vout = 1.8 V, Inductor: IFSC0806AZER2R2M01

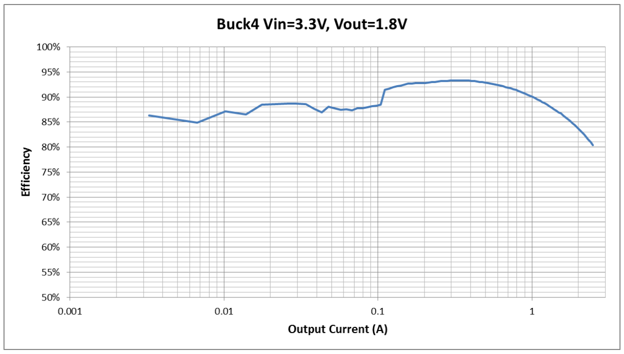


Figure 3. Buck 4, Vin = 3.3 V, Vout = 1.8 V, Inductor: MAMK2520T1R0

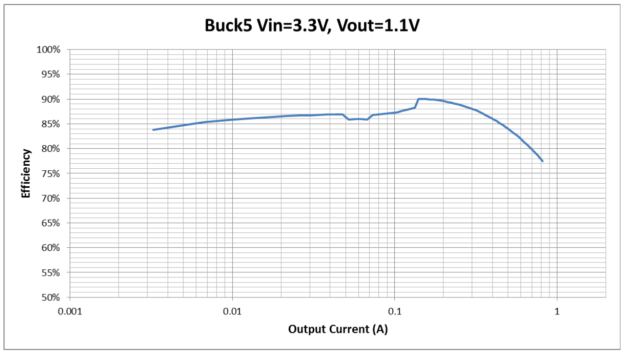


Figure 4. Buck 5, Vin = 3.3 V, Vout = 1.1 V, Inductor: IFSC0806AZER2R2M01

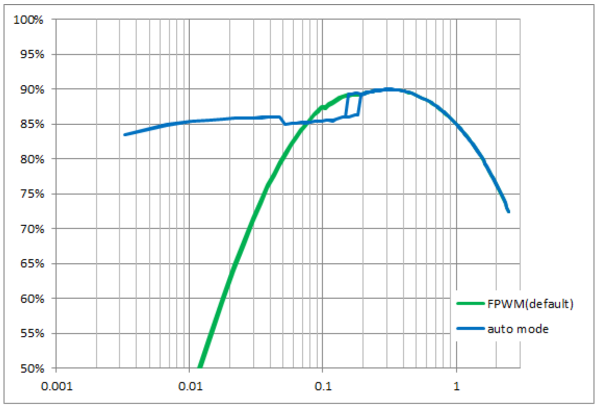


Figure 5. Buck 6, Vin = 3.3 V, Vout = 1.1 V, Inductor: MAMK2520T1R0

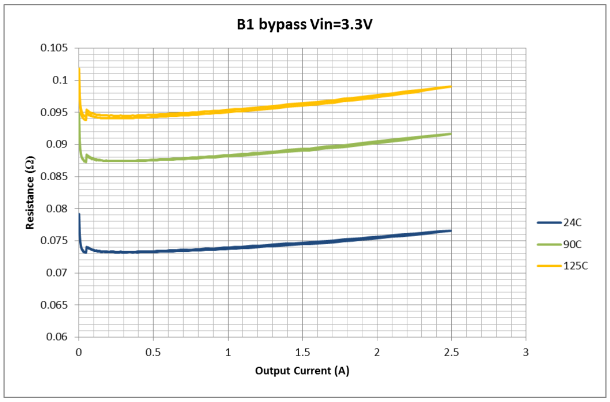


Figure 6. B1 Bypass, Vin = 3.3 V

7.13 Typical Characteristics, Load Regulation

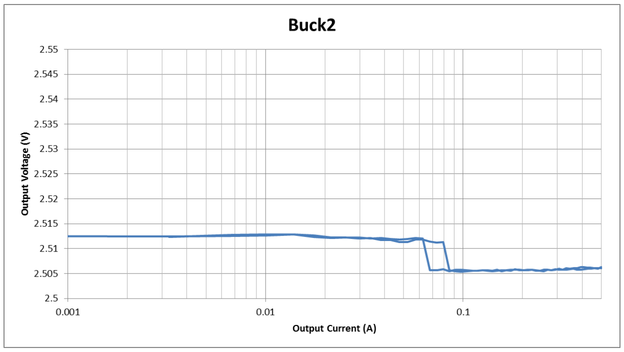


Figure 7. Buck 2 Output Voltage vs Output Current

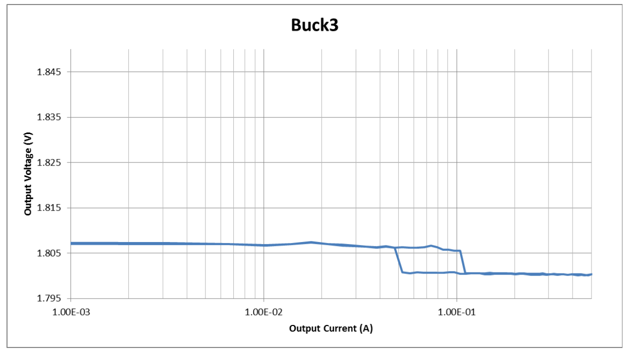


Figure 8. Buck 3, Output Voltage vs Output Current

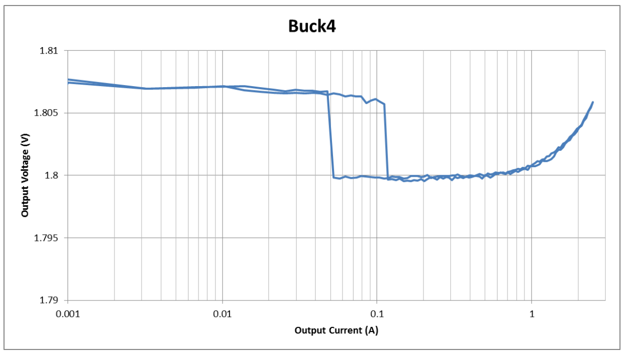


Figure 9. Buck 4, Output Voltage vs Output Current

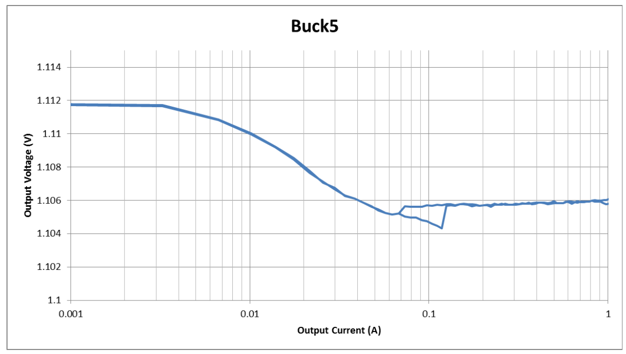


Figure 10. Buck 5, Output Voltage vs Output Current

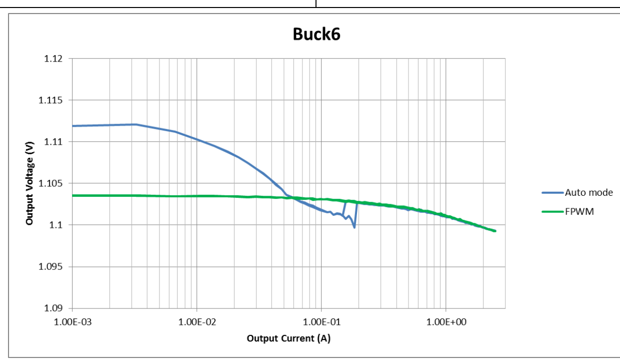


Figure 11. Buck 6, Output Voltage vs Output Current (Default: FPWM)

7.14 Typical Characteristics, Load Transients

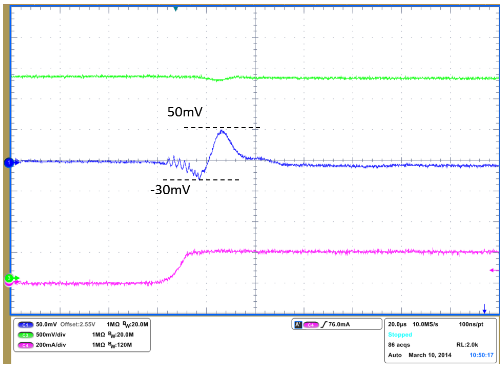


Figure 12. Buck 2 Load Transient, Image 1 of 2

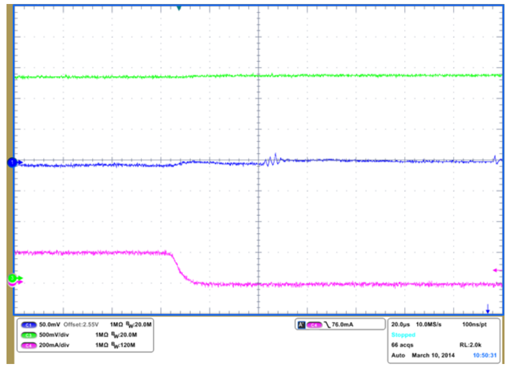


Figure 13. Buck 2 Load Transient, Image 2 of 2

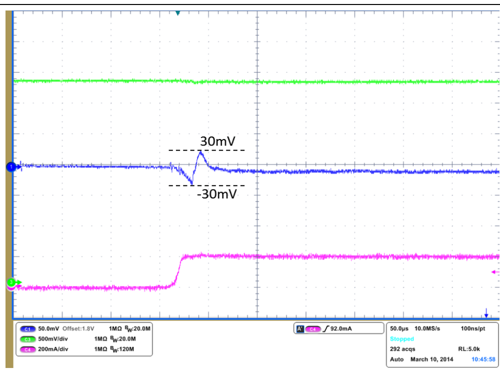


Figure 14. Buck 3 Load Transient, 1 of 2

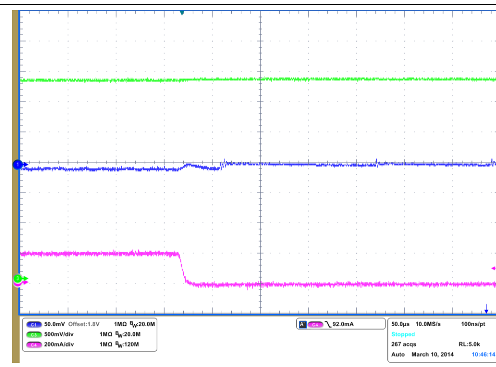


Figure 15. Buck 3 Load Transient, 2 of 2

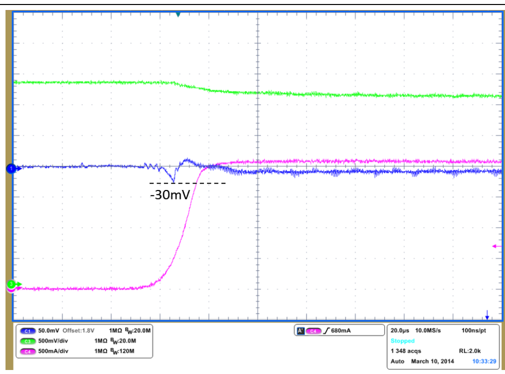


Figure 16. Buck 4 Load Transient, 1 of 2

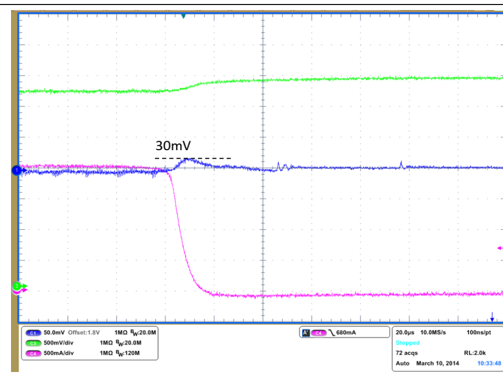


Figure 17. Buck 4 Load Transient, 2 of 2

Typical Characteristics, Load Transients (continued)

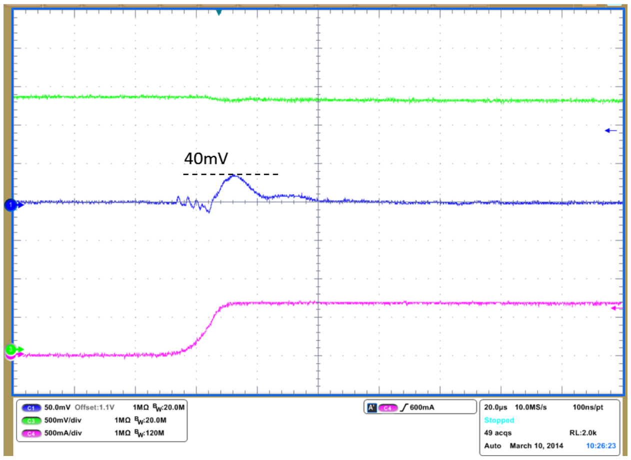


Figure 18. Buck 5 Load Transient, 1 of 2

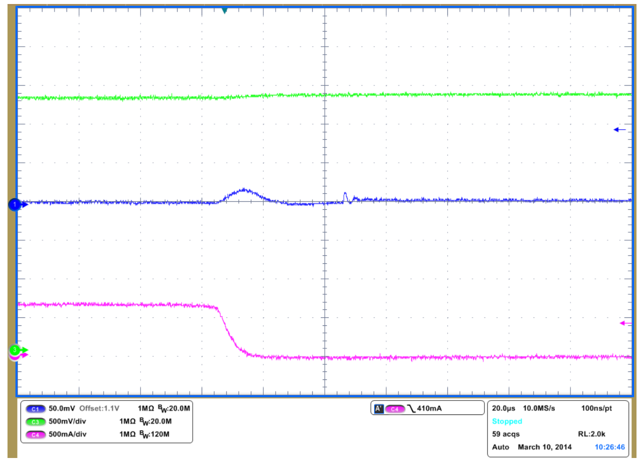


Figure 19. Buck 5 Load Transient Image 2 of 2

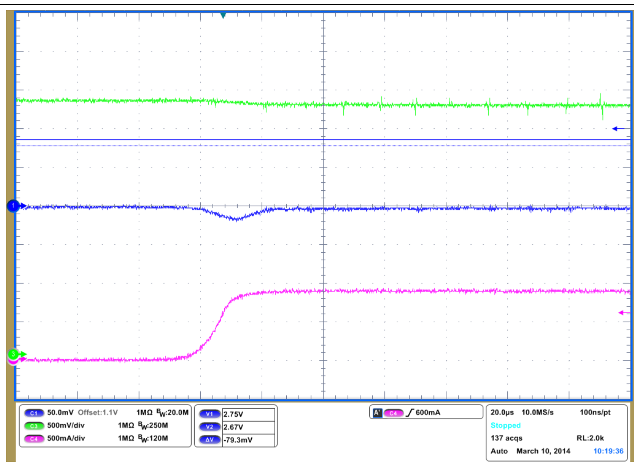


Figure 20. Buck 6 Load Transient (FPWM) Image 1 of 2

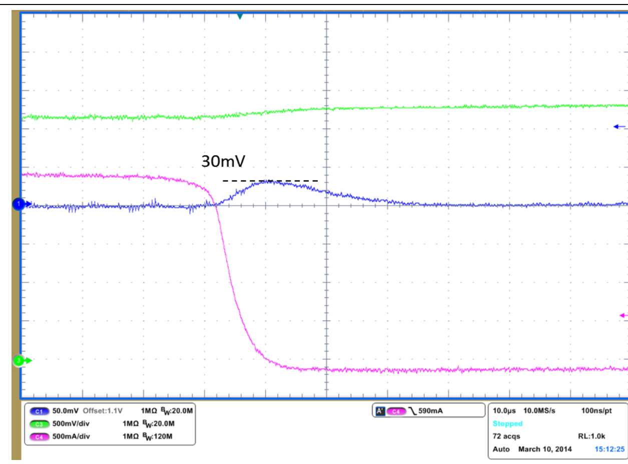


Figure 21. Buck 6 Load Transient (FPWM) Image 2 of 2

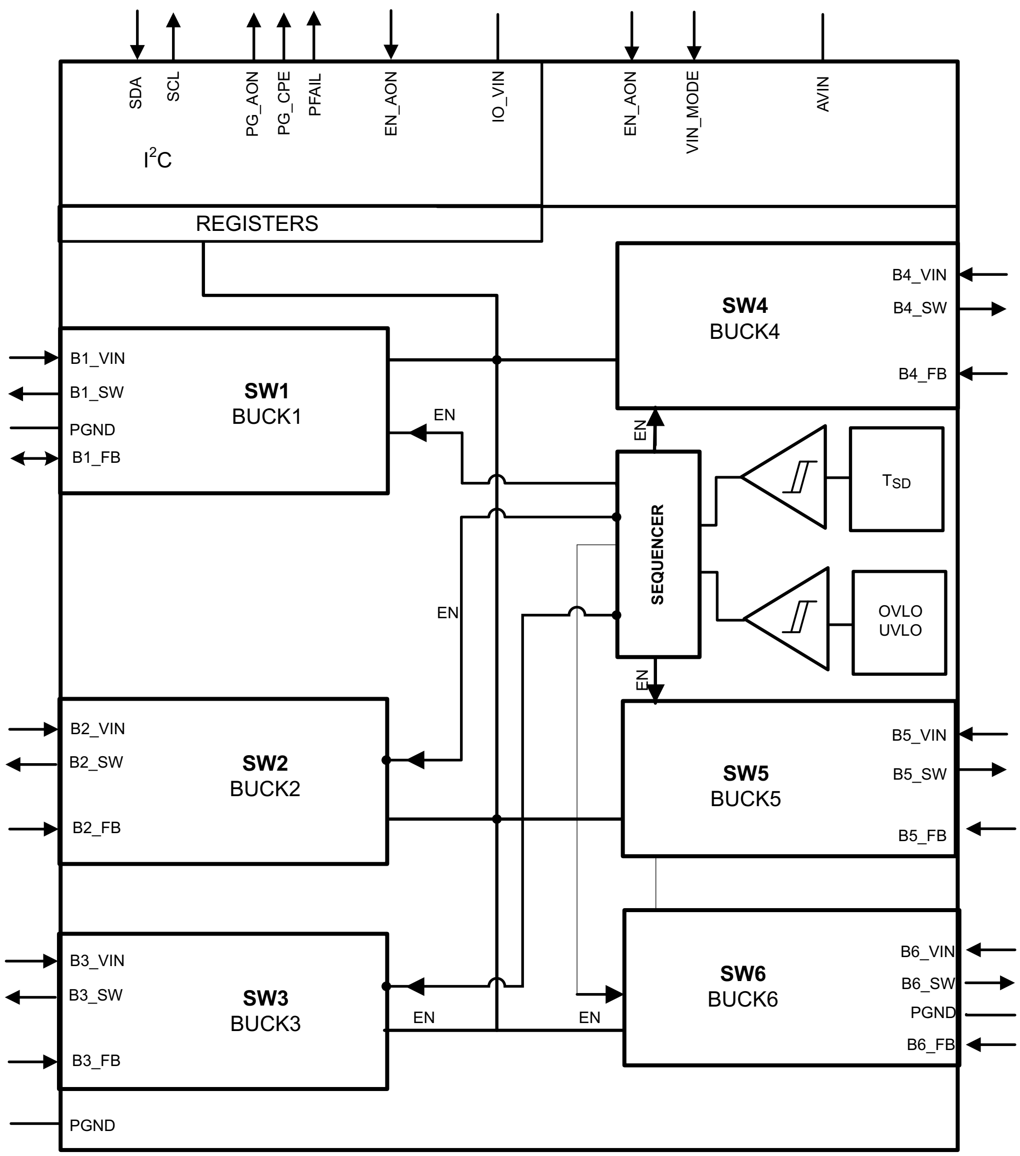
8 Detailed Description

8.1 Overview

LM10692 is a highly efficient and integrated Power Management Unit for Systems-on-a-Chip (SoCs), ASICs, and processors. It operates cooperatively and communicates with ASICs over an I2C compatible serial interface with programmable Regulator Vout, Dynamic Voltage Scaling (DVS), and individual Output Enable/Disable.

The device incorporates six high-efficiency synchronous buck regulators that deliver six output voltages from a single power source.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 UVLO, PFAIL and OVLO

The IC has a default UVLO setting of 2.4V with a hysteresis of 100mV (2.3V when VIN is falling). When VIN rises above this threshold, start-up sequence is initialized and begins 3ms after. PFAIL_N output comes up when VIN rises above 2.7V. There is a delay of 4ms between the time VIN rises above the PFAIL threshold and the PFAIL_N output goes high. There is no delay when VIN falls below the PFAIL threshold.

When VIN rises over the OVLO threshold, the outputs are disabled. PFAIL_N output will not come down during an OVLO event. The outputs are re-enabled in sequence when VIN falls below the OVLO threshold.

The PFAIL_N output needs an IO_VIN voltage of more than 1.0V to be operational. The value of the output is invalid for IO_VIN voltages below 1.0V.

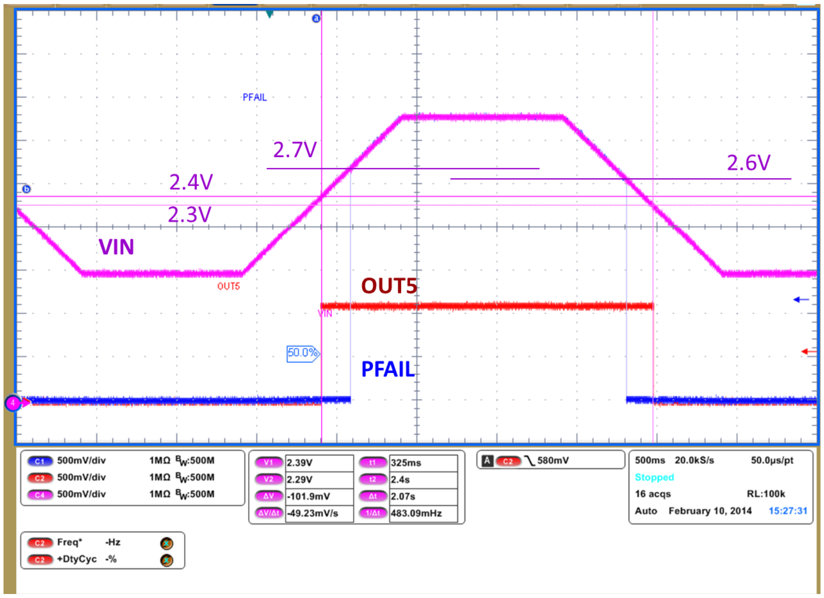


Figure 22. UVLO and PFAIL Thresholds. VIN is Slewed at 1V/s

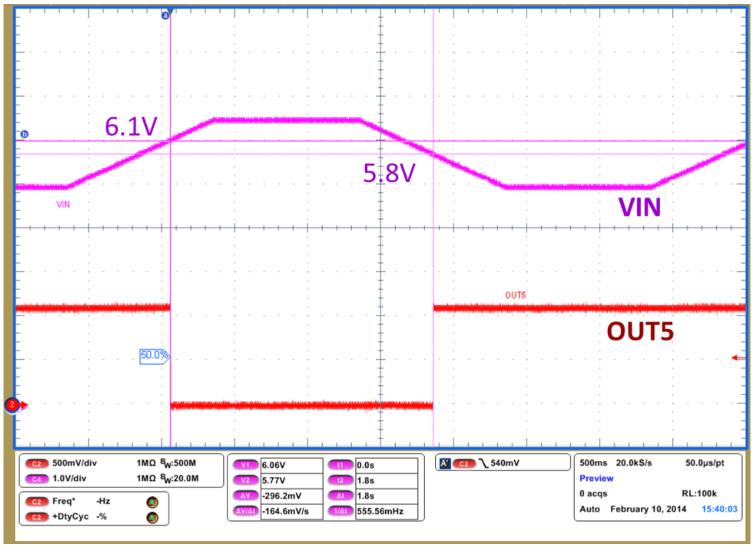


Figure 23. OVLO Thresholds. VIN is Slewed at 1.5V/s

Feature Description (continued)

8.3.2 OCP

When one channel reaches the Over Current Protection threshold, the current will be limited and the output voltage will collapse as a result. The situation remains until the over current event is cleared and the system can resume regulation. The IC will not reset due to an OCP event and the other channels will remain operational. One exception is in the case of OCP on Buck6 or Buck1. Since Buck1 is enabled only when Buck6 is in a Power Good state (output voltage within 90% of set value) and Buck4 is enabled only when Buck1 is in a Power Good state as well, Buck1 and Buck4 will shut-down during OCP events on Buck6. Likewise, Buck4 will shut-down during OCP events on Buck1.

Buck1 OCP is not operational when Buck1 is used as a bypass switch.

Values given in the EC table refer to peak inductor current, not average output current. The average output current threshold will be lower due to the ripple in the inductor current.

The ripple can be estimated with the following formula:

$$\Delta I_L = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times 2 \times 10^6}$$

where

- ΔI_L is the inductor ripple
- L is the inductance (1)

The threshold for the output current will then be:

$$I_{OUT\_MAX} = I_{PEAK} - 0.5 \times \Delta I_L \quad (2)$$

8.3.3 PFAIL_N Operation and Output Thresholds

PFAIL_N is a digital output with open drain. It can be pulled-up up to Vin. When the input voltage drops below the threshold, PFAIL_N turns low within 20us. When the Vin rises above the threshold. PFAIL_N turns high after a delay that is programmable in EPROM (Default is 4ms). By default there is a 100mV hysteresis between the Vin threshold falling and the Vin threshold rising.

The PFAIL_N output needs an IO_VIN voltage of more than 1.0V to be operational. The value of the output is invalid for IO_VIN voltages below 1.0V.

The PFAIL function is operational 2ms after power-up.

The rising and falling thresholds for the PFAIL_N output comparator are independently programmable. This enables the setting of the hysteresis to any desired value within 50mV steps.

Table 1. Register Settings for HOSTMONITOR / PFAIL Rising and Falling Thresholds

N	PFAILN UP_ PFAILN_DN SETTING	THRESHOLD (V)
0	0	3.2
1	1	3.15
2	10	3.1
3	11	3.05
4	100	3
5	101	2.95
6	110	2.9
7	111	2.85
8	1000	2.8
9	1001	2.75
10	1010	2.7
11	1011	2.65
12	1100	2.6

Feature Description (continued)

Table 1. Register Settings for HOSTMONITOR / PFAIL Rising and Falling Thresholds (continued)

N	PFAILN UP_ PFAILN_DN SETTING	THRESHOLD (V)
13	1101	2.55
14	1110	2.5
15	1111	2.45
16	10000	2.4
17	10001	2.35
18	10010	2.3
19	10011	2.3
20	10100	2.3

8.3.4 Power-Up Sequencing and EN_AON and EN_CPE

The EN_AON pin controls the sequenced startup of Always-On rails Buck 5, Buck 3, and Buck 2, each separated by 0.5ms. The EN_CPE pin controls the sequenced startup of core power rails Buck 6, Buck 1, and Buck 4. There is no logical dependency between EN_CPE and EN_AON, and it is expected that any required dependency (for example, EN_CPE must be low when EN_AON is low) between these signals will be enforced externally. Different startup sequences and timing are possible via factory trim. However, there is a fixed dependency for the CPE rails (Buck1, Buck4, Buck6): Buck6 must be up and running for Buck1 to start-up. Likewise, Buck1 needs to be up and running (in bypass mode or in buck mode) for Buck4 to start-up.

During the initial Power-up sequence, the controller checks all the internal Power Good flags. If all the PG flags (Buck1-Buck6) are not high 8ms after the last programmed buck has begun soft-start, the IC will power-down and wait 200ms before restarting. This means that EN_CPE must be high during the power-up sequence. Once all the PGs have been asserted, EN_CPE can be toggled low at will.

The startup timing of the rails controlled by EN_CPE is different depending on whether EN_CPE goes high during the initial startup sequence upon power-up, or during wake-up from a sleep mode. In the case where EN_CPE goes high during the initial startup, the startup of Buck 6, Buck1, and Buck4 are delayed by 500us (or longer depending on the soft-start time of each buck). In the case where it is waking up from a sleep mode, the startups are only delayed by the PGOOD of the previous rail, so the timing is dependent on the soft-start time of the rails which may be 100us to 1000us.

EN_AON controls Buck5, Buck3 and Buck2. When EN_AON is toggled high, Buck5, Buck3 and Buck2 will power-up in sequence (5->3->2). When EN_AON is toggled low, all six rails (Buck1-Buck6) will power-down at the same time regardless of the state of the EN_CPE pin.

When EN_AON is toggled back high, EN_CPE needs to be set high too for the system to re-start properly as in the power-up sequence.

EN_CPE controls Buck6,Buck1 and Buck4. When EN_CPE is toggled high, Buck6, Buck1 and Buck4 will power-up in sequence (6->1->4). When EN_CPE is toggled low, all three rails will shut-down at the same time.

Voltage at IO_VIN pin is not necessary for the AON rails to power-up. However IO_VIN needs to be supplied with a proper voltage for the CPE rails to power-up.

Each channel has an active discharge circuitry which will discharge the output into an 18-20Ω internal resistance when the channel is turned-off in order to quickly lower the output voltage as needed by the SSD circuits before being able to power up again. This will enable the user to toggle EN_CPE off and back on within a few milliseconds. The discharge time of the output rails is dependant on the output capacitance used.

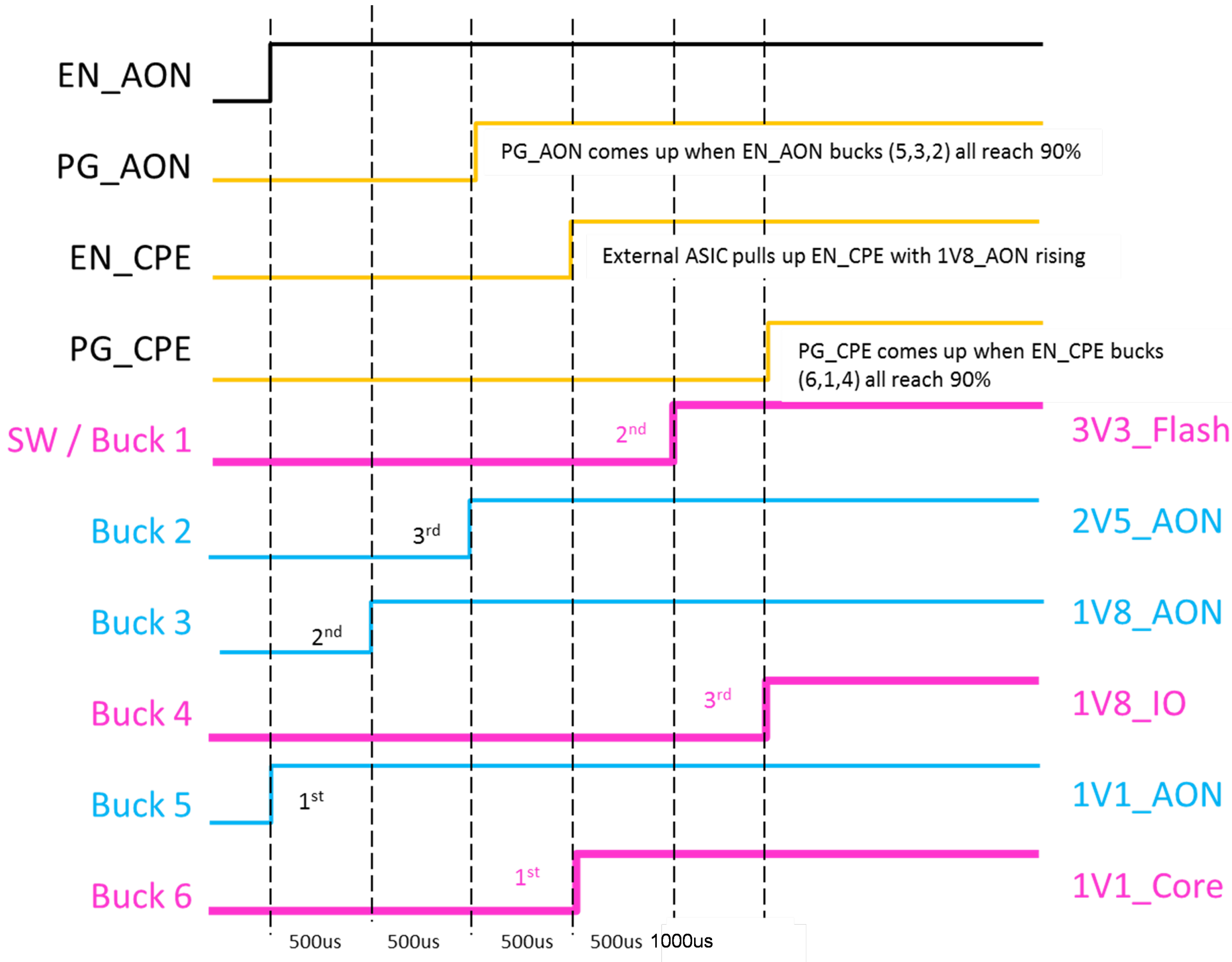


Figure 24. Power-up Sequence with EN_AON and EN_CPE, where EN_CPE is Tied to 1V8_AON.

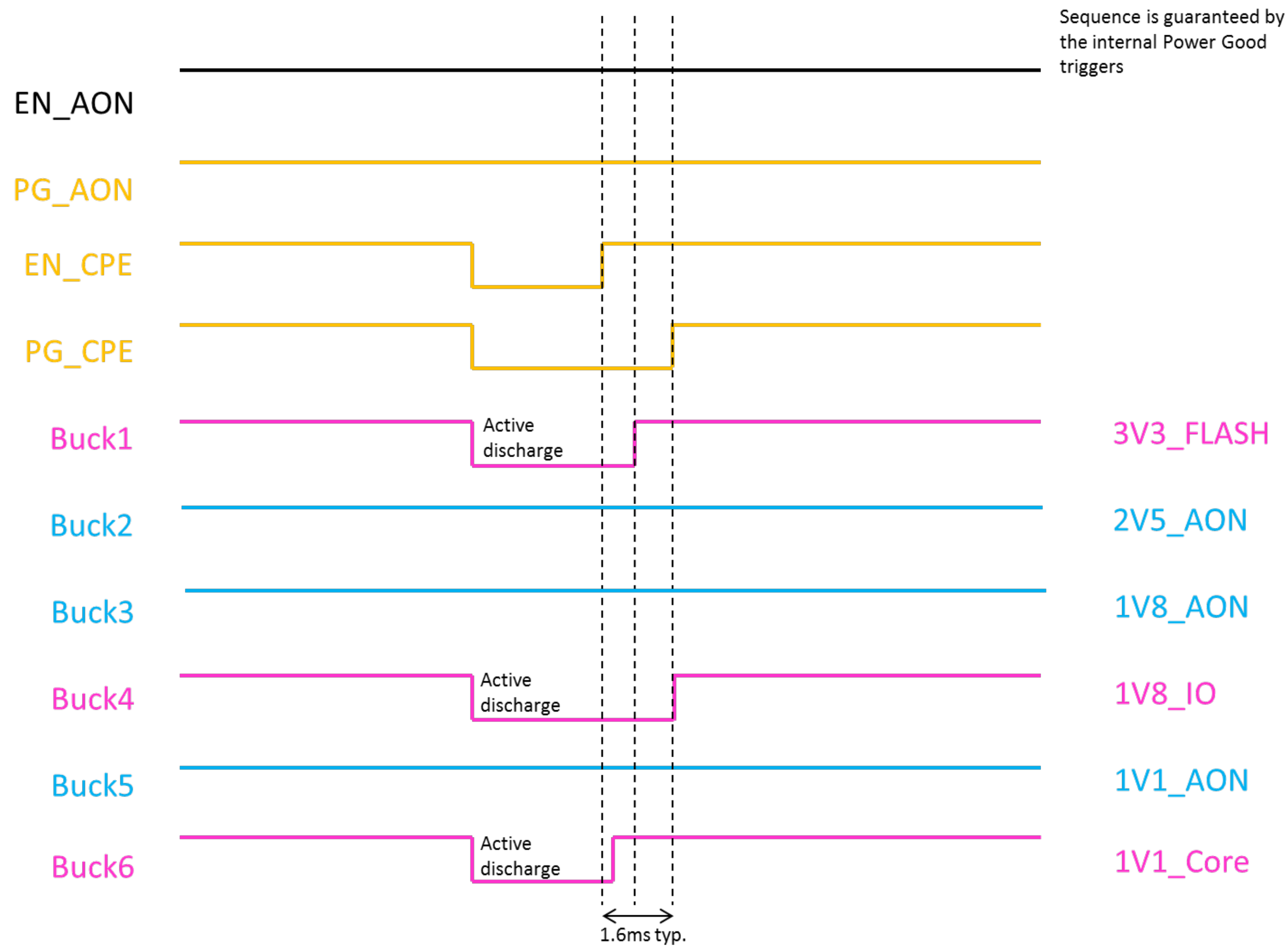


Figure 25. Wake-up Sequence from EN_CPE

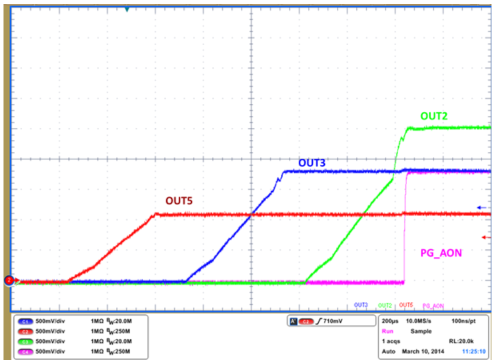


Figure 26. AON Rails Power-up

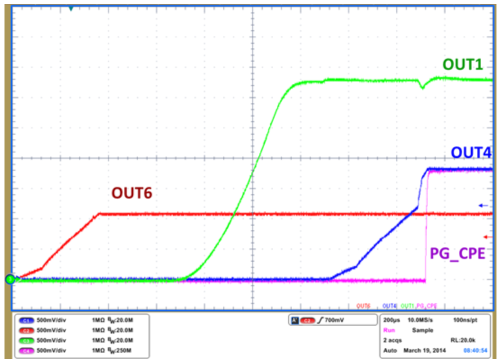


Figure 27. CPE Rails Power-up

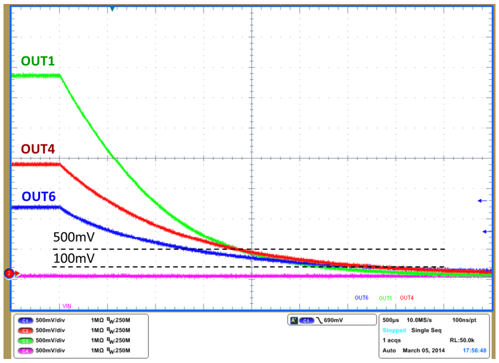


Figure 28. EN_CPE Toggle Off

8.3.5 Low Power Operation

When the output current is low, each converter operates in PFM with a hysteretic pattern to limit the amount of switching event to a minimum and keep the current consumption lower. Buck1 and Buck6 are programmed to operate in PWM mode all the time.

This mode can be overridden by the user with specific I2C commands (Specification ensured by design. Not tested during production). However, the default programmed mode will be reloaded upon reset.

8.4 Device Functional Modes

8.4.1 Soft Start

8.4.1.1 Buck Mode

During power-up or when EN_AON or EN_CPE is toggled high, the bucks will turn on following a three steps soft-start pattern. Each step lasts 125us and consist of a constant average inductor current. The output voltage rise in a set of ramps as the output capacitor is being charged. If the set output voltage is reached prior to all the steps being completed, the soft-start period will be over. After the 375us soft-start period has elapsed, the full current (limited by the OCP setting for that buck converter) is allowed into the inductor regardless of the state of the output voltage.

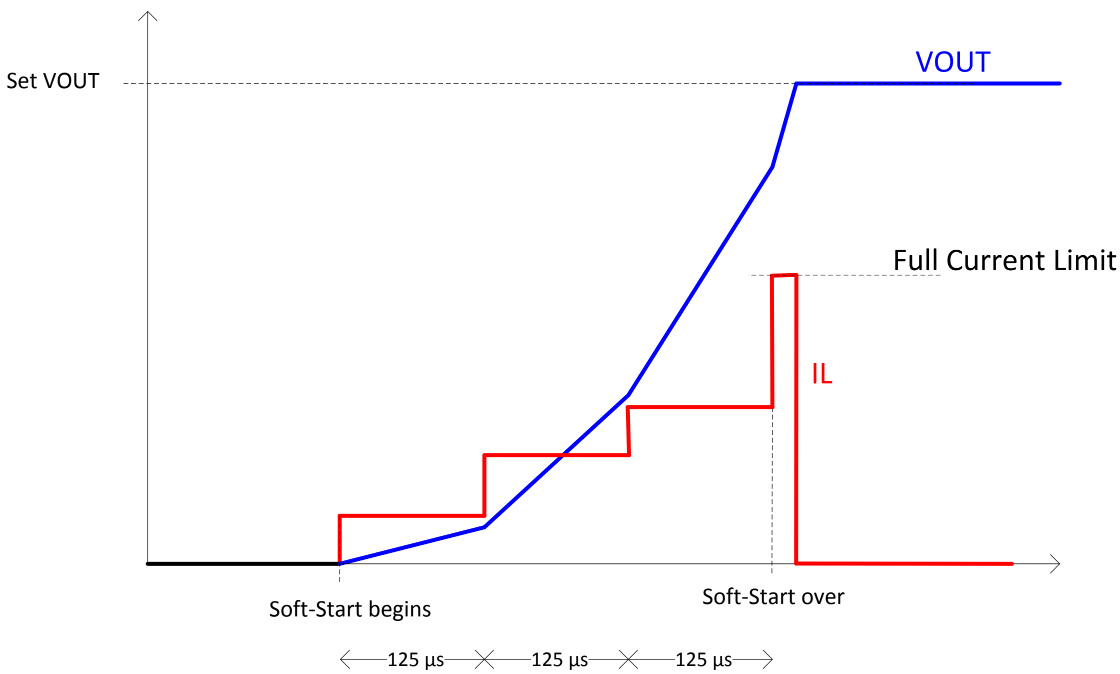


Figure 29. Typical Soft-Start Pattern

It is preferable to ensure that the output voltage will be reached before the Soft-Start period is over. If not, in-rush current spike might be observed on the input. That spike depends on input capacitor, output capacitor and output voltage but is typically 1A to 2A in magnitude.

For higher output capacitances, the output voltage will rise more slowly. Also, for higher output voltage settings, the desired output voltage will be reached less quickly. Hence depending on the output voltage, the output capacitance might have to be limited if in-rush current is a concern.

8.4.1.2 Bypass Mode

If Buck1 is programmed as a bypass mode, the gate of the internal High Side switch will be gradually increased to ensure a soft-start pattern. After the HS switch has fully turned ON, the internal PG signal will come up and the additional bypass switch between the input and the FB1 pin will turn-ON to help reduce the resistance and voltage drop across the switch.

Device Functional Modes (continued)

8.4.2 VIN_MODE and Buck1 Bypass Operation

The VIN_MODE input pin defines the behavior of Buck1 and the thresholds for the PFAIL comparator.

The VIN_MODE pin function is sensed only when the converter powers-up.

Table 2. VIN_MODE and Buck1 Bypass Operation

VIN_MODE	BUCK1 BEHAVIOR
VIN_MODE floating	Buck1 will always be in bypass mode when it is enabled. OUT1 is not regulated. In this mode, it operates as a load switch and does not require an inductor.
VIN_MODE tied to GND not recommended if Vout>0.8Vin	Buck1 regulates OUT1 to the VREF1 target. If VIN drops below a threshold, Buck1 will automatically enter bypass mode.

The state of this pin is defined at startup of PMIC and changes in state afterwards are ignored.

The LM10692 is mainly designed to interact with the SF3700 controller. For this purpose, it should operate with VIN_MODE pin floating and Buck1 operating as a switch, with FB connected directly to the B1_SW pin for reduced ON resistance.

Buck1 has a bypass FET integrated in the IC that connects B1_VIN directly to B1_FB. When VIN_MODE is floating, Buck1 will always be in bypass mode when it is enabled, and OUT1 is not regulated. In this mode, Buck1 operates as a load switch with the bypass FET (on the FB node) and high-side PFET (on the buck switch node) both carrying current, and Buck1 does not require an inductor.

When the VIN_MODE pin is set to GND, Buck1 will regulate the output to the reference set by the Buck1 voltage code.

If the input voltage drops and the output cannot be regulated anymore, the output will then switch into bypass mode and keep both the high-side PFET and bypass FET ON to minimize the resistance and reduce the drop on the output voltage. The bypass FET provides a low resistance path around the inductor, and will carry the majority of the current.

Since there may be potentially high currents being passed through the B1_FB pin, the traces for this particular feedback path should be made thicker than for a conventional feedback pin.

When operating with VIN = 3.3V, it is recommended that VIN_MODE be left floating and that Buck1 be operated as a load switch. This shrinks the solution size and cost by enabling the user to remove the inductor for this output. If VIN_MODE is tied GND, care must be taken to ensure that the required output voltage (typically 2.85V for a Flash rail) can be met for the specified worst case VIN, which can be as low as 2.97V (-10% of 3.3V). Transient performance specs are also difficult to meet at these operating points due to the very high duty cycle operation. In order to meet performance specifications at worst case temperatures and max currents, a larger inductor with lower DC resistance (DCR) may be needed.

8.5 Programming

8.5.1 I^{2}C Interface

Control of LM10692 is done via I^{2}C compatible interface.

8.5.1.1 I^{2}C Signals

In I2C-compatible mode, the SCL pin is used for the I2C clock and the SDA pin is used for the I2C data. Both these signals need a pull-up resistor according to I2C specification. The values of the pull-up resistors are determined by the capacitance of the bus. See I2C specification from Philips for further details. Signal timing specifications are according to the I2C bus specification. Maximum frequency is 1MHz.

8.5.1.2 I^{2}C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

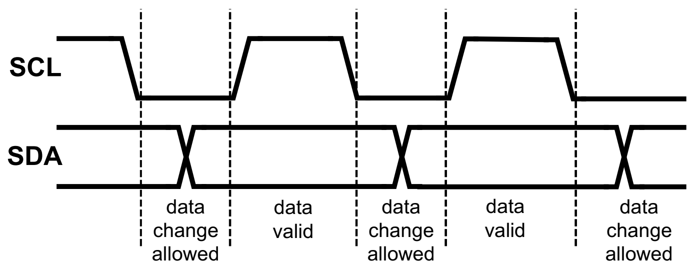


Figure 30. I^{2}C Signals – Data Validity

8.5.1.3 I2C Start and Stop Conditions

START and STOP bits classify the beginning and the end of the I2C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I2C master always generates START and STOP bits. The I2C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I2C master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

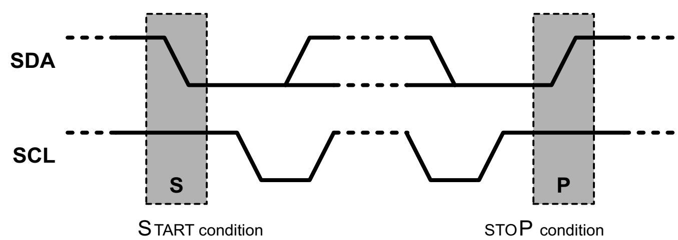


Figure 31. Start and Stop Conditions

8.5.1.4 Transferring Data

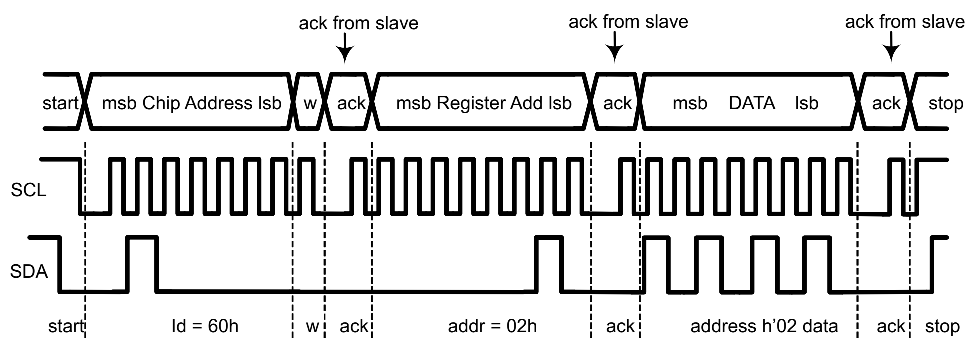
Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. All clock pulses are generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the ninth clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I2C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM10692 address is 0x60. The eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Programming (continued)

8.5.1.5 Chip Address: 0x60H

Figure 32. I^{2}C Chip Address



A. w = write (SDA = "0")

B. r = read (SDA = "1")

C. ack = acknowledge (SDA pulled down by either master or slave)

D. rs = repeated start

E. id = chip address

Figure 33. I^{2}C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform below:

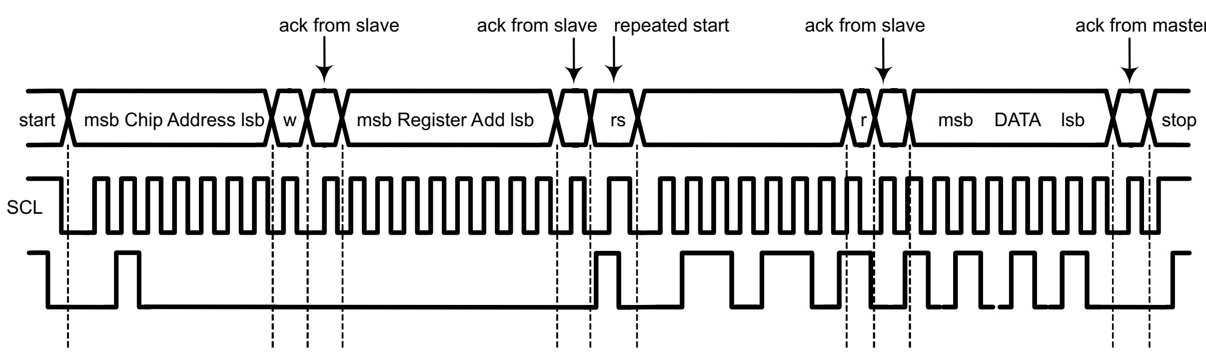


Figure 34. I^{2}C Read Cycle

8.6 Register Maps

The following table summarizes the register accessible through I2C. The content of these registers is erased at power-up and the default values are loaded from the EPROM.

Table 3. I2C Register Summary

ADDRESS (HEX)	ID	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	USER 00				Buck6 Voltage Code [4]	Buck6 Voltage Code [3]	Buck6 Voltage Code [2]	Buck6 Voltage Code [1]	Buck6 Voltage Code [0]
1	USER 01				Buck5 Voltage Code [4]	Buck5 Voltage Code [3]	Buck5 Voltage Code [2]	Buck5 Voltage Code [1]	Buck5 Voltage Code [0]
2	USER 02				Buck4 Voltage Code [4]	Buck4 Voltage Code [3]	Buck4 Voltage Code [2]	Buck4 Voltage Code [1]	Buck4 Voltage Code [0]
3	USER 03				Buck3 Voltage Code [4]	Buck3 Voltage Code [3]	Buck3 Voltage Code [2]	Buck3 Voltage Code [1]	Buck3 Voltage Code [0]
4	USER 04				Buck2 Voltage Code [4]	Buck2 Voltage Code [3]	Buck2 Voltage Code [2]	Buck2 Voltage Code [1]	Buck2 Voltage Code [0]
5	USER 05				Buck1 Voltage Code [4]	Buck1 Voltage Code [3]	Buck1 Voltage Code [2]	Buck1 Voltage Code [1]	Buck1 Voltage Code [0]
6	USER 06								
7	USER 07			Buck1 Enable	Buck2 Enable	Buck3 Enable	Buck4 Enable	Buck5 Enable	Buck6 Enable
8	USER 08			Buck1 Force PWM	Buck2 Force PWM	Buck3 Force PWM	Buck4 Force PWM	Buck5 Force PWM	Buck6 Force PWM
9	USER 09								
A	USER 10	POWER GOOD (read only)		Buck1 OK (read only)	Buck2 OK (read only)	Buck3 OK (read only)	Buck4 OK (read only)	Buck5 OK (read only)	Buck6 OK (read only)
B	USER 11	TSD Fault (read only)				CHIP REV [3]	CHIP REV [2]	CHIP REV [1]	CHIP REV [0]
C	USER 12						Oscillator Enable		

8.6.1 Address 0x00-0x05: USER 00 – USER 05:

USER00-USER05 registers set the reference voltage of each buck converter. See the tables regarding the mapping of the register values to the corresponding output voltage at the end of this datasheet.

8.6.2 Address 0x07: USER 07:

This register allows the user to turn on or off a specific buck regulator.

When a buck converter is re-enabled using I2C it will not follow the usual Soft-Start pattern. Instead VREF is stepped up from its minimum voltage (according to code 0x1F from the voltage code tables) each 20 µs until the set output voltage code is reached. The buck will also follow the usual current limited soft-start pattern as described in the soft-start section of this datasheet but in typical cases, the soft-start time will now be dictated by the VREF ramp time. (20 µs per step). For example on Buck4 with Vout4 = 1.8 V, the usual soft-start time is less than 200 µs. When enabled through I2C the soft-start time becomes 400 µs (20 steps from 1.1V to 1.8V).

NOTE

The internal enable circuitry of Buck1 and Buck4 are also determined by the internal Power Good signals of Buck6 and Buck1 respectively. This means that if Buck1 is shutdown for any reason, Buck4 will shutdown too regardless of the state of the Enable flag for Buck4. Likewise, shutting down Buck6 will turn Buck1 off (and as a ripple effect, Buck4 off too).

8.6.3 Address 0x08: USER 08:

This register allows the user to force PWM operation of each converter regardless of the load. The converters will not switch to PFM operation at light load. This results in increased current draw at light load due to switching losses compared to the regular light-load PFM regulation.

8.6.4 Address 0x0A: USER 10:

This register is read-only and displays the internal Power Good signals of each converter as well as the global Power Good signal.

8.6.5 Address 0x0B: USER 11:

This register display the Temperature Shutdown flag on bit7 as well as the chip revision ID on bits 0-3.

8.6.6 Address 0x0C: USER 12:

8.6.6.1 Oscillator Enable (bit 2)

Oscillator Enable bit allows the unit to enter Sleep mode. In this mode, internal circuitries are shut-down to minimize quiescent current. All the BUCK converters are still active.

This mode should only be entered if all the bucks are operating in PFM mode (light load). If a Buck converter tries to enter PWM operation when the IC is in sleep mode (in response to a load increase), its output voltage will collapse.

The internal I2C accessible PG flags do not operate in Sleep mode. Converters cannot be enabled or disabled in Sleep mode. Voltages cannot be changed via I2C.

External flags PG_CPE and PG_AON are still operational in Sleep mode.

Table 4. BUCK 1: Voltage Code and Vout Level Mapping - 50 mV Steps

VOLTAGE CODE	VOLTAGE
0x00	3.30
0x01	3.25
0x02	3.20
0x03	3.15
0x04	3.10
0x05	3.05
0x06	3.00
0x07	2.95
0x08	2.90
0x09	2.85
0x0A	2.80
0x0B	2.75
0x0C	2.70
0x0D	2.65
0x0E	2.60
0x0F	2.55
0x10	2.50
0x11	2.45
0x12	2.40
0x13	2.35
0x14	2.30
0x15	2.25
0x16	2.20
0x17	2.15
0x18	2.10
0x19	2.05
0x1A	2.00
0x1B	1.95
0x1C	1.90
0x1D	1.85
0x1E	1.80
0x1F	1.75

Table 5. BUCK 2: Voltage Code and Vout Level Mapping - 50 mV Steps

VOLTAGE CODE	VOLTAGE
0x00	2.55
0x01	2.50
0x02	2.45
0x03	2.40
0x04	2.35
0x05	2.30
0x06	2.25
0x07	2.20
0x08	2.15
0x09	2.10
0x0A	2.05
0x0B	2.00
0x0C	1.95
0x0D	1.90
0x0E	1.85
0x0F	1.80
0x10	1.75
0x11	1.70
0x12	1.65
0x13	1.60
0x14	1.55
0x15	1.50
0x16	1.45
0x17	1.40
0x18	1.35
0x19	1.30
0x1A	1.25
0x1B	1.20
0x1C	1.15
0x1D	1.10
0x1E	1.05
0x1F	1.00

Table 6. BUCK 3/BUCK4: Voltage Code and Vout Level Mapping - 50 mV Steps

VOLTAGE CODE	VOLTAGE
0x00	2.35
0x01	2.30
0x02	2.25
0x03	2.20
0x04	2.15
0x05	2.10
0x06	2.05
0x07	2.00
0x08	1.95
0x09	1.90
0x0A	1.85
0x0B	1.80
0x0C	1.75
0x0D	1.70
0x0E	1.65
0x0F	1.60
0x10	1.55
0x11	1.50
0x12	1.45
0x13	1.40
0x14	1.35
0x15	1.30
0x16	1.25
0x17	1.20
0x18	1.15
0x19	1.10
0x1A	1.05
0x1B	1.00
0x1C	0.95
0x1D	0.90
0x1E	0.85
0x1F	0.80

Table 7. BUCK 5/BUCK 6: Voltage Code and Vout Level Mapping - 25 mV Steps

VOLTAGE CODE	VOLTAGE
0x00	1.575
0x01	1.550
0x02	1.525
0x03	1.500
0x04	1.475
0x05	1.450
0x06	1.425
0x07	1.400
0x08	1.375
0x09	1.350
0x0A	1.325
0x0B	1.300
0x0C	1.275
0x0D	1.250
0x0E	1.225
0x0F	1.200
0x10	1.175
0x11	1.150
0x12	1.125
0x13	1.100
0x14	1.075
0x15	1.050
0x16	1.025
0x17	1.000
0x18	0.975
0x19	0.950
0x1A	0.925
0x1B	0.900
0x1C	0.875
0x1D	0.850
0x1E	0.825
0x1F	0.800

9 Application and Implementation

9.1 Application Information

9.2 Typical Application

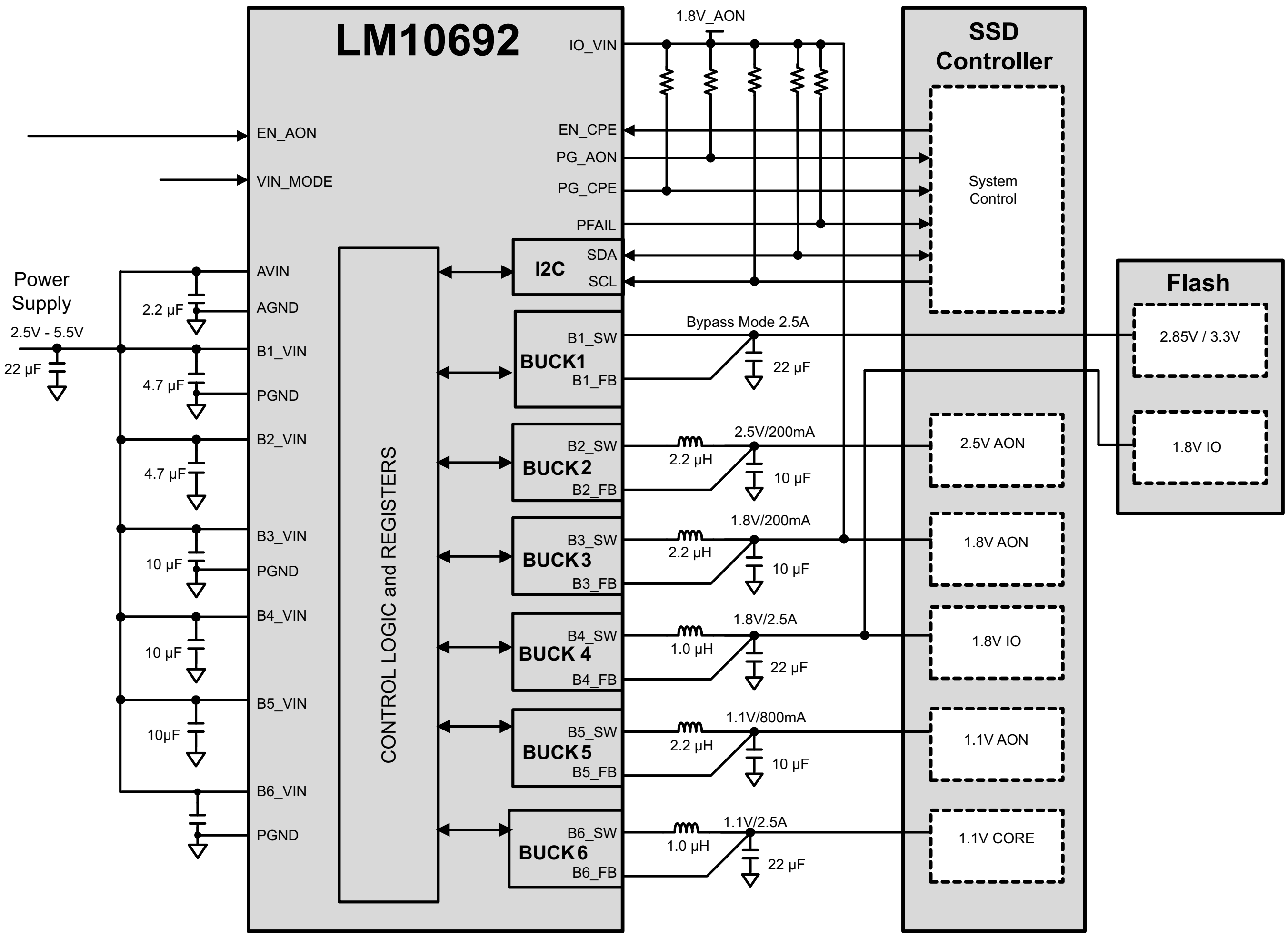


Figure 35. Typical Application Circuit

9.2.1 Design Requirements

The application needs to be able to operate with the default output voltages. Output voltages can be changed through I2C after start-up but the power-up levels will always be the default values.

Load current needs to be defined in order to ideally size the inductor and the capacitors. Inductors need to be sized in order to handle the full expected load current (saturation and heat dissipation wise) as well as the peak current generated during load transient and start-up. In rush current at start-up will depend on the output capacitor selection and vary for each channels. The section below will help the user to select a value of output capacitor to minimize the in-rush current during power-up.

The user needs to ensure that EN_CPE is up during power-up, even if the pin is not actively driven. If the EN_CPE is not up early during the sequence, the PMIC will reset and re-atempt to restart. Once all the rails are up, EN_CPE can be driven high or low as needed

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor

It is important to ensure the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current. Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

The following inductors are recommended for the use in LM10692 applications. In general we recommend the use of high performance inductor with a soft-saturation behavior in the circuit in order to optimize efficiency and space while offering adequate response to currents up to the peak OCP levels.

Table 8. Recommended Inductors for LM10692

PART NUMBER	MANUFACTURER	USE
MAMK2520-1R0	Taiyo-Yuden	B4,B6
PIFE20161T-1R0	Cyntec	B4,B6
IFSC0806AZ2R2	Vishay	B2,B3,B5
PIFE20161T-2R2	Cyntec	B2,B3,B5
MAKK2016T2R2M	Taiyo-Yuden	B5
MAKK2016T1R0M	Taiyo-Yuden	B4
MDKK1616T2R2M	Taiyo-Yuden	B2,B3,B5

9.2.2.2 Output Capacitor

The channels on the LM10692 are designed to work with 22µF of output capacitance. Extra capacitance can be added up to 100µF to improve transient performance. Depending on the output voltage, the extra capacitance can result in increase in-rush current during start-up. Typical peak in-rush current levels for switching bucks with 22µF output capacitance are within 200mA. With added capacitance the in-rush current increases.

As described in the soft-start section, the start-up sequence comprises of three steps with fixed output current levels, each 125µs long. The current level for each of these steps is summarized in the table below.

Table 9. Soft-Start Charging Current

	Step1	Step2	Step3
Buck1 (in buck mode)	0.17A	0.48A	0.48A
Buck2	0.25A	0.43A	0.65A
Buck3	0.2A	0.4A	0.4A
Buck4	0.2A	0.5A	0.9A
Buck5	0.3A	0.4A	0.4A
Buck6	0.3A	0.7A	0.7A

If the output voltage is not reached by the end of the soft-start sequence, a current spike will be seen on the input as the converter rushes to finish charging the output capacitors as fast as possible.

Assuming no or very light load on the output, the recommended maximum capacitance to limit in-rush current for each bus can be defined by:

$$C_{OUT} = \frac{(I_{step1} + I_{step2} + I_{step3}) \cdot 125 \cdot 10^{-6}}{V_{OUT}}$$

where

- I_{step} is the current of the given soft start step
- V_{OUT} the final output voltage (3)

For the default output voltage this means the recommended maximum output capacitance is:

Table 10. Output Capacitor Selection

	Output Voltage	Max. Output Capacitor
Buck1 (in buck mode)	2.85V	50µF
Buck2	2.5V	66µF
Buck3	1.8V	69µF
Buck4	1.8V	104µF
Buck5	1.1V	125µF
Buck6	1.1V	193µF

For Buck5 and Bucl6, we recommend capacitance of less than 110µF for stability reasons

9.2.2.3 Input Capacitor Selection

Input Capacitor selection For typical applications a 10µF at the input of the high current bucks (Buck4, Buck5, Buck6 and Buck1 in buck mode) should be sufficient. For lower current channels (Buck2 and Buck3) a 4.7µF is sufficient. More input capacitance can be added on the inputs to reduce in-rush current during soft-start of the channels.

9.2.3 Application Curves

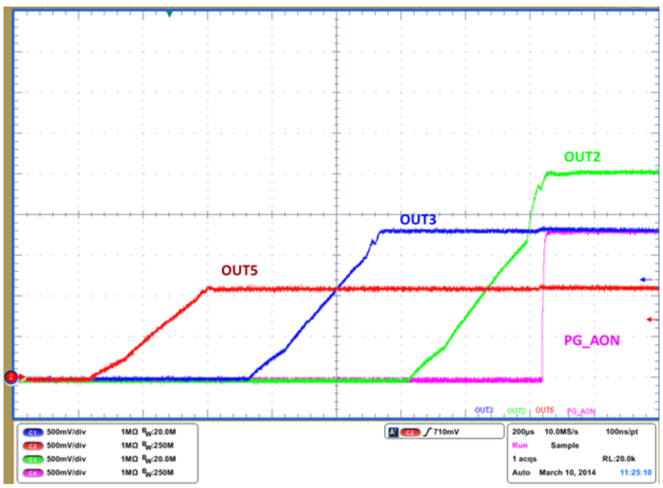


Figure 36. Startup of the AON rails

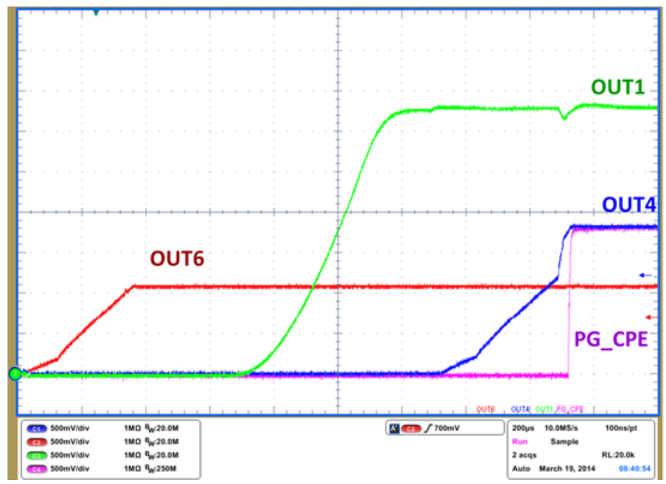


Figure 37. Startup of the CPE rails

10 Power Supply Recommendations

The device contains six programmable buck converters. Table 11 lists the output characteristics of the power regulators.

10.1 Supply Overview

Table 11. Output Characteristics of the Power Regulators

REGULATOR	Vout DEFAULT	Vout PROGRAMMABLE	OUTPUT CURRENT	VOLTAGE STEP INCREMENT
				DEFAULT
Buck 1	2.85V	1.75 – 3.3V	2.5A	50mV
Buck 2	2.5V	1.0 – 2.55V	200mA	50mV
Buck 3	1.80V	0.8 – 2.35V	200mA	50mV
Buck 4	1.80V	0.8 – 2.35V	2.5A	50mV
Buck 5	1.10V	0.8 – 1.575V	800mA	25mV
Buck 6	1.10V	0.8 – 1.575V	2.5A	25mV

11 Layout

11.1 Layout Guidelines

Proper layout of the PCB is critical to the proper operation of the IC. A compact layout will yield better performances as well as an overall reduced footprint for the solution.

Of prime importance is the location of the input capacitors. Those need to be close to the IC’s power input they are assigned to in order to reduce the parasitic inductance between the input and the power rails inside the IC.

The output capacitors should be connected close to the GND of the input capacitors of the same channel. This is because current flows from the input capacitor (through the inductor) to the output capacitor and the load during the part of the switching cycle when the HS FET is ON.

Inductors should be close to the switch nodes. The path from the switch node pin and the inductor pad should be minimized. It is a good practice to keep the PCB from having any copper such as ground planes underneath the inductor pad on the switch node side to reduce switch node capacitance. Increased switch node capacitance can lead to lower efficiency as it increases the turn-on and turn-off time of the FET and thereby increases switching losses.

Signal traces should avoid crossing underneath the switch node traces and pads or passing between the inductor’s pads in order to avoid noise from the switch node and the magnetic components to couple into these lines. This applies particularly to the feedback lines.

To increase thermal conductivity and help carry heat away from the IC, the planes should have as large surfaces as possible, which is applicable in particular to PVIN and GND with regard to the IC. This also applies to the six outputs lines in order to spread the heat generated on each of the inductors.

11.2 Layout Example

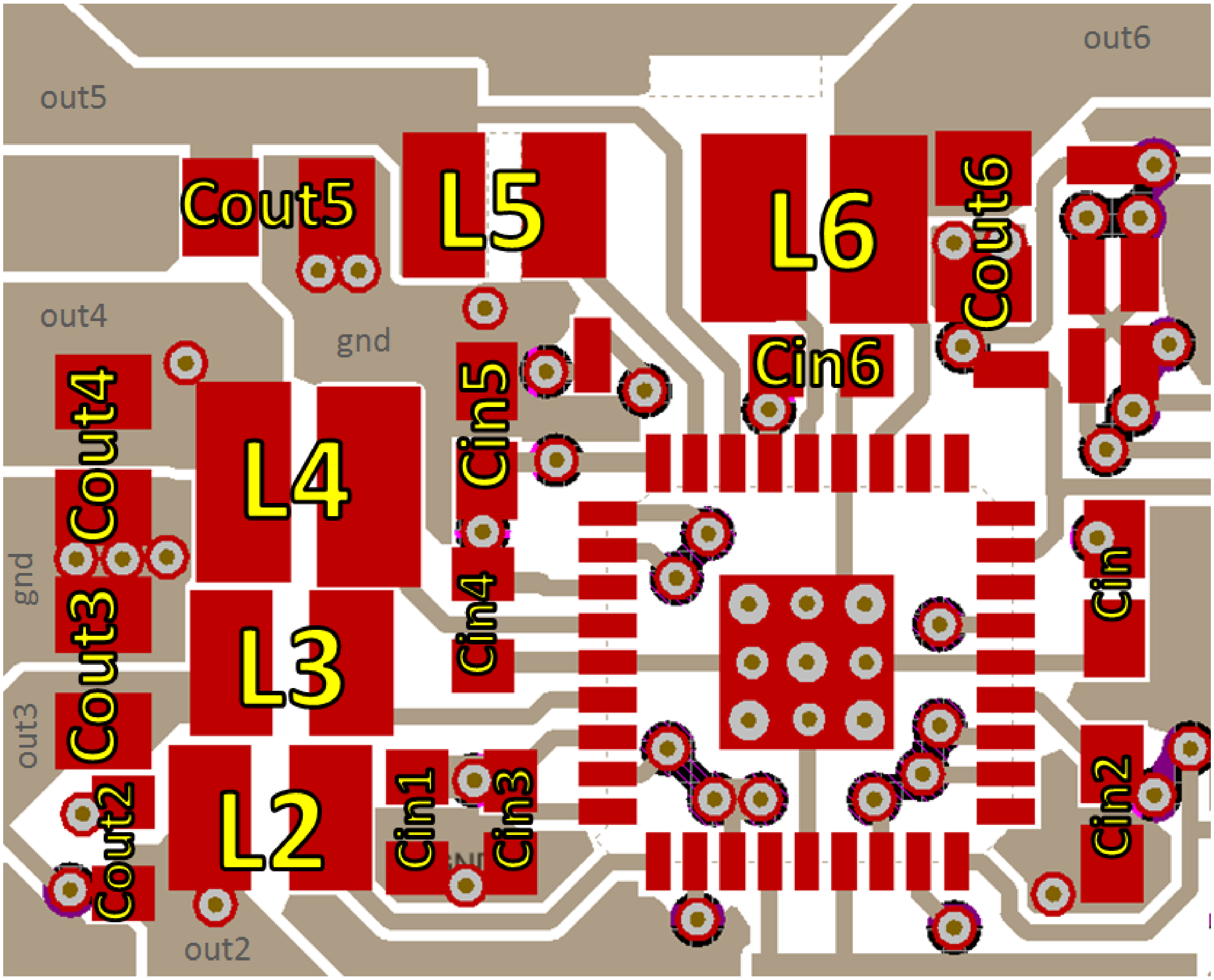


Figure 38. LM10692 Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10692BRMYR	ACTIVE	VQFN-HR	RMY	36	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	10692B A1	Samples
LM10692BRMYT	ACTIVE	VQFN-HR	RMY	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	10692B A1	Samples
LM10692RMYR	ACTIVE	VQFN-HR	RMY	36	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM10692 A1	Samples
LM10692RMYT	ACTIVE	VQFN-HR	RMY	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM10692 A1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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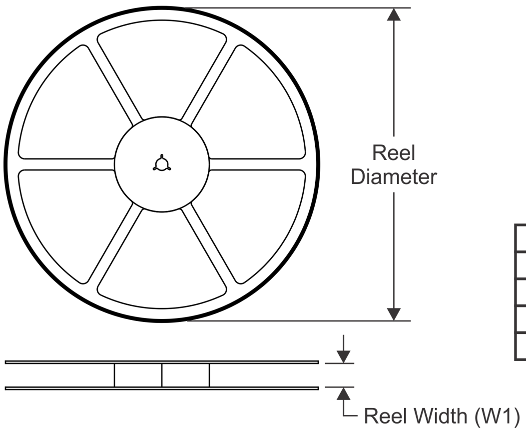
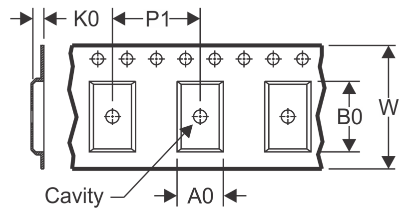
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

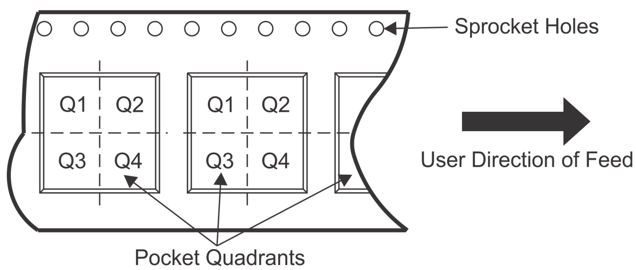


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

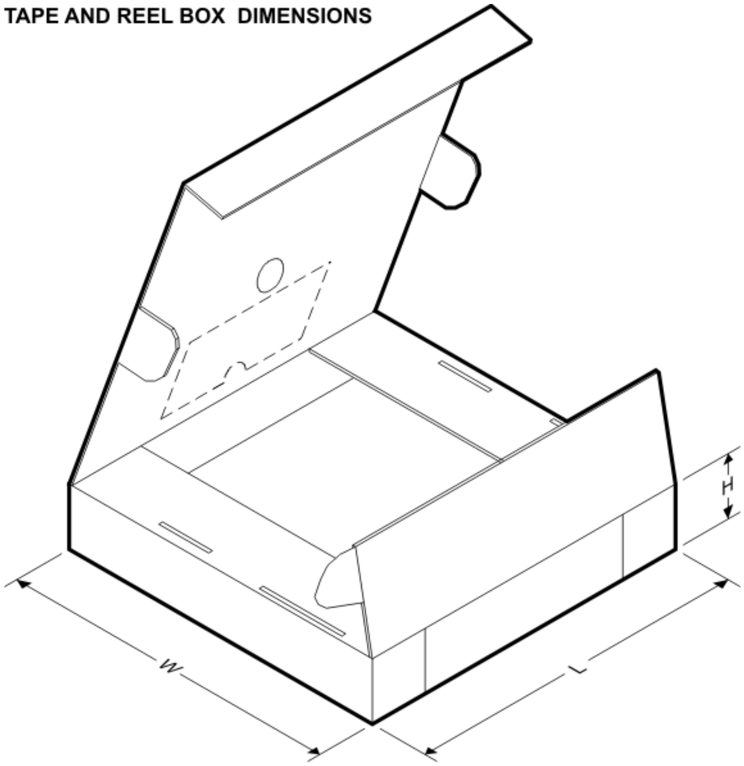
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10692BRMYR	VQFN-HR	RMY	36	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LM10692BRMYT	VQFN-HR	RMY	36	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LM10692RMYR	VQFN-HR	RMY	36	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LM10692RMYT	VQFN-HR	RMY	36	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

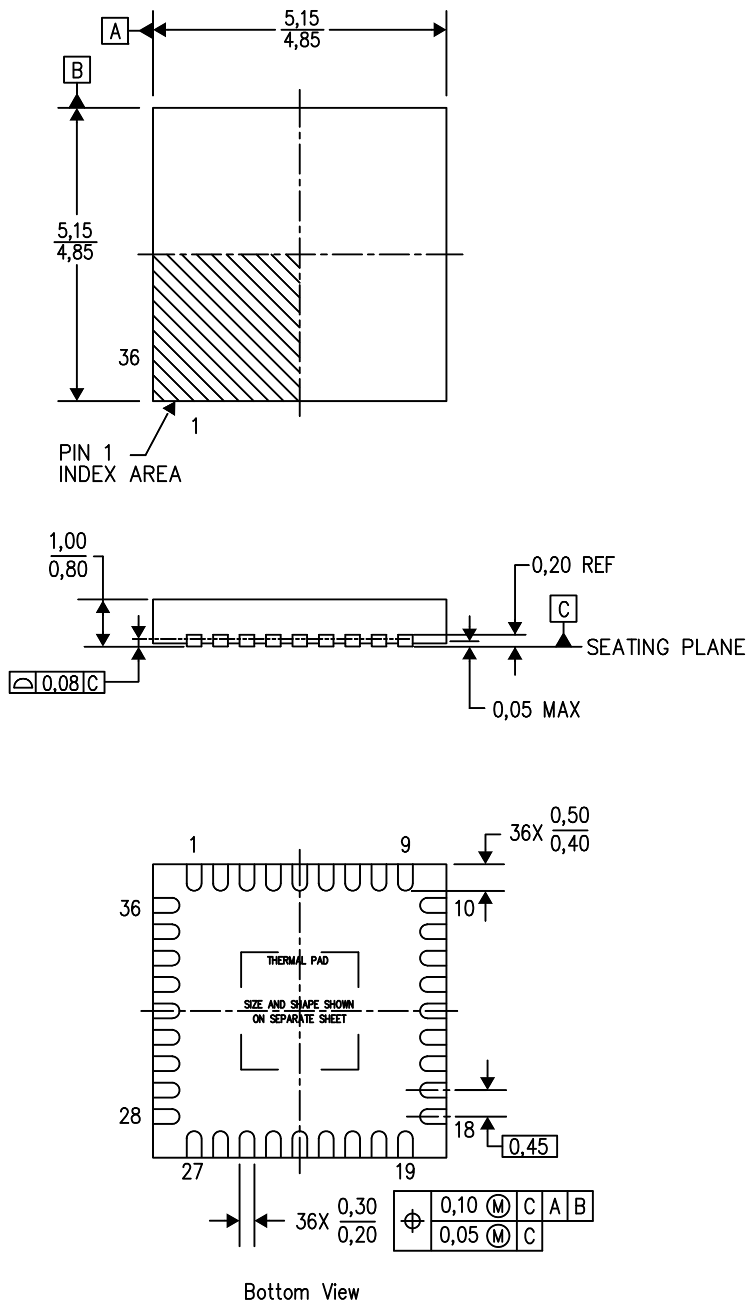
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10692BRMYR	VQFN-HR	RMY	36	3000	367.0	367.0	35.0
LM10692BRMYT	VQFN-HR	RMY	36	250	210.0	185.0	35.0
LM10692RMYR	VQFN-HR	RMY	36	3000	367.0	367.0	35.0
LM10692RMYT	VQFN-HR	RMY	36	250	210.0	185.0	35.0

RMY (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

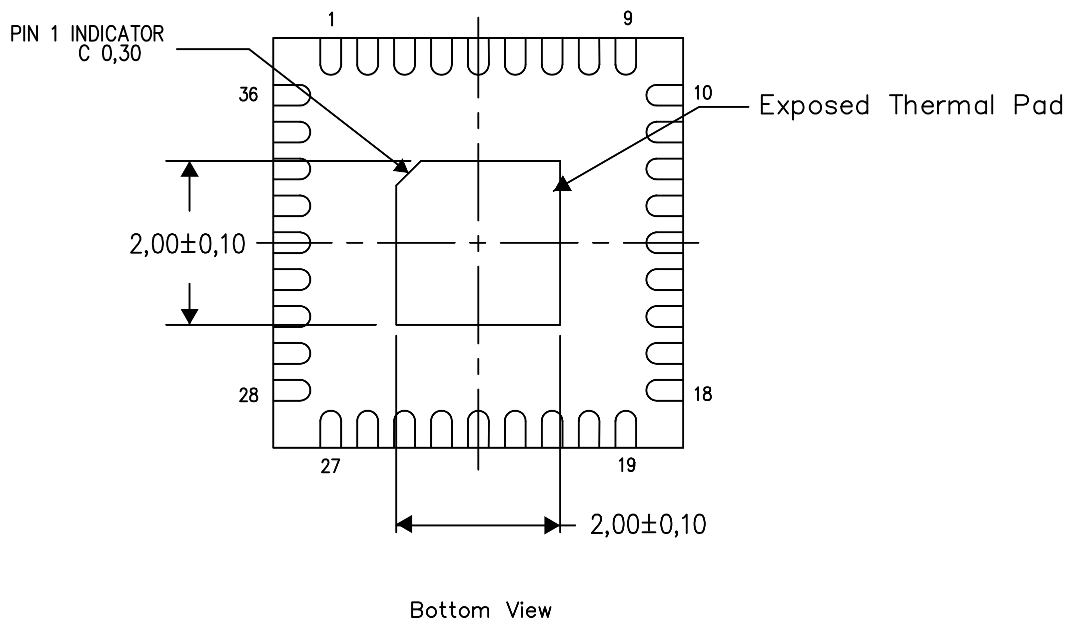
RMY (S-PWQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4221519/A 05/14

NOTE: All linear dimensions are in millimeters

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