

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

SDAS220B – DECEMBER 1982 – REVISED DECEMBER 1994

- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation:**
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- **Operate With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for n-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - Stacked or Push-Down Registers
  - Buffer Storage
  - Accumulator Registers
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

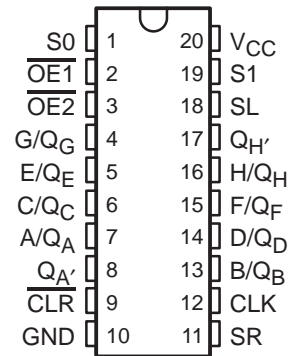
## description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select ( $S_0$ ,  $S_1$ ) inputs and two output-enable ( $\overline{OE1}$ ,  $\overline{OE2}$ ) inputs can be used to choose the modes of operation listed in the function table.

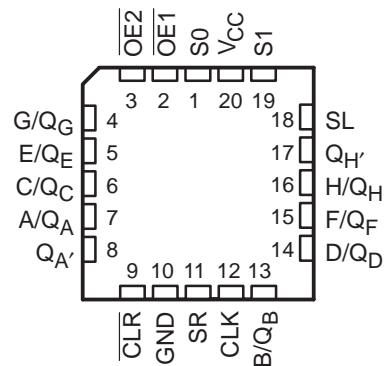
Synchronous parallel loading is accomplished by taking both  $S_0$  and  $S_1$  high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear ( $\overline{CLR}$ ) input is low. Taking either  $\overline{OE1}$  or  $\overline{OE2}$  high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ALS299 is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

SN54ALS299 . . . J PACKAGE  
SN74ALS299 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54ALS299 . . . FK PACKAGE  
(TOP VIEW)



# SN54ALS299, SN74ALS299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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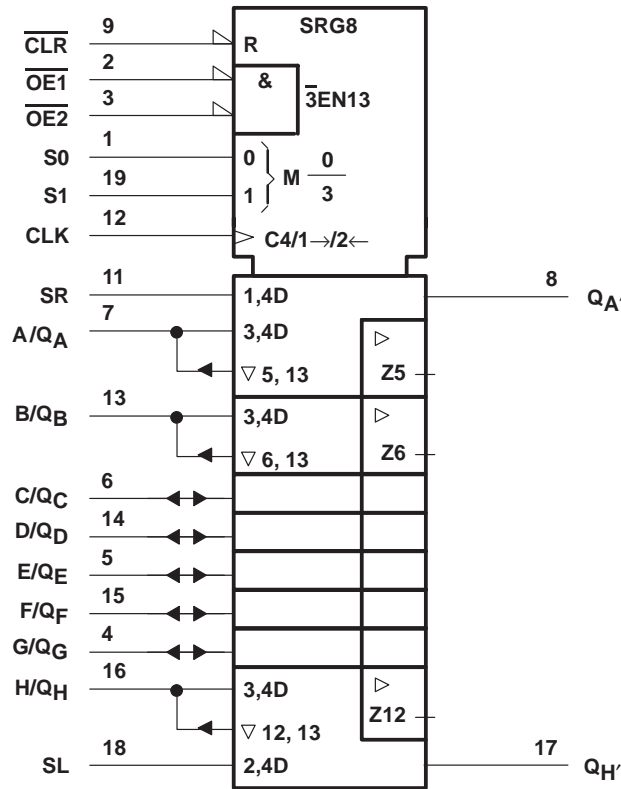
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS			
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'		
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	↑	X	H	H	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	H	QH <sub>n</sub>	H	QH <sub>n</sub>
	H	L	H	L	L	↑	X	L	L	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	L	QH <sub>n</sub>	L	QH <sub>n</sub>
Shift Left	H	H	L	L	L	↑	H	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	H	QB <sub>n</sub>	H	QB <sub>n</sub>	H
	H	H	L	L	L	↑	L	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	L	QB <sub>n</sub>	L	QB <sub>n</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

### logic symbol‡

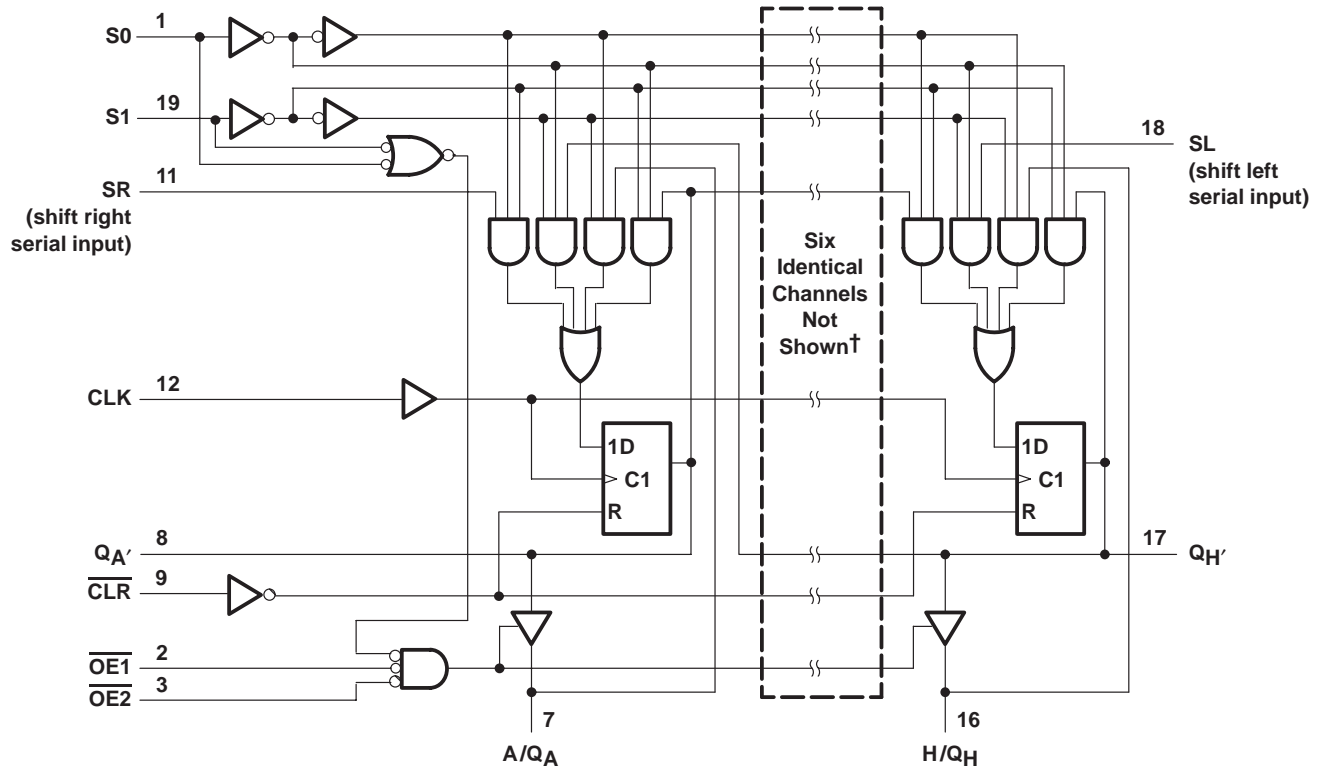


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



† I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS299	-55°C to 125°C
SN74ALS299	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54ALS299, SN74ALS299

## 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions

		SN54ALS299			SN74ALS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current	$Q_A'$ or $Q_H'$		-0.4		-0.4		mA
		$Q_A - Q_H$		-1		-2.6		
$I_{OL}$	Low-level output current	$Q_A'$ or $Q_H'$		4		8		mA
		$Q_A - Q_H$		12		24		
$T_A$	Operating free-air temperature	-55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299			SN74ALS299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$		-1.5			-1.5			V
$V_{OH}$	All outputs	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
	$Q_A - Q_H$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$		2.4	3.3			2.4 3.2	
			$I_{OH} = -2.6\text{ mA}$							
$V_{OL}$	$Q_A'$ or $Q_H'$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4	0.25 0.4		V	
			$I_{OL} = 8\text{ mA}$				0.35 0.5			
	$Q_A - Q_H$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$		0.25	0.4	0.25 0.4			
			$I_{OL} = 24\text{ mA}$				0.35 0.5			
$I_I$	A – H	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$		0.1			0.1	mA	
	Any others		$V_I = 7\text{ V}$		0.1			0.1		
$I_{IH}^\ddagger$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		20			20	μA	
$I_{IL}^\ddagger$	S0, S1, SR, SL	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		-0.2			-0.2	mA	
	Any others				-0.1			-0.1		
$I_{OS}^\S$	$Q_A'$ or $Q_H'$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$		-15	-70	-15	-70	mA	
	$Q_A - Q_H$				-20	-112	-30	-112		
$I_{CC}$	$V_{CC} = 5.5\text{ V}$		Outputs high		15	28	15	28	mA	
			Outputs low		22	38	22	38		
			Outputs disabled		23	40	23	40		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports ( $Q_A - Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN54ALS299		SN74ALS299		UNIT	
		MIN	MAX	MIN	MAX		
$f_{\text{clock}}$	Clock frequency (at 50% duty cycle)	0	17	0	30	MHz	
$t_w$	Pulse duration	CLK high or low		16.5		ns	
		CLR low		10			
$t_{\text{su}}$	Setup time before CLK $\uparrow$	S0 or S1		20		ns	
		Serial or parallel data	High		16		
			Low		6		
	Inactive-state setup time before CLK $\uparrow$ $\dagger$	CLR		15			
$t_h$	Hold time after CLK $\uparrow$	S0 or S1		0		ns	
		Serial or parallel data		0			

$\dagger$  Inactive-state setup time is also referred to as recovery time.

## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}\ddagger$				UNIT
			SN54ALS299		SN74ALS299		
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			17		30	MHz	
$t_{\text{PLH}}$	CLK	$Q_A - Q_H$	2	19	4	13	ns
$t_{\text{PHL}}$			4	25	7	19	
$t_{\text{PLH}}$	CLK	$Q_{A'} \text{ or } Q_{H'}$	2	21	5	15	ns
$t_{\text{PHL}}$			4	25	8	18	
$t_{\text{PHL}}$	CLR	$Q_A - Q_H$	6	29	6	22	ns
		$Q_{A'} \text{ or } Q_{H'}$	6	29	6	22	
$t_{\text{PZH}}$	$\overline{OE1}, \overline{OE2}$	$Q_A - Q_H$	5	22	6	16	ns
$t_{\text{PZL}}$			6	27	8	22	
$t_{\text{PZH}}$	S0, S1	$Q_A - Q_H$	5	27	7	17	ns
$t_{\text{PZL}}$			6	26	8	22	
$t_{\text{PHZ}}$	$\overline{OE1}, \overline{OE2}$	$Q_A - Q_H$	1	15	1	8	ns
$t_{\text{PLZ}}$			4	38	5	15	
$t_{\text{PHZ}}$	S0, S1	$Q_A - Q_H$	1	16	1	12	ns
$t_{\text{PLZ}}$			4	34	8	25	

$\ddagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS299, SN74ALS299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
83021012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK	<a href="#">Samples</a>
8302101RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J	<a href="#">Samples</a>
8302101SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W	<a href="#">Samples</a>
SN74ALS299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299	<a href="#">Samples</a>
SN74ALS299DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS299DWRE4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS299DWRG4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS299N	<a href="#">Samples</a>
SN74ALS299NSR	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS299NSRE4	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS299NSRG4	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		
SNJ54ALS299FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK	<a href="#">Samples</a>
SNJ54ALS299J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J	<a href="#">Samples</a>
SNJ54ALS299W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS299, SN74ALS299 :**

● Catalog: [SN74ALS299](#)

● Military: [SN54ALS299](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

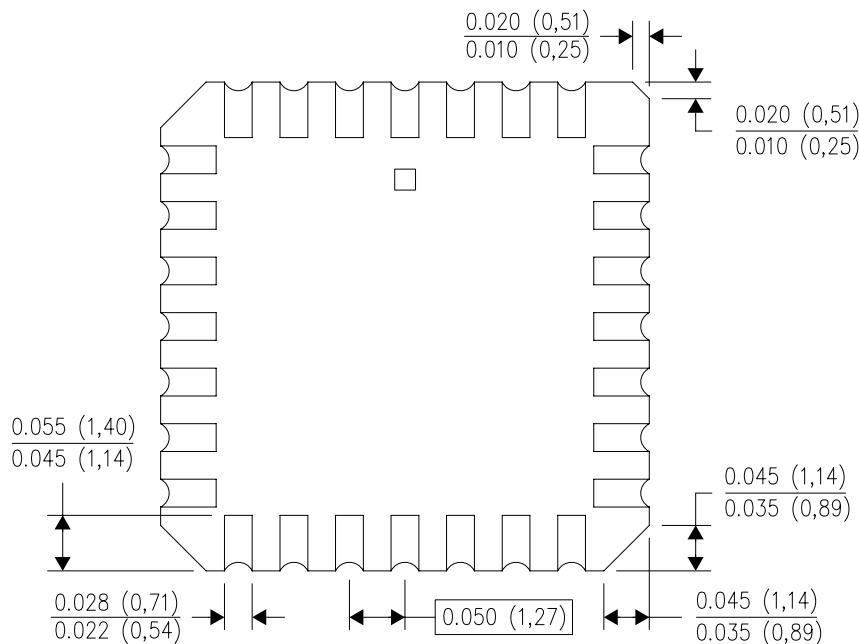
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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