CAT1163 (16K)

Supervisory Circuits with I²C Serial CMOS EEPROM, Precision Reset Controller and Watchdog Timer

FEATURES

- **Watchdog timer input (WDI)**
- **400kHz I²C bus compatible**
- **2.7V to 6.0V operation**
- **Low power CMOS technology**
- **16-Byte page write buffer**
- **Built-in inadvertent write protection**
  - **— V_{CC} lock out**
  - **— Write protect pin, WP**
- **Active high or low reset**
  - **— Precision power supply voltage monitor**
  - **— 5V, 3.3V and 3V systems**
  - **— Five threshold voltage options**
- **1,000,000 Program/Erase cycles**
- **Manual reset**
- **100 Year data retention**
- **8-pin DIP or 8-pin SOIC**
- **Commercial and industrial temperature ranges**

DESCRIPTION

The CAT1163 is a complete memory and supervisory solution for microcontroller-based systems. A serial EEPROM memory (16K) with hardware memory write protection, a system power supervisor with brown out protection and a watchdog timer are integrated together in low power CMOS technology. Memory interface is via an I²C bus.

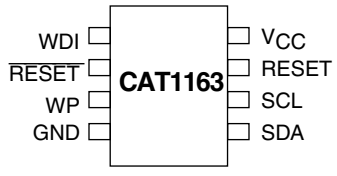
The 1.6-second watchdog circuit returns a system to a known good state if a software or hardware glitch halts or "hangs" the system. The CAT1163 watchdog monitors the WDI input pin.

The power supply monitor and reset circuit protects memory and system controllers during power up/down and against brownout conditions. Five reset threshold voltages support 5V, 3.3V and 3V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 200 ms after the supply voltage exceeds the reset threshold level. With both active high and low reset signals, interface to microcontrollers and other ICs is simple. In addition, a reset pin can be used as debounced input for push-button manual reset capability.

The CAT1163 memory features a 16-byte page. In addition, hardware data protection is provided by a write protect pin WP and by a V_{CC} sense circuit that prevents writes to memory whenever V_{CC} falls below the reset threshold or until V_{CC} reaches the reset threshold during power up.

Available packages include an 8-pin DIP and a surface mount, 8-pin SO package.

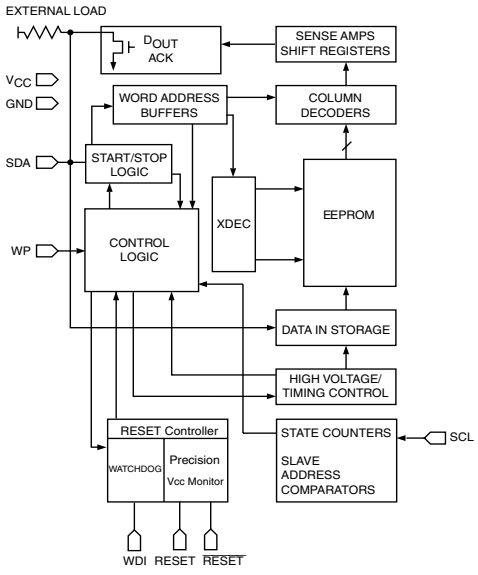
PIN CONFIGURATION



Reset Threshold Voltage Options

Part Dash Number	Minimum Threshold	Maximum Threshold
-45	4.50	4.75
-42	4.25	4.50
-30	3.00	3.15
-28	2.85	3.00
-25	2.55	2.70

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

PIN FUNCTIONS

Pin No.	Pin Name	Function
1	WDI	Watchdog Timer Input
2	$\overline{\text{RESET}}$	Active Low Reset I/O
3	WP	Write Protect
4	GND	Ground
5	SDA	Serial Data/Address
6	SCL	Clock Input
7	RESET	Active High Reset I/O
8	V_{CC}	Power Supply

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END}(3)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR}(3)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP}(3)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I_{LTH}(3)(4)	Latch-Up	JEDEC Standard 17	100		mA

DC OPERATING CHARACTERISTICS

V_{CC} = +2.7V to +6.0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 100 kHz			3	mA
I_{SB}	Standby Current	V_{CC} = 3.3V V_{CC} = 5			40 50	µA µA
I_{LI}	Input Leakage Current	V_{IN} = G_{ND} or V_{CC}			2	µA
I_{LO}	Output Leakage Current	V_{IN} = G_{ND} or V_{CC}			10	µA
V_{IL}	Input Low Voltage		-1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage (SDA)	I_{OL} = 3 mA, V_{CC} = 3.0V			0.4	V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

CAPACITANCE

T_A = 25˚C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

AC CHARACTERISTICS

V_{CC}=2.7V to 6.0V unless otherwise specified.
Output Load is 1 TTL Gate and 100pF.

		V_{CC} = 2.7V - 6V		V_{CC} = 4.5V - 5.5V		
SYMBOL	PARAMETER	Min	Max	Min	Max	Units
F_{SCL}	Clock Frequency		100		400	kHz
T_I(1)	Noise Suppresion Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SLC Low to SDA Data Out and ACK Out		3.5		1	µs
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.2		µs
t_{HIGH}	Clock High Period	4		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	50		50		ns
t_R(1)	SDA and SCL Rise Time		1		0.3	µs
t_F(1)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		µs
t_{DH}	Data Out Hold Time	100		100		ns

POWER-UP TIMING (1)(2)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

WRITE CYCLE LIMITS

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specific operation can be initiated.

RESET CIRCUIT CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units
t_{GLITCH}	Glitch Reject Pulse Width			100	ns
V_{RT}	Reset Threshold Hystersis	15			mV
V_{OLRS}	Reset Output Low Voltage (I_{OLRS}=1mA)			0.4	V
V_{OHRS}	Reset Output High Voltage	V_{CC}-0.75			V
V_{TH}	Reset Threshold (VCC=5V) (CAT1163-45)	4.50		4.75	V
	Reset Threshold (VCC=5V) (CAT1163-42)	4.25		4.50	
	Reset Threshold (VCC=3.3V) (CAT1163-30)	3.00		3.15	
	Reset Threshold (VCC=3.3V) (CAT1163-28)	2.85		3.00	
	Reset Threshold (VCC=3V) (CAT1163-25)	2.55		2.70	
t_{PURST}	Power-Up Reset Timeout	130		270	ms
t_{WD}	Watchdog Period		1.6		sec
t_{RPD}	V_{TH} to RESET Output Delay			5	µs
V_{RVALID}	RESET Output Valid	1			V

PIN DESCRIPTIONS

WDI: WATCHDOG INPUT
If there is no transition on the WDI for more than 1.6 seconds, the watchdog timer times out.

WP: WRITE PROTECT
If the pin is tied to V_{CC} the entire memory array becomes Write Protected (READ only). When the pin is tied to GND or left floating normal read/write operations are allowed to the device.

RESET/$\overline{\text{RESET}}$: RESET I/O
These are open drain pins and can be used as reset trigger inputs. By forcing a reset condition on the pins the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull-down resistor and the $\overline{\text{RESET}}$ pin must be connected through a pull-up resistor.

SDA: SERIAL DATA ADDRESS
The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

SCL: SERIAL CLOCK
Serial clock input.

DEVICE OPERATION

Reset Controller Description

The CAT1163 precision RESET controller ensures correct system operation during brownout and power up/down conditions. It is configured with open drain RESET outputs. During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TH} threshold and will continue driving the outputs for approximately 200ms (t_{PURST}) after reaching V_{TH}. After the t_{PURST} timeout interval, the device will cease to drive the reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/down resistors. During power-down, the RESET outputs will be active when V_{CC} falls below V_{TH}. The RESET outputs will be valid so long as V_{CC} is >1.0V (V_{RVALID}).

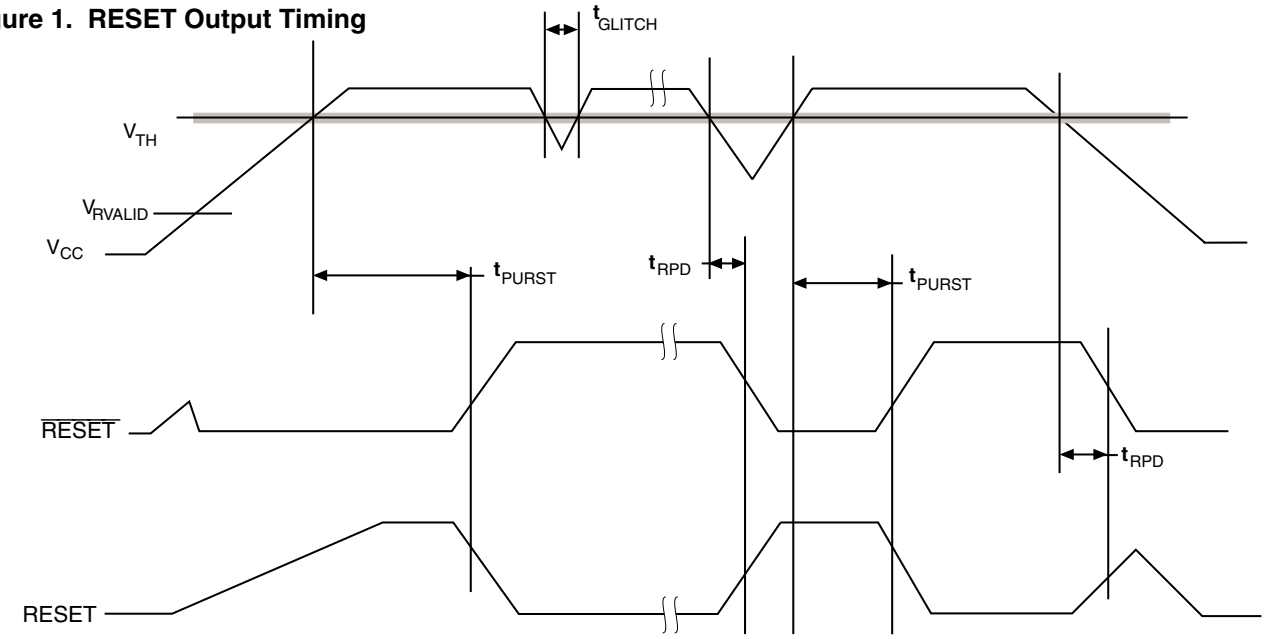
The RESET pins are I/Os; therefore, the CAT1163 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input in the CAT1163 will initiate a reset timeout after detecting a low to high transition and the $\overline{\text{RESET}}$ input in the CAT1163 will initiate a reset timeout after detecting a high to low transition.

Watchdog Timer

The Watchdog Timer provides an independent protection for microcontrollers. During a system failure, the CAT1163 will respond with a reset signal after a time-out interval of 1.6 seconds for a lack of activity. The CAT1163 is designed with a WDI input pin for the Watchdog Timer function. If the microcontroller does not toggle the WDI input pin within 1.6 seconds, the Watchdog Timer times out. This will generate a reset condition on reset outputs. The Watchdog Timer is cleared by any transition on WDI.

As long as the reset signal is asserted, the Watchdog Timer will not count and will stay cleared.

Figure 1. RESET Output Timing



Hardware Data Protection

The CAT1163 is designed with the following hardware data protection features to provide a high degree of data integrity.

(1) The CAT1163 features a WP pin. When the WP pin is tied high the entire memory array becomes write protected (read only).

(2) The V_{CC} sense provides write protection when V_{CC} falls below the reset threshold value (VTH). The V_{CC} lock out inhibits writes to the serial EEPROM whenever V_{CC} falls below (power down) VTH or until V_{CC} reaches the reset threshold (power up) V_{TH}.

Any attempt to access the internal EEPROM is not recognized and an ACK will not be sent on the SDA line when RESET or $\overline{\text{RESET}}$ is active.

Reset Threshold Voltage

The CAT1163 is offered with five reset threshold voltage ranges. They are 4.50-4.75V, 4.25-4.50V, 3.00-3.15V, 2.85-3.00V and 2.55-2.70V.

Figure 2. Bus Timing

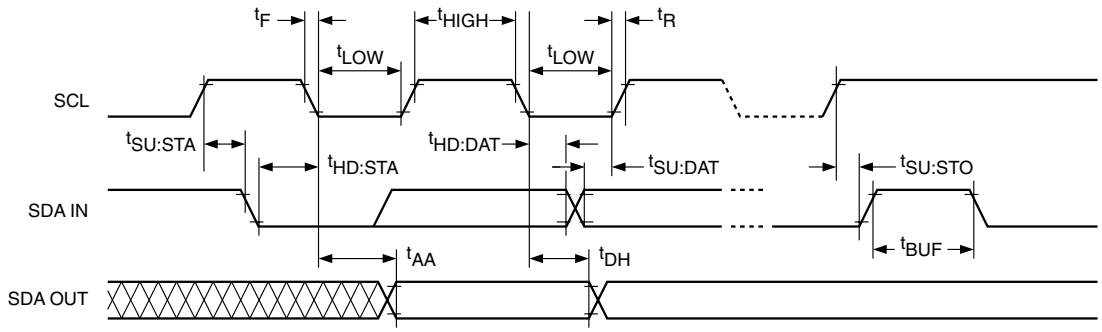


Figure 3. Write Cycle Timing

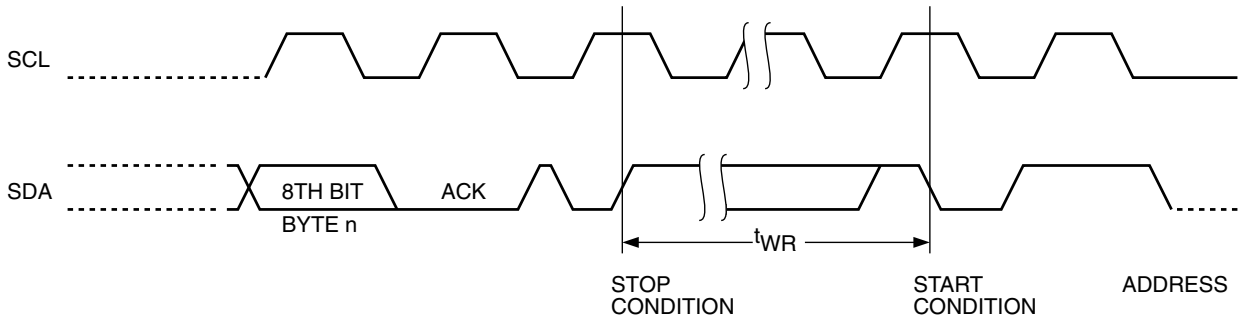
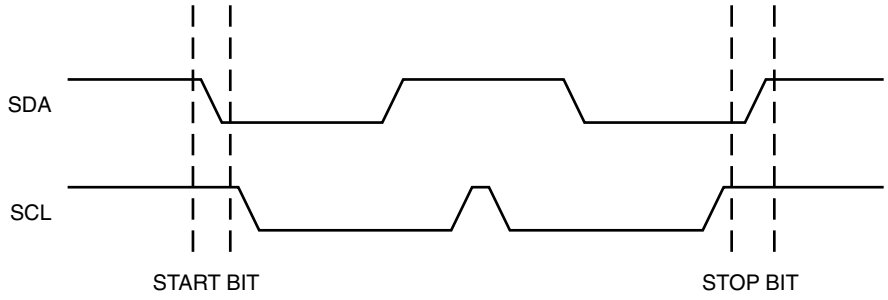


Figure 4. Start/Stop Timing



FUNCTIONAL DESCRIPTION

The CAT1163 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1163 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010.

The next three bits (Figure 6) define memory addressing. For the CAT1163 the three bits define higher order bits.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1163 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1163 then performs a Read or Write operation depending on the R/$\overline{W}$ bit.

Figure 5. Acknowledge Timing

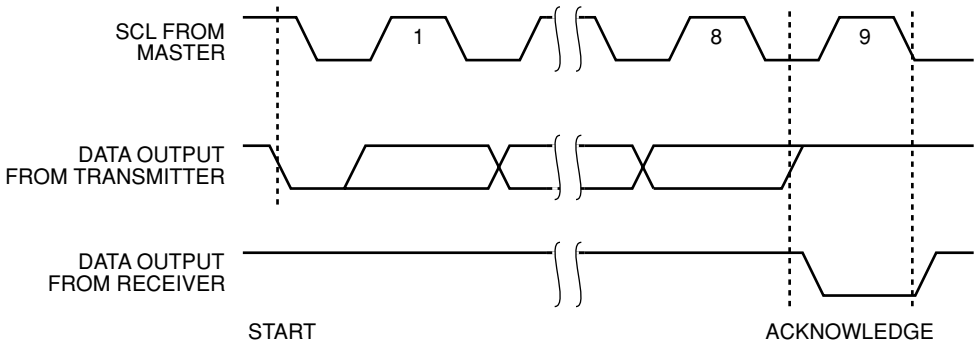


Figure 6. Slave Address Bits

CAT1163	1	0	1	0	a10	a9	a8	R/$\overline{W}$

* 'X' corresponds to Don't Care Bits (can be zero or a one).

** a8, a9 and a10 correspond to the address of the memory array address word.

ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1163 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT1163 begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1163 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends a 8-bit address that is to be written into the address pointers of the CAT1163. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT1163 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non-volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT1163 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted, the CAT1163 will respond with an acknowledge and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes before sending the STOP condition, the address counter 'wraps around,' and previously transmitted data will be overwritten.

When all 16 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT1163 in a single write cycle.

Figure 7. Byte Write Timing

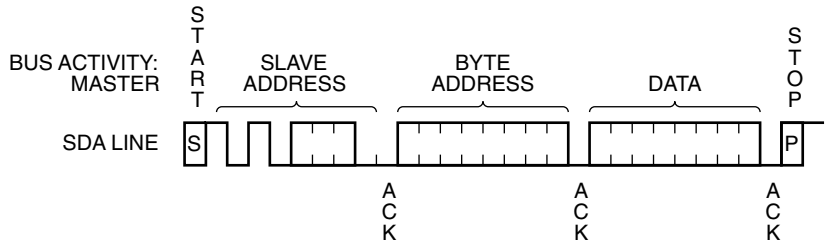
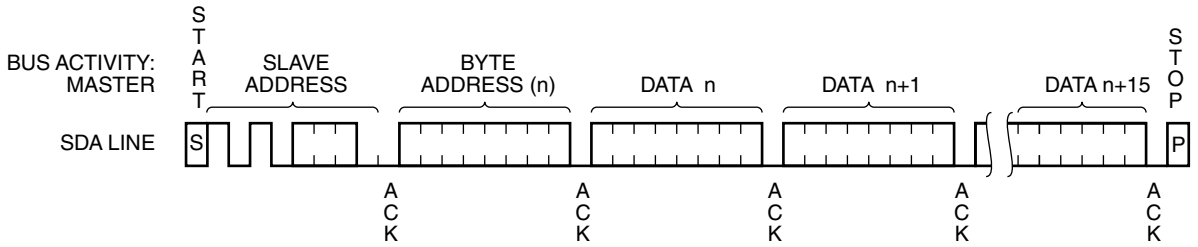


Figure 8. Page Write Timing



Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write opration the CAT1163 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT1163 is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

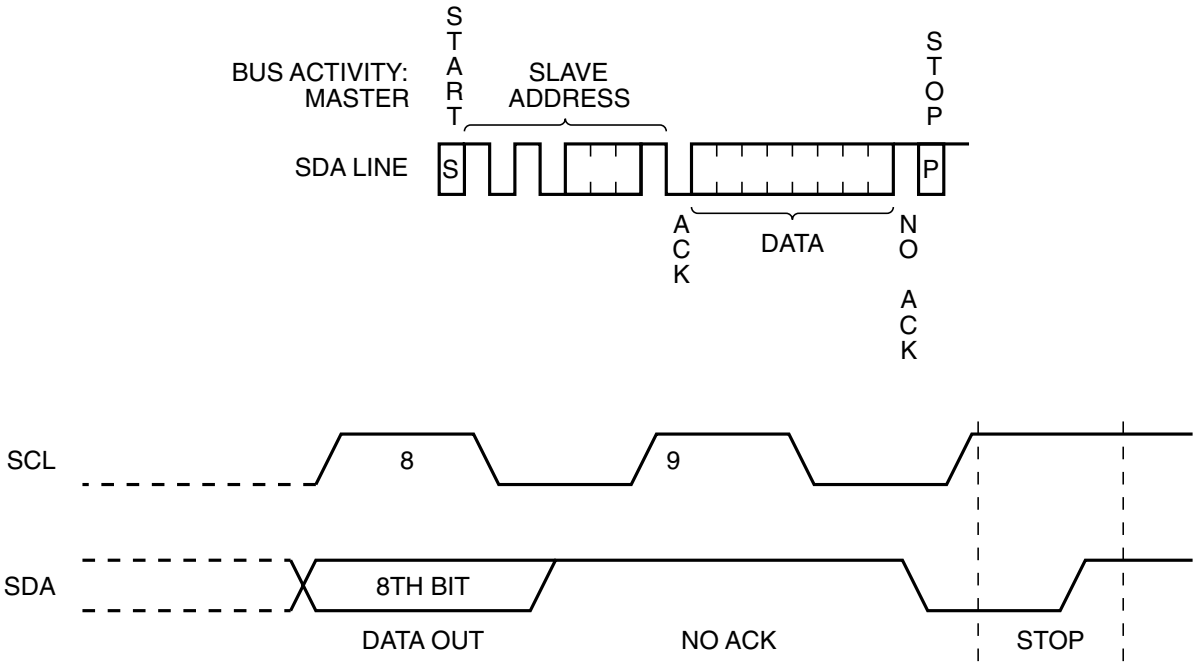
WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent memory array programming. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT1163 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

Read Operations

The READ operation for the CAT1163 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Figure 9. Immediate Address Read Timing



Immediate/Current Address Read

The CAT1163's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E=2047 for the CAT1163) then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT1163 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1163 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1163 then responds with its acknowledge and sends teh 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1163 sends the inital 8-bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1163 will continue to output an 8-bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from CAT1163 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT1163 address bits so that the entire memory array can be read during one operation. If more than E (where E=2047 for the CAT1163) bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Manual Reset Operation

The CAT116x RESET or $\overline{RESET}$ pin can also be used as a manual reset input.

Only the "active" edge of the manual reset input is internally sensed. The positive edge is sensed if RESET is used as a manual reset input and the negative edge is sensed if $\overline{RESET}$ is used as a manual reset input.

An internal counter starts a 200 ms count. During this time, the complementary reset output will be kept in the active state. If the manual reset input is forced active for more than 200 ms, the complementary reset output will switch back to the non active state after the 200 ms expired, regardless for how long the manual reset input is forced active.

The embedded EEPROM is disabled as long as a reset condition is maintained on any RESET pin. If the external forced RESET/$\overline{RESET}$ is longer than internal controlled time-out period, tPURST, the memory will not respond with an acknowledge for any access as long as the manual reset input is active.

Figure 10. Selective Read Timing

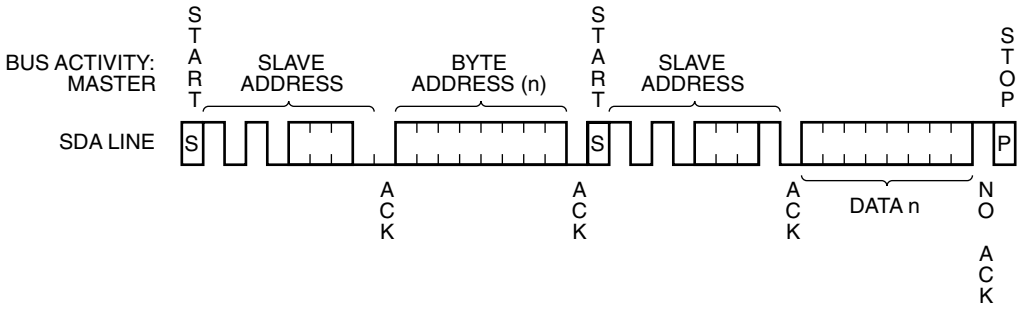
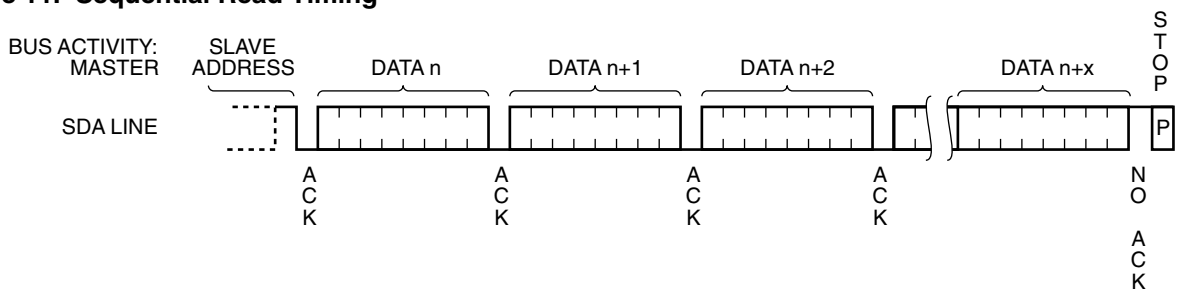
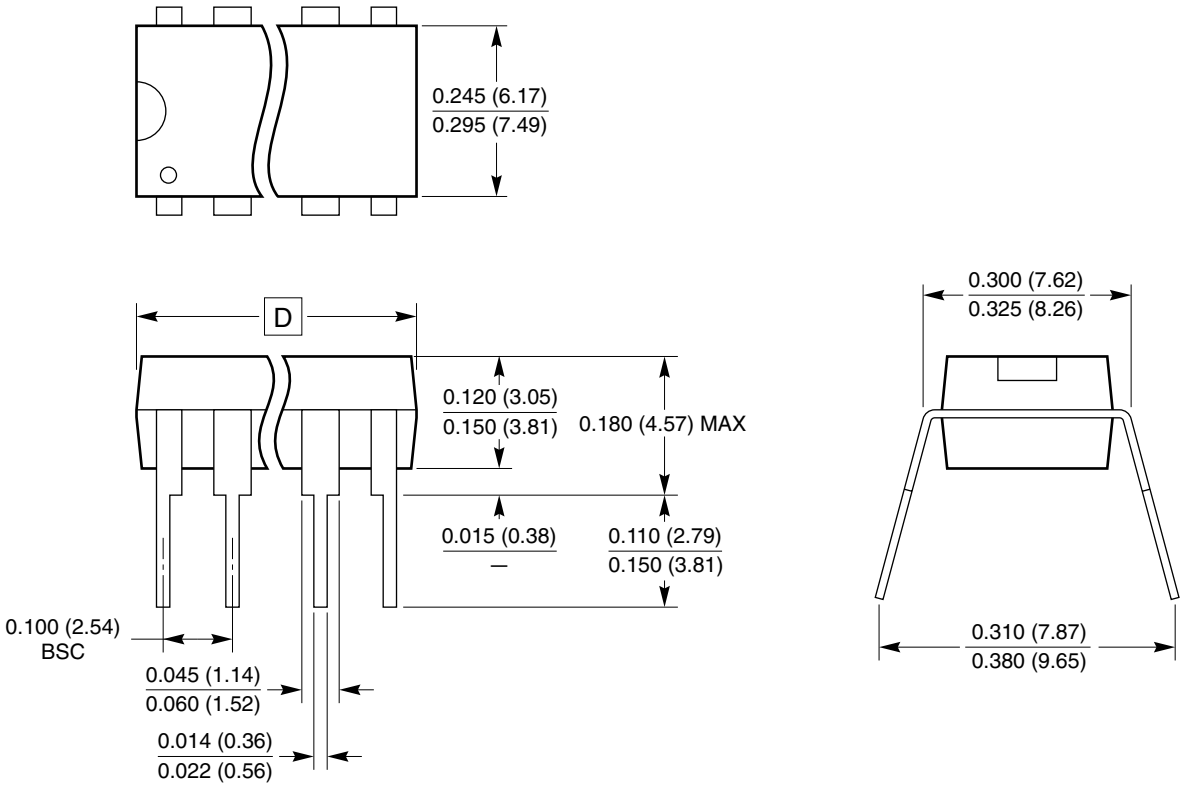


Figure 11. Sequential Read Timing



PACKAGE OUTLINES

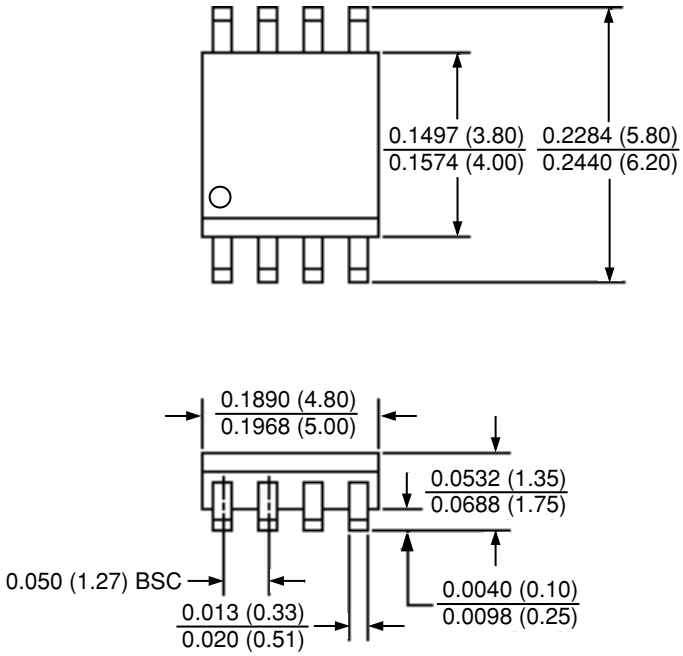
8-LEAD 300 MIL WIDE PLASTIC DIP (P, L)



Dimension D		
Pkg	**Min**	**Max**
8L	0.355 (9.02)	0.400 (10.16)

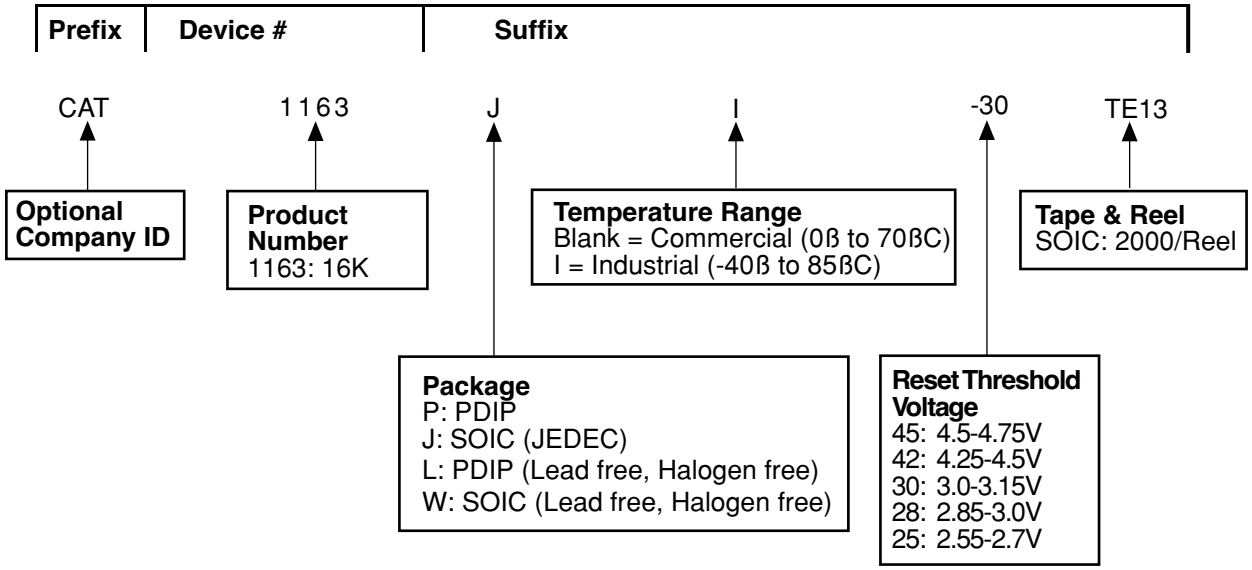
Notes:
1. Complies with JEDEC Publication 95 MS001 dimensions; however, some of the dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

8-LEAD 150 MIL WIDE SOIC (J, W)



Notes:
1. Complies with JEDEC publication 95 MS-012 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.
3. Lead coplanarity is 0.004" (0.102mm) maximum.

Ordering Information



Note:
(1) The device used in the above example is a CAT1163JI-30TE13 (16K I²C Memory, SOIC, Industrial Temperature, 3.0-3.15V Reset Threshold Voltage, Tape and Reel)

REVISION HISTORY

Date	Revision	Comments
02/17/05	D	Add Green Logo Add Package Outline Update Ordering Information

CATALYST

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Publication #: 3003
Revison: D
Issue date: 02/17/05
Type: Final