Features

- 32K x 36 or 64K x 18 organizations
- 0.25µ CMOS technology
- Synchronous Register-Latch Mode of Operation with Self-Timed Late Write
- Single Differential PECL Clock
- +3.3V Power Supply, Ground, 2.5V V_{DDQ}
- 2.5V LVTTL Input and Output levels
- Registered Addresses, Write Enables, Synchronous Select, and Data Ins
- Latched Outputs
- Common I/O
- 30Ω Drivers
- Asynchronous Output Enable and Power Down Inputs
- Boundary Scan using limited set of JTAG 1149.1 functions
- Byte Write Capability & Global Write Enable
- 7 x 17 Bump Ball Grid Array Package with SRAM JEDEC Standard Pinout and Boundary SCAN Order

Description

IBM0436A1ANLAA and IBM0418A1ANLAA are 1Mb Synchronous Register-Latch Mode, high-performance CMOS Static Random Access Memories (SRAM). These SRAMs are versatile, have a wide input/output (I/O) interface, and can achieve cycle times as short as 4.5ns. Differential K clocks are used to initiate the read/write operation; all internal operations are self-timed. At the rising edge of the K clock, all address, write-enable, sync select, and data input signals are registered internally. Data outputs are updated from output registers off the falling edge of the K clock. An internal write buffer allows write data to follow one cycle after addresses and controls. The device is operated with a single +3.3V power supply and is compatible with 2.5V LVTTL I/O interfaces.

x36 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQ19	DQ18	V_{SS}	NC	V_{SS}	DQ9	DQ10
E	DQ22	DQ20	V_{SS}	$\overline{SS}$	V_{SS}	DQ11	DQb13
F	V_{DDQ}	DQ21	V_{SS}	$\overline{G}$	V_{SS}	DQ12	V_{DDQ}
G	DQ24	DQ23	$\overline{SBWc}$	NC	$\overline{SBWb}$	DQ14	DQb15
H	DQ25	DQ26	V_{SS}	NC	V_{SS}	DQ17	DQb16
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ34	DQ35	V_{SS}	K	V_{SS}	DQ8	DQ7
L	DQ33	DQ32	$\overline{SBWd}$	$\overline{K}$	$\overline{SBWa}$	DQ5	DQ6
M	V_{DDQ}	DQ30	V_{SS}	$\overline{SW}$	V_{SS}	DQ3	V_{DDQ}
N	DQ31	DQ29	V_{SS}	SA	V_{SS}	DQ2	DQ4
P	DQ28	DQ27	V_{SS}	SA	V_{SS}	DQ0	DQ1
R	NC	SA	M1*	V_{DD}	M2*	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD} and V_{SS} respectively.

x18 BGA Pinout (Top View)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	NC	NC	NC	NC	NC	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQ14	NC	V_{SS}	NC	V_{SS}	DQ0	NC
E	NC	DQ15	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQ1
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ2	V_{DDQ}
G	NC	DQ16	$\overline{SBWb}$	NC	NC	NC	DQ3
H	DQ17	NC	V_{SS}	NC	V_{SS}	DQ4	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ13	V_{SS}	K	V_{SS}	NC	DQ8
L	DQ12	NC	NC	$\overline{K}$	$\overline{SBWa}$	DQ7	NC
M	V_{DDQ}	DQ10	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQ11	NC	V_{SS}	SA	V_{SS}	DQ6	NC
P	NC	DQ9	V_{SS}	SA	V_{SS}	NC	DQ5
R	NC	SA	M1	V_{DD}	M2	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Note: * M1 and M2 are clock mode pins. For this application, M1 and M2 need to connect to V_{DD} and V_{SS} respectively.

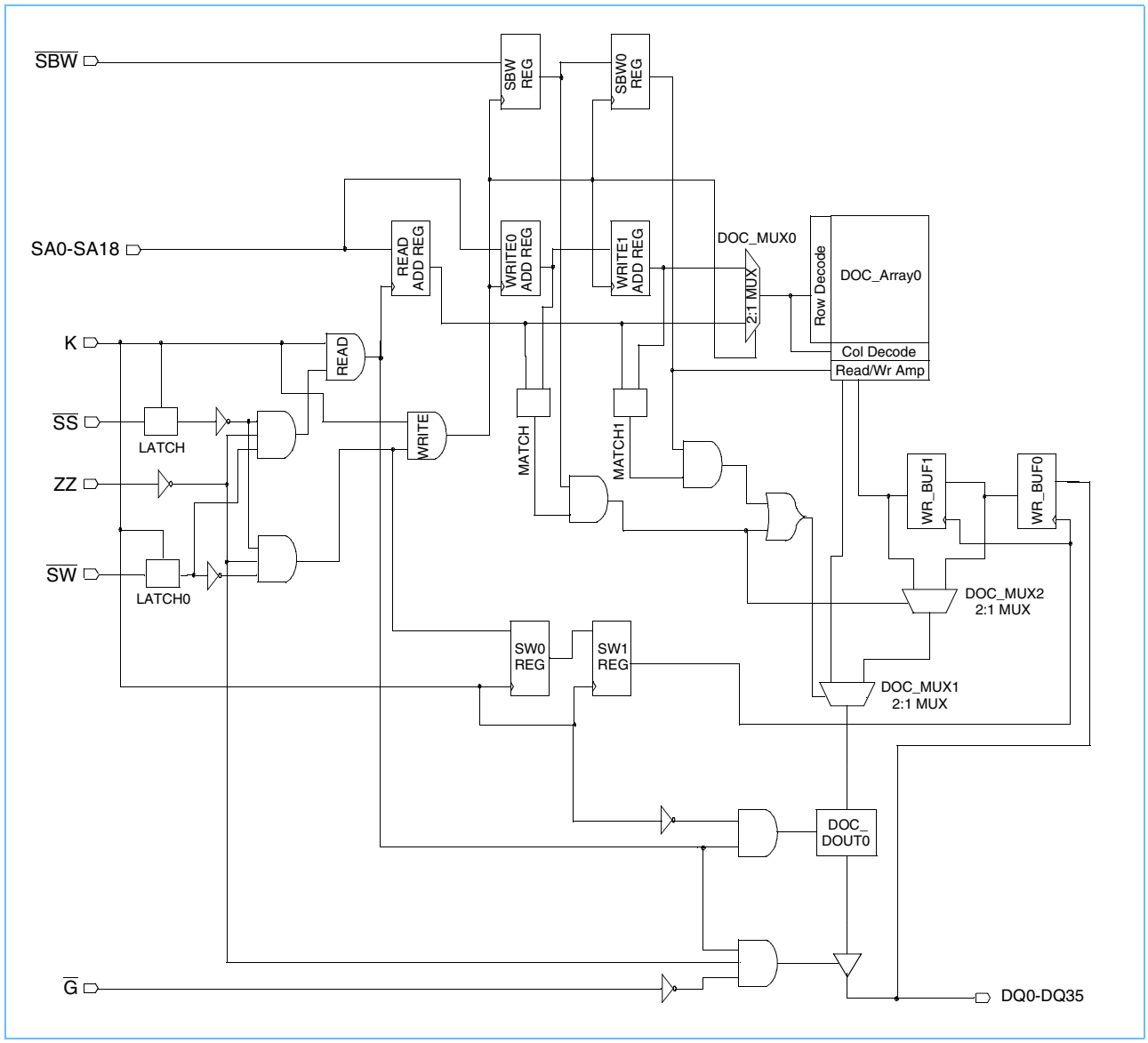
Pin Description

SA	Address Input 16 Addresses for 64K x 18 15 Addresses for 32K x 36	TDO	IEEE 1149.1 Test Output (LVTTL level)
DQ0-DQ35	Data I/O DQ0-DQ17 for 512K x 18 DQ0-DQ35 for 256K x 36	$\overline{G}$	Asynchronous Output Enable
K, $\overline{K}$	Differential Input Register Clocks	$\overline{SS}$	Synchronous Select
$\overline{SW}$	Write Enable, Global	M1, M2	Clock Mode Inputs. Selects Single or Dual Clock Operation.
$\overline{SBWa}$	Write Enable, Byte a (DQ0-DQ8)	V_{DD}	Power Supply (+3.3V)
$\overline{SBWb}$	Write Enable, Byte b (DQ9-DQ17)	V_{SS}	Ground
$\overline{SBWc}$	Write Enable, Byte c (DQ18-DQ26)	V_{DDQ}	Output Power Supply
$\overline{SBWd}$	Write Enable, Byte d (DQ27-DQ35)	ZZ	Asynchronous Sleep Mode
TMS, TDI, TCK	IEEE® 1149.1 Test Inputs (LVTTL levels)	NC	No Connect

Ordering Information

Part Number	Organization	Speed	Leads
IBM0436A1ANLAA - 4H	32K x 36	4.5ns Access / 4.5ns Cycle	7 x 17 BGA
IBM0436A1ANLAA - 5	32K x 36	5.0ns Access / 5.0ns Cycle	7 x 17 BGA
IBM0436A1ANLAA - 5H	32K x 36	5.5ns Access / 5.5ns Cycle	7 x 17 BGA
IBM0418A1ANLAB - 4H	256K x 18	4.5ns Access / 4.5ns Cycle	7 x 17 BGA
IBM0418A1ANLAB - 5	256K x 18	5.0ns Access / 5.0ns Cycle	7 x 17 BGA
IBM0418A1ANLAB - 5H	256K x 18	5.5ns Access / 5.5ns Cycle	7 x 17 BGA

Block Diagram



SRAM Features

Late Write

The Late Write function allows for write data to be registered one cycle after addresses and controls. This feature eliminates one bus-turnaround cycle, necessary when going from a read to a write operation. Late write is accomplished by buffering write addresses and data so that the write operation occurs during the next write cycle. When a read cycle occurs after a write cycle, the address and write data information are stored temporarily in holding registers. During the first write cycle preceded by a read cycle, the SRAM array is updated with address and data from the holding registers. Read cycle addresses are monitored to determine if read data is to be supplied from the SRAM array or the write buffer. The bypassing of the SRAM array occurs on a byte-by-byte basis. When only one byte is written during a write cycle, read data from the last written address has new byte data from the write buffer and remaining bytes from the SRAM array.

Mode Control

Mode control pins M1 and M2 are used to select four different JEDEC-standard read protocols. This SRAM supports single clock, register latch operation (M1 = V_{DD}, M2 = V_{SS}). This datasheet describes single clock register latch functionality only. Mode control inputs must be set at power up and must not change during SRAM operation. This SRAM is tested only in the register-latch mode.

Sleep Mode

The sleep mode is enabled by switching the synchronous signal ZZ High. When the SRAM is in the sleep mode, the outputs go to a High-Z state and the SRAM draws standby current. SRAM data is preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation.

Power-Up Requirements

To ensure the optimum internally regulated supply voltage, the SRAM requires 4µs of power-up time after V_{DD} reaches its operating range.

Power-Up and Power-Down Sequencing

The power supplies must be powered up in the following order: V_{DD}, V_{DDQ}, and Inputs. The power-down sequence must be in the reverse order. V_{DDQ} may not exceed V_{DD} by more than 0.6V. No special tracking between power supplies is required.

Clock Truth Table

K	ZZ	$\overline{SS}$	$\overline{SW}$	$\overline{SBWa}$	$\overline{SBWb}$	$\overline{SBWc}$	$\overline{SBWd}$	DQ (n)	DQ (n+1)	MODE
L→H	L	L	H	X	X	X	X	X	D_{OUT} 0-35	Read Cycle All Bytes
L→H	L	L	L	L	H	H	H	X	D_{IN} 0-8	Write Cycle 1st Byte
L→H	L	L	L	H	L	H	H	X	D_{IN} 9-17	Write Cycle 2nd Byte
L→H	L	L	L	H	H	L	H	X	D_{IN} 18-26	Write Cycle 3rd Byte
L→H	L	L	L	H	H	H	L	X	D_{IN} 27-35	Write Cycle 4th Byte
L→H	L	L	L	L	L	L	L	X	D_{IN} 0-35	Write Cycle All Bytes
L→H	L	L	L	H	H	H	H	X	High-Z	Abort Write Cycle
L→H	L	H	X	X	X	X	X	X	High-Z	Deselect Cycle
X	H	X	X	X	X	X	X	High-Z	High-Z	Sleep Mode

Output Enable Truth Table

Operation	$\overline{G}$	DQ
Read	L	D_{OUT} 0-35
Read	H	High-Z
Sleep (ZZ = H)	X	High-Z
Write ($\overline{SW}$ = L)	X	High-Z
Deselect ($\overline{SS}$ = H)	X	High-Z

Absolute Maximum Ratings

Item	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.3	V	1
Output Power Supply Voltage	V_{DDQ}	-0.5 to 2.825	V	1
Input Voltage	V_{IN}	-0.5 to 4.3	V	1, 2
DQ Input Voltage	V_{DQIN}	-0.5 to 2.825	V	1
Operating Temperature	T_A	0 to 85	°C	1
Junction Temperature	T_J	110	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	25	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Excludes DQ inputs.

Recommended DC Operating Conditions (T_A = 0 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.3 - 5%	3.3	3.3 + 10%	V	1
Output Driver Supply Voltage	V_{DDQ}	2.375	2.5	2.625	V	1
Input High Voltage	V_{IH}	1.65	—	V_{DD}+0.3	V	1, 2, 4
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3, 4
PECL K-Clock Input High Voltage	$V_{IH - PECL}$	2.135	—	2.420	V	1, 2
PECL K-Clock Input Low Voltage	$V_{IL - PECL}$	1.490	—	1.825	V	1
Output Current	I_{OUT}	—	5	8	mA	

1. All voltages are referenced to V_{SS}. All V_{DD}, V_{DDQ} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = V_{DDQ} + 0.3 V, V_{IH}(Max)AC = V_{DDQ} + 1.5 V (pulse width ≤ 4.0ns).
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns).
4. It does not include DQs.

DC Electrical Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

Parameter	Symbol	Min.	Max.	Units	Notes
Average Power Supply Operating Current- **x36** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD4H} I_{DD5} I_{DD5H}	—	380 340 300	mA	1, 3
Average Power Supply Operating Current - **x18** (I_{OUT} = 0, V_{IN} = V_{IH} or V_{IL}, ZZ & $\overline{SS}$ = V_{IL})	I_{DD4H} I_{DD5} I_{DD5H}	—	350 310 270	mA	1, 3
Power Supply Standby Current ($\overline{SS}$ = V_{IH}, ZZ = V_{IH}. All other inputs = V_{IH} or V_{IH}, I_{IH} = 0)	I_{SBSS}	—	150	mA	1
Power Supply Sleep Current (ZZ = V_{IH}, All other inputs = V_{IH} or V_{IL}, I_{OUT} = 0)	I_{SBZZ}	—	100	mA	1, 5
Input Leakage Current, any input (except JTAG) (V_{IN} = V_{SS} or V_{DDQ})	I_{LI}	-2	+2	µA	
Output Leakage Current (V_{OUT} = V_{SS} or V_{DDQ}, DQ in High-Z)	I_{LO}	-5	+5	µA	
Output “High” Level Voltage (I_{OH} = -8mA)	V_{OH}	1.6	V_{DDQ}	V	2, 4
Output “Low” Level Voltage (I_{OL} = +8mA)	V_{OL}	V_{SS}	V_{SS} + .4	V	2, 4
JTAG Leakage Current (V_{IN} = V_{SS} or V_{DD})	I_{LIJTAG}	-50	+10	µA	6

1. I_{OUT} = Device Output Current.
2. Minimum Impedance Output Driver.
3. The numeric suffix indicates part operating at speed as indicated in AC Characteristics on page 9: that is, I_{DD4H} indicates 4.5ns cycle time.
4. JEDEC Standard JESD8-6 Class 1 Compatible.
5. When ZZ = High, spec is guaranteed at 75°C junction temperature.
6. For JTAG inputs only.

PBGA Thermal Characteristics

Item	Symbol	Rating	Units
Thermal Resistance Junction to Case	RΘJC	tbd	°C/W

Capacitance (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%, f = 1MHz)

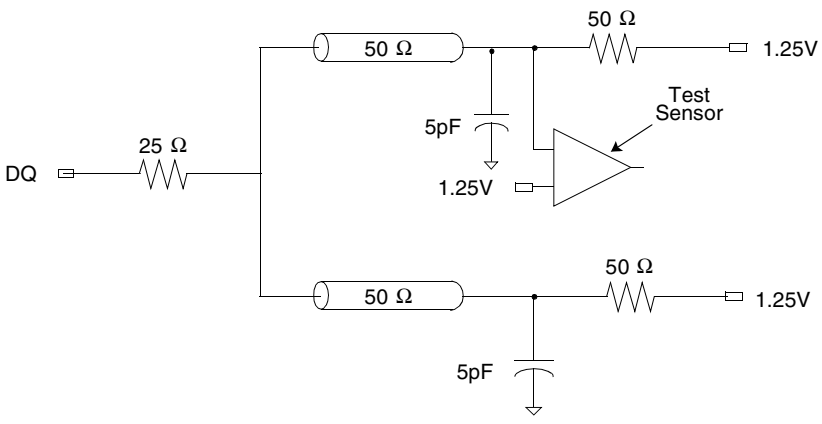
Parameter	Symbol	Test Condition	Max	Units
Input Capacitance	C_{IN}	V_{IN} = 0V	4	pF
Data I/O Capacitance (DQ0-DQ35)	C_{OUT}	V_{OUT} = 0V	4	pF

AC Test Conditions (T_A=0 to +70°C, V_{DD} =3.3V -5%, +10%, V_{DDQ} =2.5V -5%, +5%)

Parameter	Symbol	Conditions	Units	Notes
Output Driver Supply Voltage	V_{DDQ}	2.5		
Input High Level for 2.5V I/O	$V_{IH(2.5V)}$	2.25	V	2
Input Low Level for 2.5V I/O	$V_{IL(2.5V)}$	0.25	V	2
PECL K-Clock Input High Voltage	$V_{IH-PECL}$	2.4	V	
PECLK-Clock Input Low Voltage	$V_{IL-PECL}$	1.5	V	
Input Rise Time	T_R	1.0	ns	
Input Fall Time	T_F	1.0	ns	
PECL Clock Input Rise Time	T_{R-PECL}	0.5	ns	
PECL Clock Input Fall Time	T_{F-PECL}	0.5	ns	
Input and Output Timing Reference Level (except K, $\overline{K}$)		1.25	V	
PECL Clock Reference Level		K and $\overline{K}$ Cross Point	V	
Output Load Conditions				1

1. See the AC Test Loading figure below.
2. Does not include DQs.

AC Test Loading

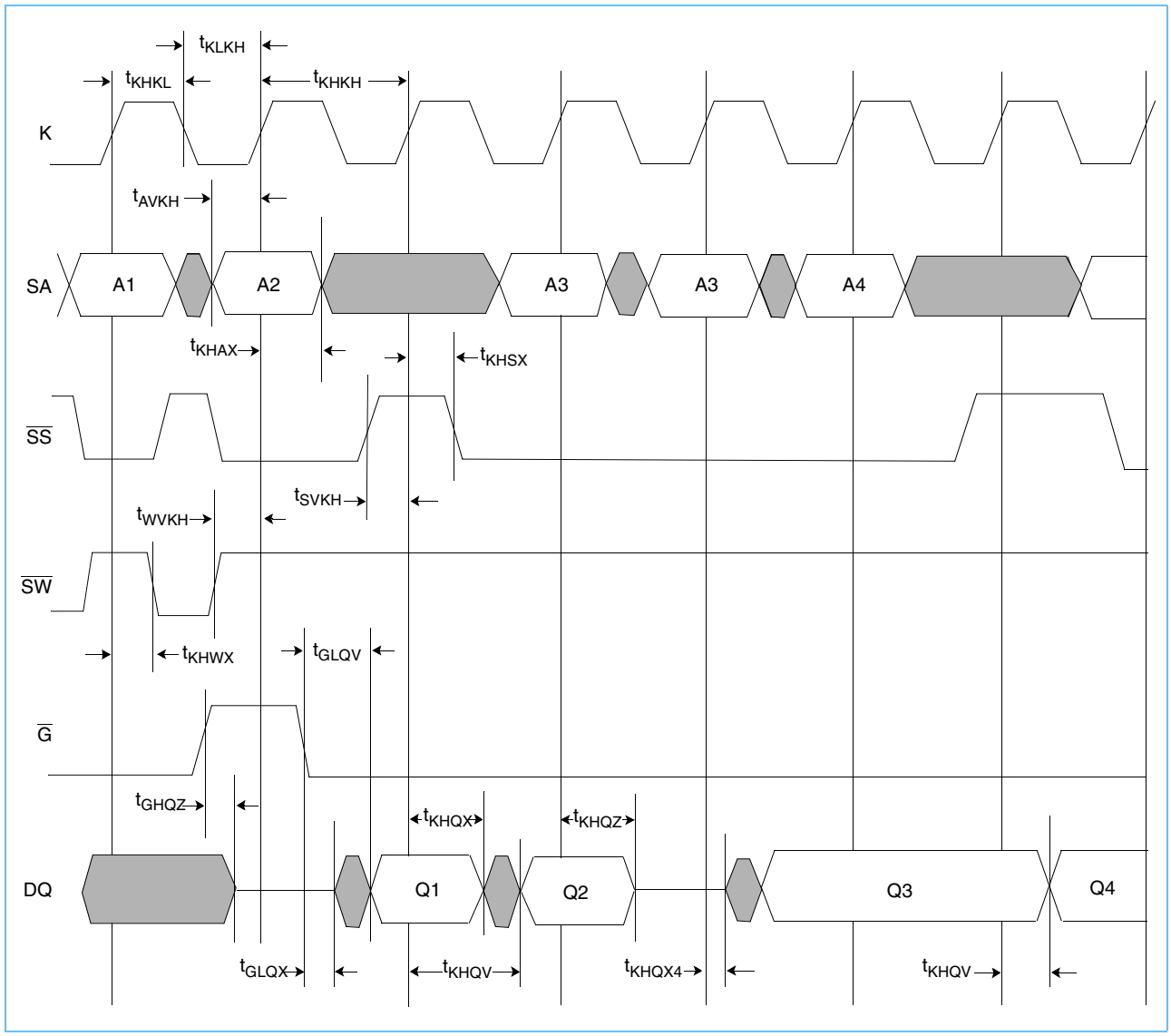


AC Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%, V_{DDQ} = 2.5V).

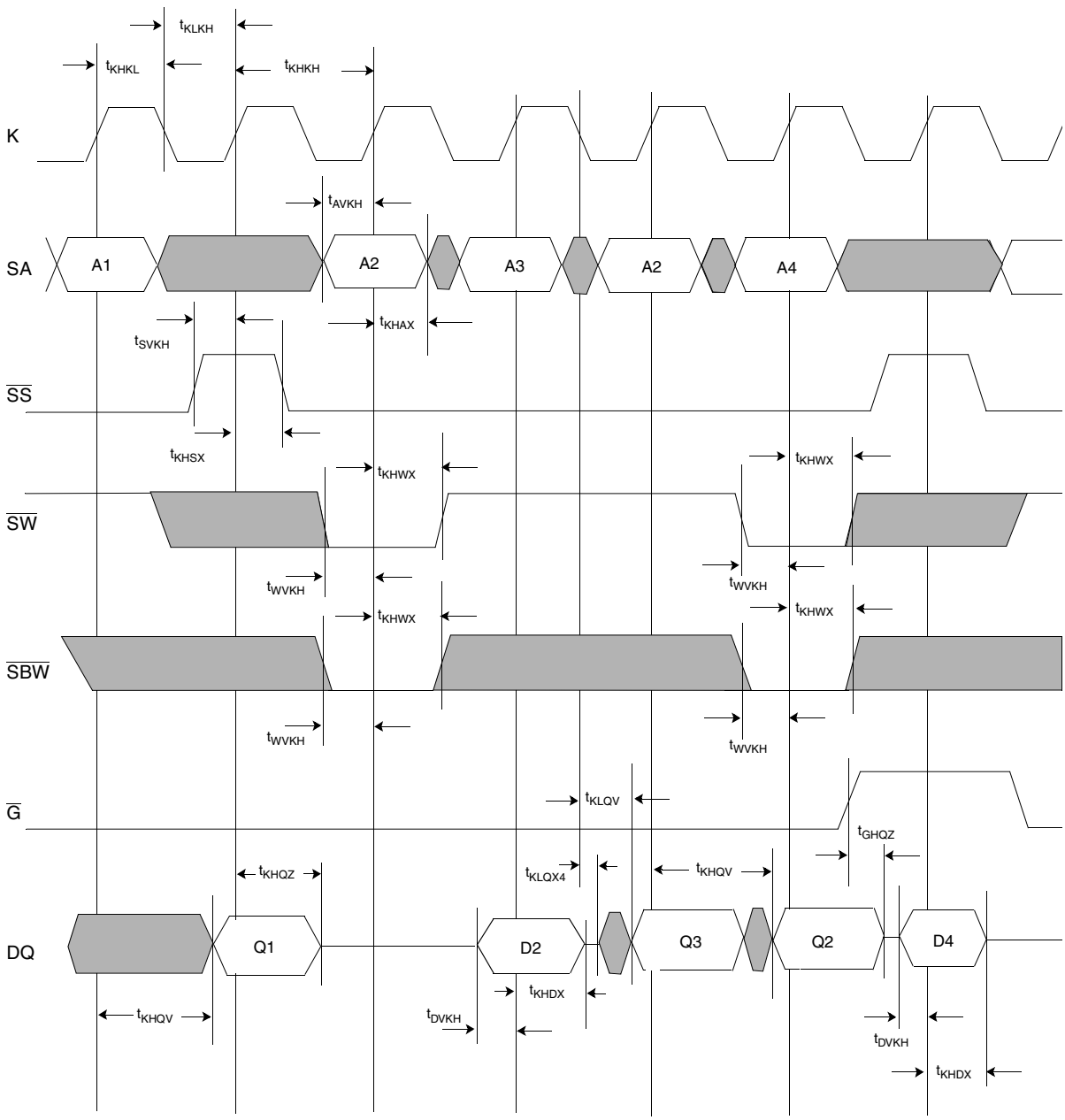
Parameter	Symbol	-4H		-5		-5H		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Cycle Time	t_{KHKH}	4.5	—	5.0	—	5.5	—	ns	
Clock High Pulse Width	t_{KHKL}	1.5	—	1.5	—	1.5	—	ns	
Clock Low Pulse Width	t_{KLKH}	1.5	—	1.5	—	1.5	—	ns	
Clock High to Output Valid	t_{KHQV}	—	4.5	—	5.0	—	5.5	ns	1
Clock Low to Output Valid	t_{KLQV}	—	2.0	—	2.25	—	2.5	ns	1
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	0.5	—	ns	
Address Hold Time	t_{KHAX}	1.0	—	1.0	—	1.0	—	ns	
Sync Select Setup Time	t_{SVKH}	0.5	—	0.5	—	0.5	—	ns	
Sync Select Hold Time	t_{KHSX}	1.0	—	1.0	—	1.0	—	ns	
Write Enables Setup Time	t_{WVKH}	0.5	—	0.5	—	0.5	—	ns	
Write Enables Hold Time	t_{KHWX}	1.0	—	1.0	—	1.0	—	ns	
Data In Setup Time	t_{DVKH}	0.5	—	0.5	—	0.5	—	ns	
Data In Hold Time	t_{KHDX}	1.0	—	1.0	—	1.0	—	ns	
Clock Low to Data Out Hold Time	t_{KLQX}	0.5	—	0.5	—	0.5	—	ns	1
Clock Low to Output Active	t_{KLQX4}	0.5	—	0.5	—	0.5	—	ns	1, 2
Clock High to Output High-Z	t_{KHQZ}	—	2.5	—	2.5	—	2.5	ns	1, 2
Output Enable to High-Z	t_{GHQZ}	—	2.5	—	2.5	—	2.5	ns	1, 2
Output Enable to Low-Z	t_{GLQX}	0.5	—	0.5	—	0.5	—	ns	1
Output Enable to Output Valid	t_{GLQV}	—	1.8	—	1.8	—	1.8	ns	1
Output Enable Setup Time	t_{GHKH}	0.5	—	0.5	—	0.5	—	ns	1
Output Enable Hold TIme	t_{KHGX}	1.5	—	1.5	—	1.5	—	ns	1
Sleep Mode Recovery TIme	t_{ZZR}	200	—	200	—	200	—	ns	
Sleep Mode Enable TIme	t_{ZZE}	—	9.0	—	10.0	—	11.0	ns	
Sync Select to ZZ Margin TIme	t_{SSZZ}	2		2		2		ns	

1. See the AC Test Loading figure on page 8.
2. Verified by design and tested without guardbands.

Read and Deselect Cycles Timing Diagram

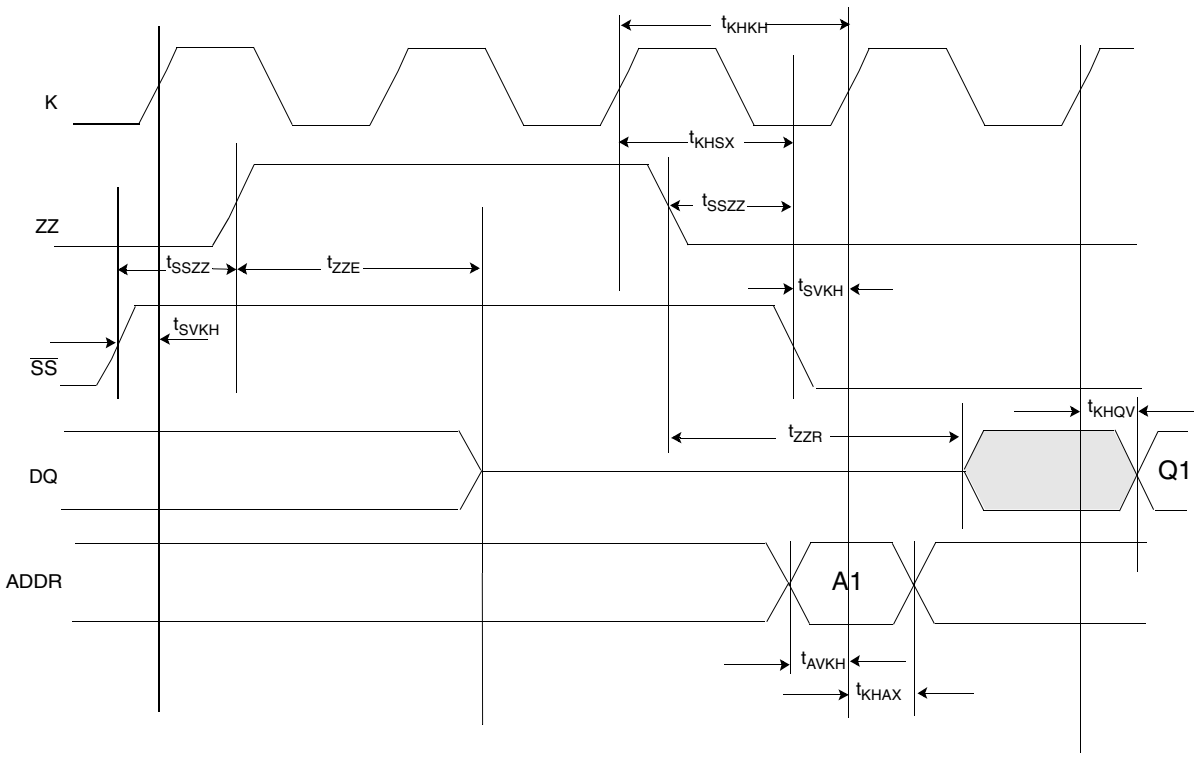


Read and Write Cycles Timing Diagram



Notes:
1. D2 is the input data written in memory location A2.
2. Q2 is output data read from the write buffer, as a result of address A2 being a match from the last write cycle address.

Asynchronous Sleep Mode Timing Diagram



IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions as defined in the IEEE Standard 1149.1 that are intended to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the SRAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a test access port (TAP) controller, instruction register, boundary scan register, bypass register, and an ID register.

The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, a test reset (TRST) signal is not required.

Signal List

- TCK: Test Clock
- TMS: Test Mode Select
- TDI: Test Data In
- TDO: Test Data Out

JTAG DC Operating Characteristics (T_A = 0 to +85°C) Operates with JEDEC Standard JESD8A (3.3V) logic signal levels

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
JTAG Input High Voltage	V_{IH1}	2.2	—	V_{DD}+0.3	V	1
JTAG Input Low Voltage	V_{IL1}	-0.3	—	0.8	V	1
JTAG Output High Level	V_{OH1}	2.4	—	—	V	1, 2
JTAG Output Low Level	V_{OL1}	—	—	0.4	V	1, 3

1. All JTAG Inputs/Outputs are LVTTL compatible only.
2. $I_{OH1} \geq$ -I8mAI.
3. $I_{OL1} \geq$ +I8mAI.

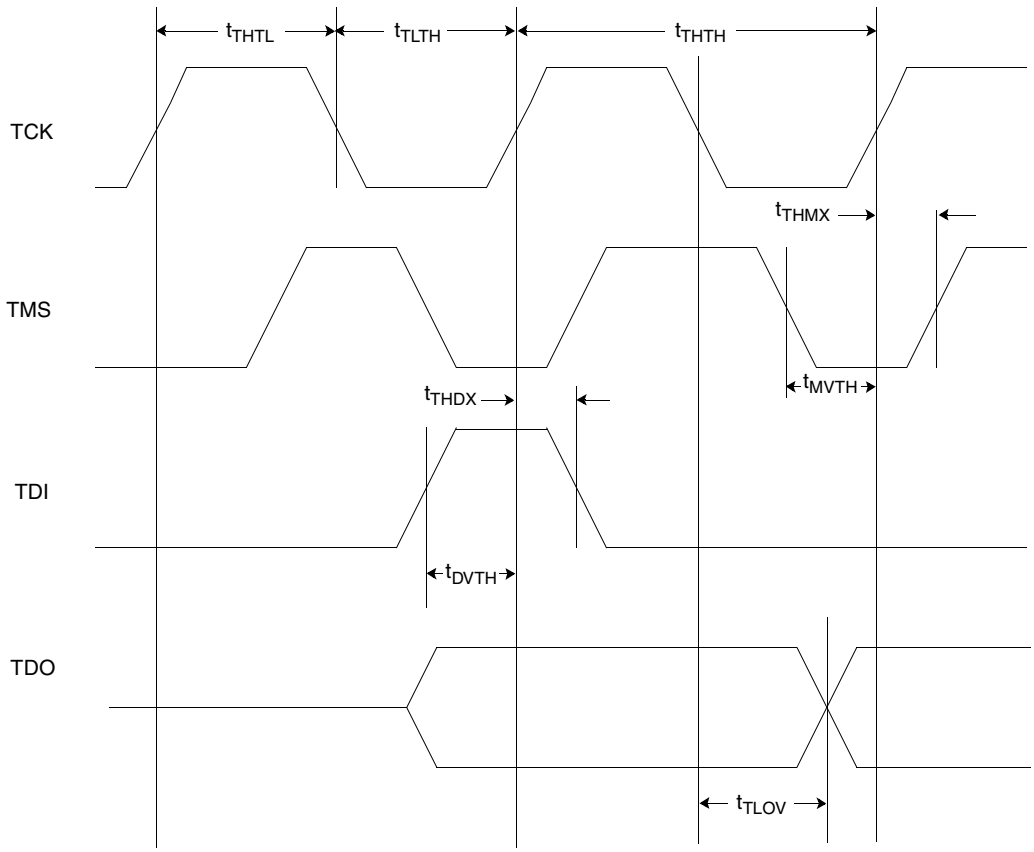
JTAG AC Test Conditions (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	V_{IH1}	3.0	V
Input Pulse Low Level	V_{IL1}	0.0	V
Input Rise Time	T_{R1}	2.0	ns
Input Fall Time	T_{F1}	2.0	ns
Input and Output Timing Reference Level		1.5	V

JTAG AC Characteristics (T_A = 0 to +85°C, V_{DD} = 3.3V -5%, +10%)

Parameter	Symbol	Min.	Max.	Units
TCK Cycle Time	t_{THTH}	20	—	ns
TCK High Pulse Width	t_{THTL}	7	—	ns
TCK Low Pulse Width	t_{TLTH}	7	—	ns
TMS Setup	t_{MVTH}	4	—	ns
TMS Hold	t_{THMX}	4	—	ns
TDI Setup	t_{DVTH}	4	—	ns
TDI Hold	t_{THDX}	4	—	ns
TCK Low to Valid Data	t_{TLOV}	—	7	ns

JTAG Timing Diagram



Scan Register Definition

Register Name	Bit Size x18	Bit Size x36
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan *	51	70

* The Boundary Scan chain consists of the following bits:
- 36 or 18 bits for Data Inputs, depending on x18 or x36 configuration
- 15 bits for SA0 - SA17 in x36, 16 bits for SA0 - SA18 in x18
- 4 bits for $\overline{\text{SBWa}}$ - $\overline{\text{SBWd}}$ in x36, 2 bits for $\overline{\text{SBWa}}$ and $\overline{\text{SBWb}}$ in x18
- 9 bits for K, $\overline{\text{K}}$, $\overline{\text{SS}}$, $\overline{\text{G}}$, $\overline{\text{SW}}$, ZZ, M1 and M2
- 7 bits for Place Holders

* K and $\overline{\text{K}}$ clocks connect to a differential receiver that generates a single-ended clock signal. This signal and its inverted value are used for Boundary Scan sampling.

ID Register Definition

Part	Field Bit Number and Description				
	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Manufacturer JEDEC Code (11:1)	Start Bit(0)
64K x 18	tbd	001 000 0011	xxxxxx	000 101 001 00	1
32K x 36	tbd	000 110 0100	xxxxxx	000 101 001 00	1

Instruction Set

Code	Instruction	Notes
000	SAMPLE-Z	1
001	IDCODE	
010	SAMPLE-Z	1
011	PRIVATE	5
100	SAMPLE	4
101	PRIVATE	5
110	PRIVATE	5
111	BYPASS	2, 3

1. Places DQs in High-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the Shift DR state.
4. SAMPLE instruction does not place DQs in High-Z.
5. This instruction is reserved for the exclusive use of IBM. Invoking this instruction will cause improper SRAM functionality.

List of IEEE 1149.1 Standard Violations

- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

Boundary Scan Order (32K x 36)) (PH = Place Holder)

Exit Order	Signal	Bump #	Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	25	DQ12	6F	49	DQ26	2H
2	SA	4P	26	DQ13	7E	50	DQ25	1H
3	SA	4T	27	DQ11	6E	51	$\overline{SBW}$c	3G
4	SA	6R	28	DQ10	7D	52	PH[2]	4D
5	SA	5T	29	DQ9	6D	53	$\overline{SS}$	4E
6	ZZ	7T	30	SA	6A	54	PH[1]	4G
7	DQ0	6P	31	SA	6C	55	PH[2]	4H
8	DQ1	7P	32	SA	5C	56	$\overline{SW}$	4M
9	DQ2	6N	33	SA	5A	57	$\overline{SBW}$d	3L
10	DQ4	7N	34	PH[1]	6B	58	DQ34	1K
11	DQ3	6M	35	PH[1]	5B	59	DQ35	2K
12	DQ5	6L	36	PH[1]	3B	60	DQ33	1L
13	DQ6	7L	37	PH[1]	2B	61	DQ32	2L
14	DQ8	6K	38	SA	3A	62	DQ30	2M
15	DQ7	7K	39	SA	3C	63	DQ29	1N
16	$\overline{SBW}$a	5L	40	SA	2C	64	DQ31	2N
17	$\overline{K}$	4L	41	SA	2A	65	DQ28	1P
18	K	4K	42	DQ18	2D	66	DQ27	2P
19	$\overline{G}$	4F	43	DQ19	1D	67	SA	3T
20	$\overline{SBW}$b	5G	44	DQ20	2E	68	SA	2R
21	DQ16	7H	45	DQ22	1E	69	SA	4N
22	DQ17	6H	46	DQ21	2F	70	M1	3R
23	DQ15	7G	47	DQ23	2G			
24	DQ14	6G	48	DQ24	1G			

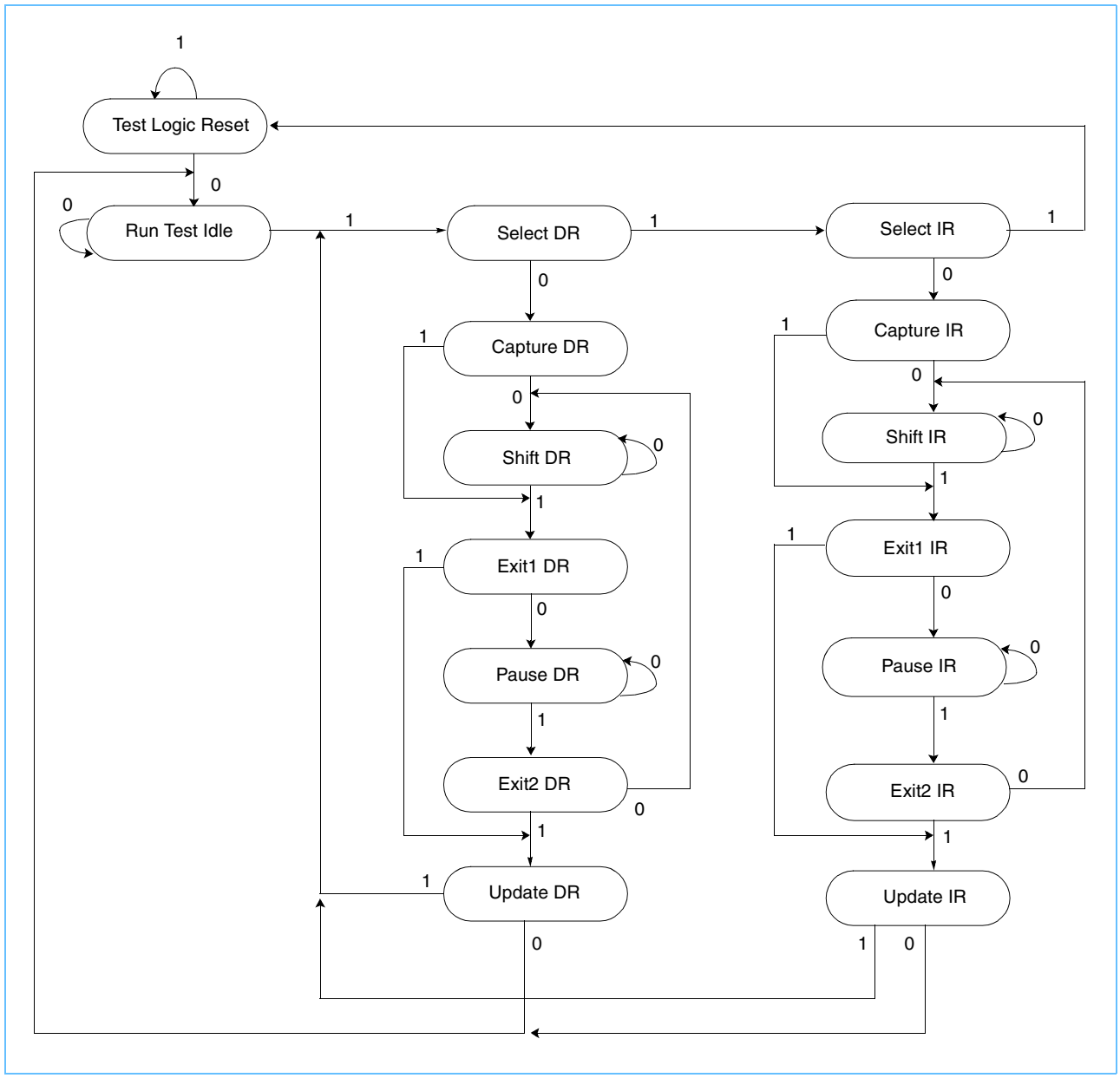
1. Input of PH register connected to V_{SS}.
2. Input of PH register connected to V_{DD}.

Boundary Scan Order (64K x 18)) (PH = Place Holder)

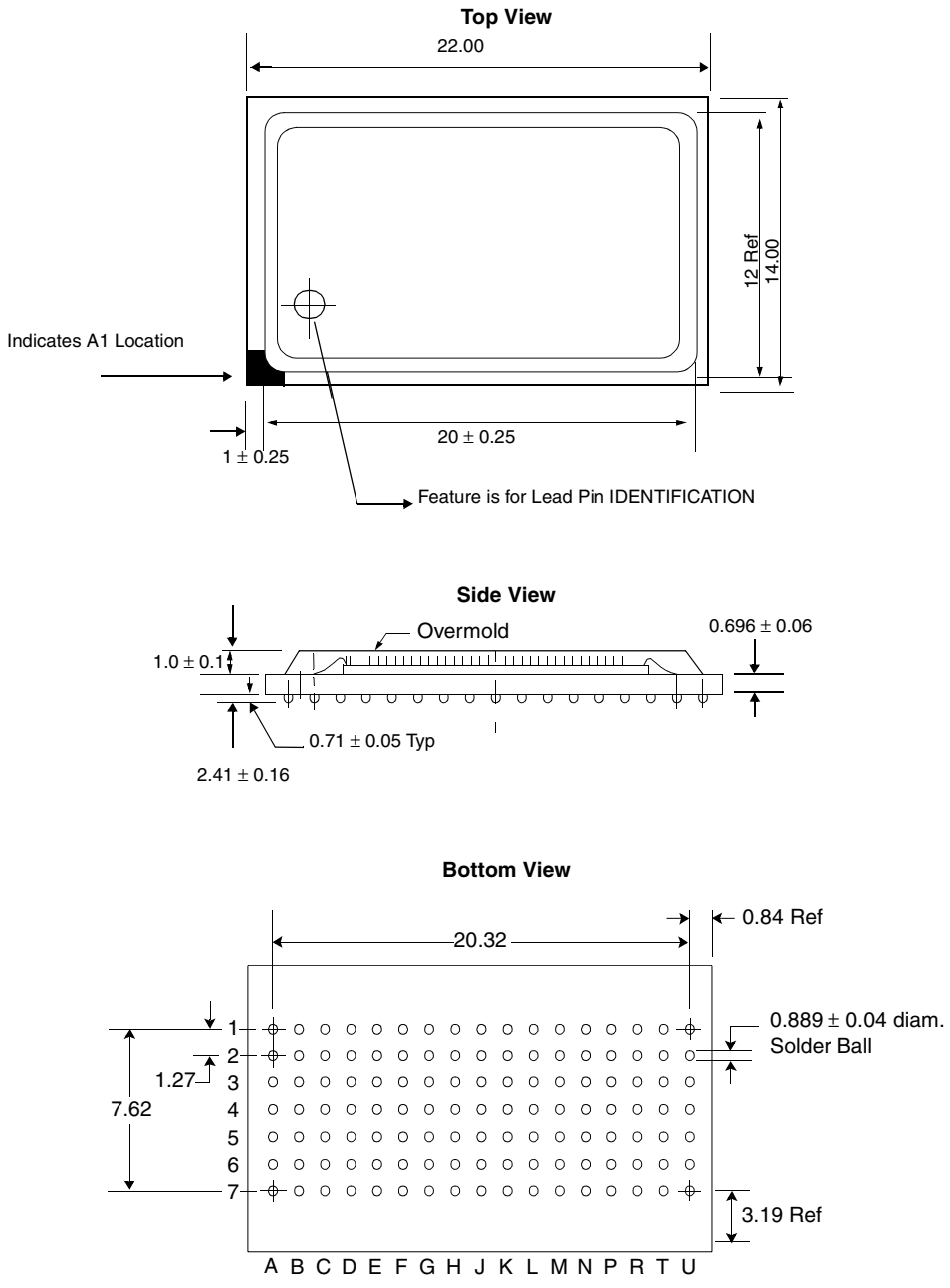
Exit Order	Signal	Bump #	Exit Order	Signal	Bump #
1	M2	5R	27	PH[1]	2B
2	SA	6T	28	SA	3A
3	SA	4P	29	SA	3C
4	SA	6R	30	SA	2C
5	SA	5T	31	SA	2A
6	ZZ	7T	32	DQ14	1D
7	DQ5	7P	33	DQ15	2E
8	DQ6	6N	34	DQ16	2G
9	DQ7	6L	35	DQ17	1H
10	DQ8	7K	36	$\overline{SBWb}$	3G
11	$\overline{SBWa}$	5L	37	PH[2]	4D
12	$\overline{K}$	4L	38	$\overline{SS}$	4E
13	K	4K	39	PH[1]	4G
14	$\overline{G}$	4F	40	PH[2]	4H
15	DQ4	6H	41	$\overline{SW}$	4M
16	DQ3	7G	42	DQ13	2K
17	DQ2	6F	43	DQ12	1L
18	DQ1	7E	44	DQ10	2M
19	DQ0	6D	45	DQ11	1N
20	SA	6A	46	DQ9	2P
21	SA	6C	47	SA	3T
22	SA	5C	48	SA	2R
23	SA	5A	49	SA	4N
24	PH[1]	6B	50	SA	2T
25	PH[1]	5B	51	M1	3R
26	PH[1]	3B			

1. Input of PH register connected to V_{SS}.
2. Input of PH register connected to V_{DD}.

TAP Controller State Machine



7 x17 BGA Dimensions



Note: All dimensions are in millimeters

References

The following documents give recommendations, restrictions, and limitations for 2nd level attach process:

Double Sided 4Mb SRAM Coupled Cap PBGA Card Assembly Guide

Qualification information, including the scope of application conditions qualified, is available from your IBM sales representative.

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Revision Log

Revision	Contents of Modification
08/06/2001	Initial Release (00).

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