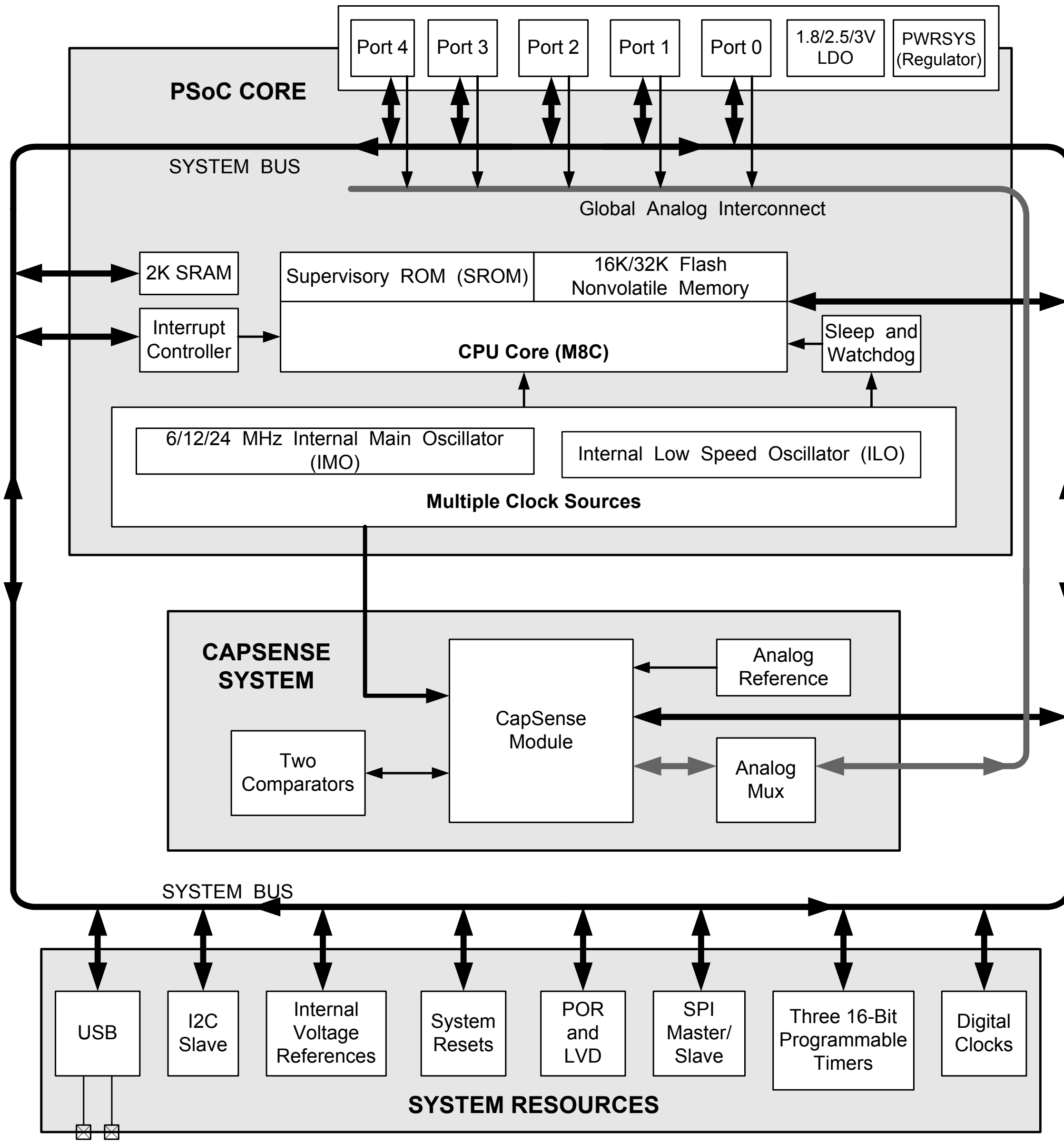
CY8C20x46, CY8C20x66

CapSense™ Applications

Features

- **Low Power CapSense™ Block**
  - Configurable Capacitive Sensing Elements
  - Supports Combination of CapSense Buttons, Sliders, Touchpads, TouchScreens, and Proximity Sensors
- **Powerful Harvard Architecture Processor**
  - M8C Processor Speeds Running to 24 MHz
  - Low Power at High Speed
  - Interrupt Controller
  - 1.71V to 5.5V Operating Voltage
  - Temperature Range: – 40°C to +85°C
- **Flexible On-Chip Memory**
  - Two Program Storage Size Options
    - CY8C20x46: 16K Flash
    - CY8C20x66: 32K Flash
  - 50,000 Erase/Write Cycles
  - 2048 Bytes SRAM Data Storage
  - Partial Flash Updates
  - Flexible Protection Modes
  - In-System Serial Programming (ISSP)
- **Full-Speed USB (12 Maps)**
  - Eight Uni-Directional Endpoints
  - One Bi-Directional Control Endpoint
  - USB 2.0 Compliant
  - Dedicated 512 Byte Buffer
  - Internal 3.3V Output Regulator
  - Available on 48-Pin QFN and 48-Pin SSOP packages only
  - Operating voltage with USB enabled:
    - 3.15 to 3.45V when supply voltage is around 3.3V
    - 4.35 to 5.25V when supply voltage is around 5.0V
- **Complete Development Tools**
  - Free Development Tool (PSoC Designer™)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Trace Memory
- **Precision, Programmable Clocking**
  - Internal ± 5.0% 6/12/24 MHz Main Oscillator
  - Internal Low Speed Oscillator at 32 kHz for Watchdog and Sleep
  - Optional External 32 kHz Crystal
  - 0.25% Accuracy for USB with No External Components
- **Programmable Pin Configurations**
  - 25 mA Sink Current on All GPIO
  - Pull Up, High Z, Open Drain Drive Modes on All GPIO
  - CMOS Drive Mode on Ports 0 and 1
  - Up to 36 Analog Inputs on GPIO
  - Configurable Inputs on All GPIO
  - Selectable, Regulated Digital IO on Port 1
  - Configurable Input Threshold for Port 1
  - 3.0V, 20 mA Total Port 1 Source Current
  - 5 mA Source Current Mode on Ports 0 and 1
  - Hot-Swap Capability on all Port1 GPIO
- **Versatile Analog Mux**
  - Common Internal Analog Bus
  - Simultaneous Connection of IO Combinations
  - High PSRR Comparator
  - Low Dropout Voltage Regulator for the Analog Array
- **Additional System Resources**
  - I^2C™ Slave
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - Implementation Requires No Clock Stretching
    - Implementation During Sleep Modes with Less Than 100 μA
    - Hardware Address Detection
  - SPI™ Master and SPI Slave
    - Configurable Between 46.9 kHz – 12 MHz
  - Three 16-Bit Timers
  - Watchdog and Sleep Timers
  - Internal Voltage Reference
  - Integrated Supervisory Circuit
- **Package Options**
  - 16-Pin 3x3 x 0.6 mm QFN
  - 24-Pin 4x4 x 0.6 mm QFN
  - 32-Pin 5x5 x 0.6 mm QFN
  - 48-Pin 7x7 x 1.0 mm QFN (CY8C20x66 only)
  - 48-Pin SSOP

Block Diagram



PSoC® Functional Overview

The PSoC family consists of many *Mixed-Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, as well as programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The architecture for this device family, as illustrated above, is comprised of three main areas: the Core, the CapSense Analog System, and the System Resources (including a full-speed USB port). A common, versatile bus allows connection between IO and the analog system. Each CY8C20x46/CY8C20x66 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 general purpose IO (GPIO) are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO (internal main oscillator) and ILO (internal low speed oscillator). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-MIPS, 8-bit Harvard architecture microprocessor.

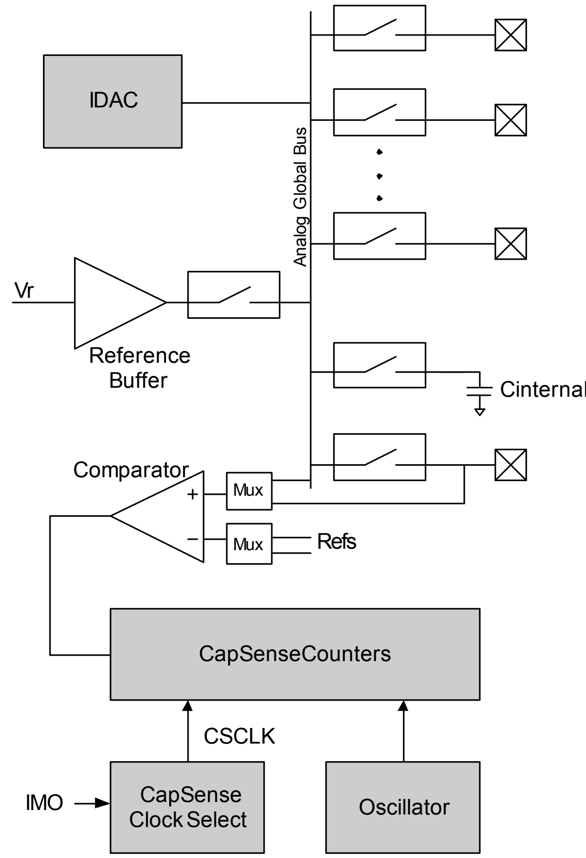
System Resources provide additional capability, such as configurable USB and I2C slave/SPI master-slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

The Analog System is composed of the CapSense PSoC block and an internal 1.2V analog reference, which together support capacitive sensing of up to 36 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



The Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any IO pin.
- Crosspoint connection between any IO pin combinations.

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements Application Notes, which can be found under http://www.cypress.com >> Documentation >> Application Notes. In general, and unless otherwise noted in the relevant Application Notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over 3 or 4 wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I2C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power-On-Reset) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- The 5.5V maximum input, 1.8/2.5/3V-selectable output, low-dropout regulator (LDO) provides regulation for IOs. A register-controlled bypass mode allows the user to disable the LDO.
- Standard Cypress PSoC IDE tools are available for debugging the CY8C20x46/CY8C20x66 family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug a Power PSoC design. A custom bonded On-Chip Debug (OCD) device is available in an 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC Mixed-Signal Array Technical Reference Manual*, which can be found on http://www.cypress.com/psoc.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com/shop/. Under Product Categories click PSoC® Mixed Signal Arrays to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to http://www.cypress.com/techtrain.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Support located at the top of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a four hour guaranteed response at http://www.cypress.com/support.

Application Notes

A long list of application notes assists you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Documentation list located at the top of the web page. Application notes are sorted by date by default.

Development Tools

PSoC Designer™ is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows XP and Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

The system-level view is a drag-and-drop visual embedded system design environment based on PSoC Express. In this view you solve design problems the same way you might think about the system. Select input and output devices based upon system requirements. Add a communication interface and define the interface to the system (registers). Define when and how an output device changes state based upon any/all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.x. You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of pre-built, pre-tested hardware peripheral components. In the system-level view these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view the components are called “user modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed-signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the IO pins, or connect system-level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog-to-digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, you perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 1. Acronyms

Acronym	Description
AC	alternating current
API	application programming interface
CPU	central processing unit
DC	direct current
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
SLIMO	slow IMO
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Units of Measure lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

Pin Information

This section describes, lists, and illustrates the CY8C20x46/CY8C20x66 PSoC device pins and pinout configurations.

The CY8C20x46/CY8C20x66 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO and connection to the common analog bus. However, Vss, Vdd, and XRES are not capable of Digital IO.

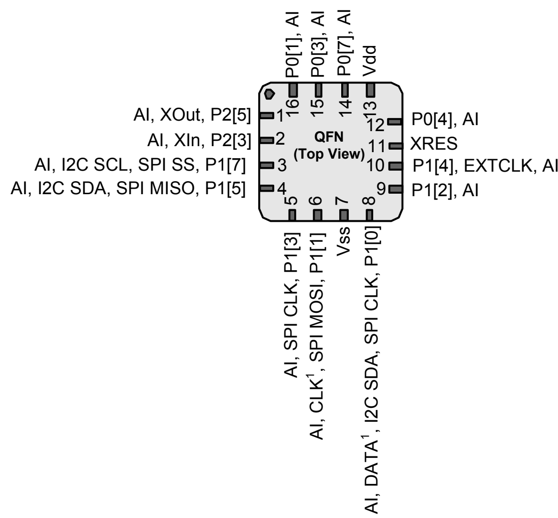
16-Pin Part Pinout

Table 2. 16-Pin QFN Part Pinout[2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P2[5]	Crystal output (XOut).
2	IO	I	P2[3]	Crystal input (XIn).
3	IOHR	I	P1[7]	I2C SCL, SPI SS.
4	IOHR	I	P1[5]	I2C SDA, SPI MISO.
5	IOHR	I	P1[3]	SPI CLK.
6	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI.
7	Power		Vss	Ground connection.
8	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK.
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull down.
12	IOH	I	P0[4]	
13	Power		Vdd	Supply voltage.
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input.
16	IOH	I	P0[1]	Integrating input.

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C20246, CY8C20266 16-Pin PSoC Device



Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset).
2. During power up or reset event, device P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter any issues.

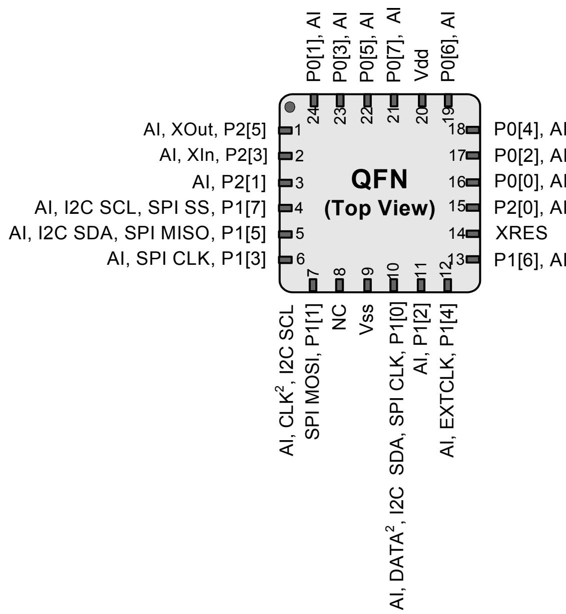
24-Pin Part Pinout

Table 3. 24-Pin QFN Part Pinout[2, 3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I	P2[5]	Crystal output (XOut).
2	IO	I	P2[3]	Crystal input (XIn).
3	IO	I	P2[1]	
4	IOHR	I	P1[7]	I2C SCL, SPI SS.
5	IOHR	I	P1[5]	I2C SDA, SPI MISO.
6	IOHR	I	P1[3]	SPI CLK.
7	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI.
8			NC	No connection.
9	Power		Vss	Ground connection.
10	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK.
11	IOHR	I	P1[2]	
12	IOHR	I	P1[4]	Optional external clock input (EXTCLK).
13	IOHR	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull down.
15	IO	I	P2[0]	
16	IOH	I	P0[0]	
17	IOH	I	P0[2]	
18	IOH	I	P0[4]	
19	IOH	I	P0[6]	
20	Power		Vdd	Supply voltage.
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input.
24	IOH	I	P0[1]	Integrating input.
CP	Power		Vss	Center pad must be connected to ground.

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20346, CY8C20366 24-Pin PSoC Device



Note
3. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

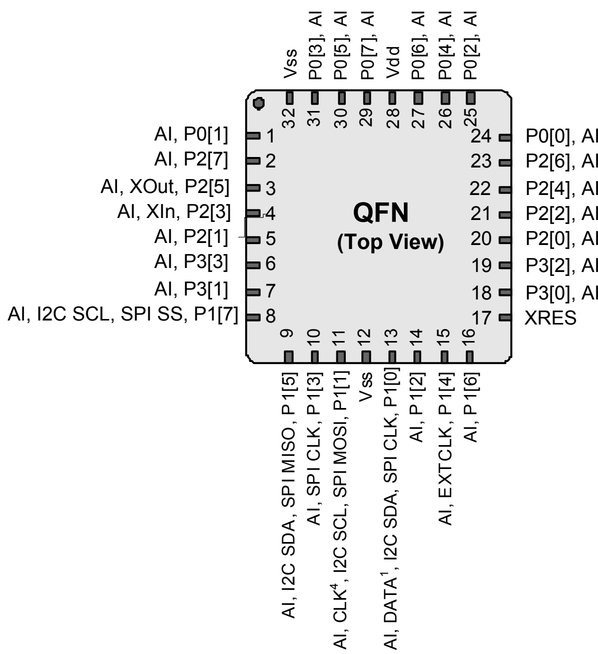
32-Pin Part Pinout

Table 4. 32-Pin QFN Part Pinout (2, 3)

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input.
2	IO	I	P2[7]	
3	IO	I	P2[5]	Crystal output (XOut)
4	IO	I	P2[3]	Crystal input (XIn)
5	IO	I	P2[1]	
6	IO	I	P3[3]	
7	IO	I	P3[1]	
8	IOHR	I	P1[7]	I2C SCL, SPI SS.
9	IOHR	I	P1[5]	I2C SDA, SPI MISO.
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK(1), I2C SCL, SPI MOSI.
12	Power		Vss	Ground connection.
13	IOHR	I	P1[0]	ISSP DATA(1), I2C SDA., SPI CLK
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK).
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull down.
18	IO	I	P3[0]	
19	IO	I	P3[2]	
20	IO	I	P2[0]	
21	IO	I	P2[2]	
22	IO	I	P2[4]	
23	IO	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		Vdd	Supply voltage.
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input.
32	Power		Vss	Ground connection.
CP	Power		Vss	Center pad must be connected to ground.

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 4. CY8C20446, CY8C20466 32-Pin PSoC Device



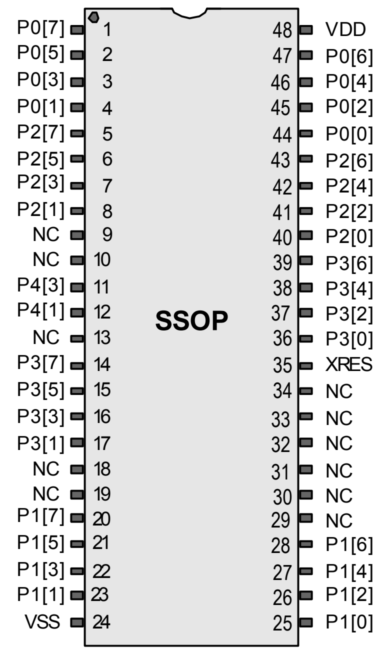
48-Pin SSOP Part Pinout

Table 5. 48-Pin SSOP Part Pinout[2]

Pin No.	Digital	Analog	Name	Description
1	IOH	IO	P0[7]	
2	IOH	IO	P0[5]	
3	IOH	IO	P0[3]	
4	IOH	IO	P0[1]	
5	IO	IO	P2[7]	
6	IO	IO	P2[5]	XTAL Out
7	IO	IO	P2[3]	XTAL In
8	IO	IO	P2[1]	
9			NC	No connection
10			NC	No connection
11	IO	IO	P4[3]	
12	IO	IO	P4[1]	
13			NC	No connection
14	IO	IO	P3[7]	
15	IO	IO	P3[5]	
16	IO	IO	P3[3]	
17	IO	IO	P3[1]	
18			NC	No connection
19			NC	No connection
20	IOHR	IO	P1[7]	I2C SCL, SPI SS
21	IOHR	IO	P1[5]	I2C SDA, SPI MISO
22	IOHR	IO	P1[3]	SPI CLK
23	IOHR	IO	P1[1]	TC CLK[1], I2C SCL, SPI MOSI
24			VSS	Ground Pin
25	IOHR	IO	P1[0]	TC DATA[1], I2C SDA, SPI CLK
26	IOHR	IO	P1[2]	
27	IOHR	IO	P1[4]	EXT CLK
28	IOHR	IO	P1[6]	
29			NC	No connection
30			NC	No connection
31			NC	No connection
32			NC	No connection
33			NC	No connection
34			NC	No connection
35			XRES	Active high external reset with internal pull down
36	IO	IO	P3[0]	
37	IO	IO	P3[2]	
38	IO	IO	P3[4]	
39	IO	IO	P3[6]	
40	IO	IO	P2[0]	
41	IO	IO	P2[2]	
42	IO	IO	P2[4]	
43	IO	IO	P2[6]	
44	IOH	IO	P0[0]	
45	IOH	IO	P0[2]	
46	IOH	IO	P0[4]	
47	IOH	IO	P0[6]	
48	Power		Vdd	Power Pin

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, H = 5 mA High Output Drive, R = Regulated Output Option.

Figure 5. CY8C20546, CY8C20566-48-Pin SSOP PSoC Device

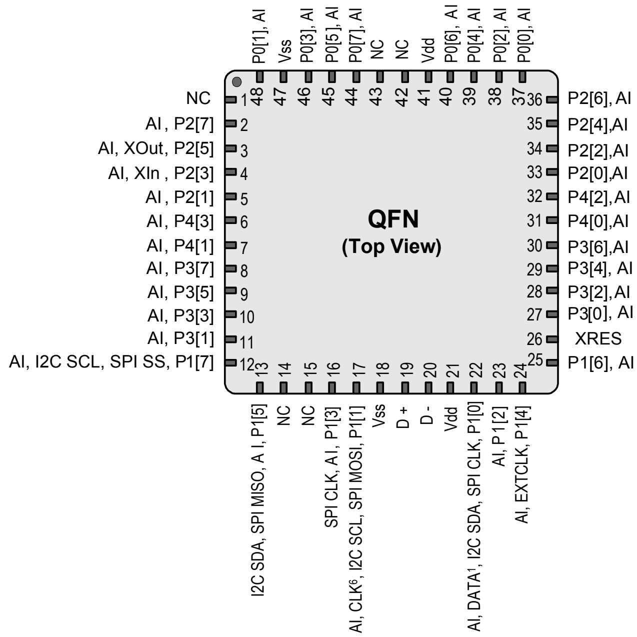


48-Pin QFN Part Pinout

Table 6. 48-Pin QFN Part Pinout (2, 3)

Pin No.	Digital	Analog	Name	Description
1			NC	No connection.
2	IO	I	P2[7]	
3	IO	I	P2[5]	Crystal output (XOut).
4	IO	I	P2[3]	Crystal input (XIn).
5	IO	I	P2[1]	
6	IO	I	P4[3]	
7	IO	I	P4[1]	
8	IO	I	P3[7]	
9	IO	I	P3[5]	
10	IO	I	P3[3]	
11	IO	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS.
13	IOHR	I	P1[5]	I2C SDA, SPI MISO.
14			NC	No connection.
15			NC	No connection.
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK(1), I2C SCL, SPI MOSI.
18	Power		Vss	Ground connection.
19	IO		D+	
20	IO		D-	
21	Power		Vdd	Supply voltage.
22	IOHR	I	P1[0]	ISSP DATA(1), I2C SDA, SPI CLK.
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK).
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down.
27	IO	I	P3[0]	
28	IO	I	P3[2]	
29	IO	I	P3[4]	
30	IO	I	P3[6]	
31	IO	I	P4[0]	
32	IO	I	P4[2]	
33	IO	I	P2[0]	
34	IO	I	P2[2]	
35	IO	I	P2[4]	
36	IO	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage.
42			NC	No connection.
43			NC	No connection.
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input.
47	Power		Vss	Ground connection.
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground.

Figure 6. CY8C20666 48-Pin QFN PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

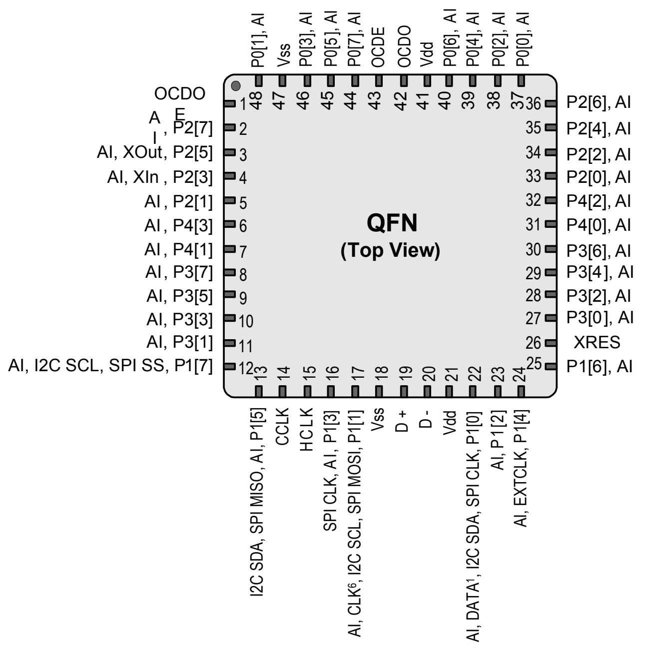
48-Pin QFN OCD Part Pinout

The 48-pin QFN part is for the CY8C20066 On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.[4]

Table 7. 48-Pin OCD QFN Part Pinout [2, 3]

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin.
2	IO	I	P2[7]	
3	IO	I	P2[5]	Crystal output (XOut).
4	IO	I	P2[3]	Crystal input (XIn).
5	IO	I	P2[1]	
6	IO	I	P4[3]	
7	IO	I	P4[1]	
8	IO	I	P3[7]	
9	IO	I	P3[5]	
10	IO	I	P3[3]	
11	IO	I	P3[1]	
12	IOHR	I	P1[7]	I2C SCL, SPI SS.
13	IOHR	I	P1[5]	I2C SDA, SPI MISO.
14			CCLK	OCD CPU clock output.
15			HCLK	OCD high speed clock output.
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK[1], I2C SCL, SPI MOSI.
18	Power		Vss	Ground connection.
19	IO		D+	
20	IO		D-	
21	Power		Vdd	Supply voltage.
22	IOHR	I	P1[0]	ISSP DATA[1], I2C SDA, SPI CLK.
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK).
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down.
27	IO	I	P3[0]	
28	IO	I	P3[2]	
29	IO	I	P3[4]	
30	IO	I	P3[6]	
31	IO	I	P4[0]	
32	IO	I	P4[2]	
33	IO	I	P2[0]	
34	IO	I	P2[2]	
35	IO	I	P2[4]	
36	IO	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		Vdd	Supply voltage.
42			OCDO	OCD even data IO.
43			OCDE	OCD odd data output.
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input.
47	Power		Vss	Ground connection.
48	IOH	I	P0[1]	
CP	Power		Vss	Center pad must be connected to ground.

Figure 7. CY8C20066 48-Pin OCD PSoC Device



LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Note
4. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x46/CY8C20x66 PSoC devices. For the most up-to-date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Figure 8. Voltage versus CPU Frequency

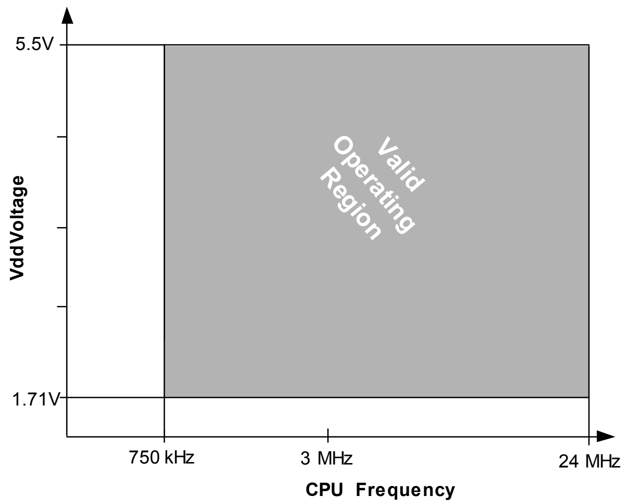
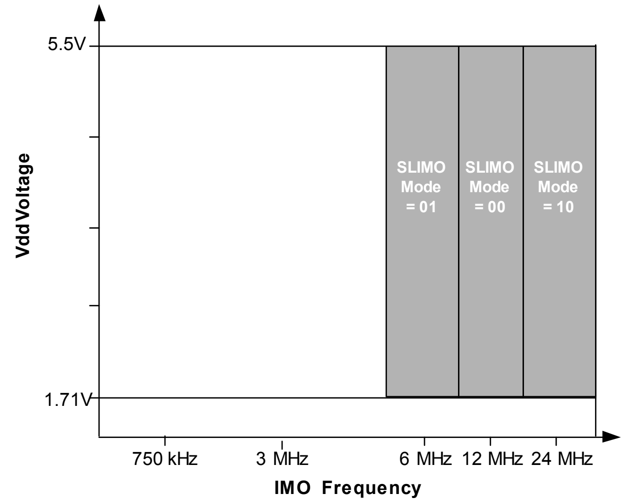


Figure 9. IMO Frequency Trim Options



The following table lists the units of measure that are used in this section.

Table 8. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mA	milli-ampere
dB	decibels	ms	milli-second
fF	femto farad	mV	milli-volts
Hz	hertz	nA	nanoampere
KB	1024 bytes	ns	nanosecond
Kbit	1024 bits	nV	nanovolts
kHz	kilohertz	Ω	ohm
ksps	kilo samples per second	pA	picoampere
kΩ	kilohm	pF	picofarad
MHz	megahertz	pp	peak-to-peak
MΩ	megaohm	ppm	parts per million
µA	microampere	ps	picosecond
µF	microfarad	sps	samples per second
µH	microhenry	s	sigma: one standard deviation
µs	microsecond	V	volts
µW	microwatts		

Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40°C <= TA <= 85°C, 1.71V <= Vdd <= 5.5V.

Table 9. Comparator User Module Electrical Specifications

Symbol	Description	Min	Typ	Max	Units	Conditions
T_{COMP}	Comparator Response Time		70	100	ns	50 mV overdrive
Offset			2.5	30	mV	
Current			20	80	µA	Average DC current, 50 mV overdrive
PSRR	Supply voltage >2V		80		dB	Power Supply Rejection Ratio
	Supply voltage <2V		40		dB	Power Supply Rejection Ratio
Input Range		0		1.5	V	

ADC Electrical SpecificationsAbsolute Maximum

Table 10. ADC User Module Electrical Specifications

Symbol	Description	Min	Typ	Max	Units	Conditions
	Input					
V_{IN}	Input Voltage Range	Vss		1.3	V	This gives 72% of maximum code
C_{IN}	Input Capacitance			5	pF	
	Resolution	8		10	Bits	Settings 8, 9, or 10
-	8-Bit Sample Rate		23.4375		ksps	Data Clock set to 6 MHz. Sample Rate = 0.001/(2^Resolution/Data clock)
-	10-Bit Sample Rate		5.859		ksps	Data Clock set to 6 MHz. Sample Rate = 0.001/(2^Resolution/Data clock)
	DC Accuracy					
-	DNL	-1		+2	LSB	For any configuration
-	INL	-2		+2	LSB	For any configuration
-	Offset Error	0	15	90	mV	
I_{ADC}	Operating Current		275	350	µA	
F_{CLK}	Data Clock	2.25		12	MHz	Source is chip's internal main oscillator. See device data sheet for accuracy.
	Monotonicity					Not guaranteed. See DNL
PSRR	Power Supply Rejection Ration					
-	PSRR (Vdd>3.0V)		24	dB		
-	PSRR (2.2 < Vdd < 3.0)		30	dB		
-	PSRR (2.0 < Vdd < 2.2)		12	dB		
-	PSRR (Vdd < 2.0)		0	dB		
	Gain Error	1		5	%FSR	For any resolution
R_{IN}	Input Resistance	1/ (500fF*Data-Clock)	1/ (400fF*Data-Clock)	1/ (300fF*Data-Clock)	Ω	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution.

Ratings

Table 11. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage Temperature	Higher storage temperatures reduces data retention time. Recommended Storage Temperature is +25°C ± 25°C. Extended duration storage temperatures above 85°C degrades reliability.	–55	+25	+125	°C
Vdd	Supply Voltage Relative to Vss		–0.5	–	+6.0	V
V_{IO}	DC Input Voltage		Vss – 0.5	–	Vdd + 0.5	V
V_{IOZ}	DC Voltage Applied to Tri-state		Vss –0.5	–	Vdd + 0.5	V
I_{MIO}	Maximum Current into any Port Pin		–25	–	+50	mA
ESD	Electro Static Discharge Voltage	Human Body Model ESD	2000	–	–	V
LU	Latch-up Current	In accordance with JESD78 standard	–	–	200	mA

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient Temperature		–40	–	+85	°C
T_J	Operational Die Temperature	The temperature rise from ambient to junction is package specific. See the table Thermal Impedances per Package on page 28. The user must limit the power consumption to comply with this requirement.	–40	–	+100	°C

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd	Supply Voltage	See the table DC POR and LVD Specifications on page 20	1.71	–	5.5	V
I_{DD24}	Supply Current, IMO = 24 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 24 MHz. CapSense running at 12 MHz, no IO sourcing current	–	2.88	4.0	mA
I_{DD12}	Supply Current, IMO = 12 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 12 MHz. CapSense running at 12 MHz, no IO sourcing current	–	1.71	2.6	mA
I_{DD6}	Supply Current, IMO = 6 MHz	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 6 MHz. CapSense running at 6 MHz, no IO sourcing current	–	1.16	1.8	mA
I_{SB0}	Deep Sleep Current	Vdd = 3.0V, T_A = 25°C, IO regulator turned off	–	0.1	–	µA
I_{SB1}	Standby Current with POR, LVD and Sleep Timer	Vdd = 3.0V, T_A = 25°C, IO regulator turned off	–	1.07	1.5	µA

DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0V to 5.5V and –40°C ≤ T_A ≤ 85°C, 2.4V to 3.0V and –40°C ≤ T_A ≤ 85°C, or 1.71V to 2.4V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 14. 3.0V to 5.5V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH ≤ 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 1 mA, maximum of 20 mA source current in all IOs	Vdd - 0.9	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 5 mA, maximum of 20 mA source current in all IOs	Vdd - 0.9	–	–	V
V_{OH5}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH < 10 µA, Vdd > 3.1V, maximum of 4 IOs all sourcing 5 mA	2.85	3.00	3.3	V
V_{OH6}	High Output Voltage Port 1 Pins with LDO Regulator Enabled for 3V Out	IOH = 5 mA, Vdd > 3.1V, maximum of 20 mA source current in all IOs	2.20	–	–	V
V_{OH7}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH < 10 µA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	2.35	2.50	2.75	V
V_{OH8}	High Output Voltage Port 1 Pins with LDO Enabled for 2.5V Out	IOH = 2 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.90	–	–	V
V_{OH9}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 µA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.60	1.80	2.1	V
V_{OH10}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, Vdd > 2.7V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V_{OL}	Low Output Voltage	IOL = 25 mA, Vdd > 3.3V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.80	V
V_{IH}	Input High Voltage		2.00	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Pin Capacitance	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 15. 2.4V to 3.0V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH < 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 0.2 mA, maximum of 10 mA source current in all IOs	Vdd - 0.4	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH < 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all IOs	Vdd - 0.5	–	–	V
V_{OH5A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH < 10 µA, Vdd > 2.4V, maximum of 20 mA source current in all IOs	1.50	1.80	2.1	V
V_{OH6A}	High Output Voltage Port 1 Pins with LDO Enabled for 1.8V Out	IOH = 1 mA, Vdd > 2.4V, maximum of 20 mA source current in all IOs	1.20	–	–	V
V_{OL}	Low Output Voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input Low Voltage		–	–	0.72	V
V_{IH}	Input High Voltage		1.4	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25^oC	0.5	1.7	5	pF

Table 16. 1.71V to 2.4V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull up Resistor		4	5.6	8	kΩ
V_{OH1}	High Output Voltage Port 2 or 3 Pins	IOH = 10 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH2}	High Output Voltage Port 2 or 3 Pins	IOH = 0.5 mA, maximum of 10 mA source current in all IOs	Vdd - 0.5	–	–	V
V_{OH3}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 100 µA, maximum of 10 mA source current in all IOs	Vdd - 0.2	–	–	V
V_{OH4}	High Output Voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	IOH = 2 mA, maximum of 10 mA source current in all IOs	Vdd - 0.5	–	–	V
V_{OL}	Low Output Voltage	IOL = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.4	V
V_{IL}	Input Low Voltage		–	–	0.3 x Vdd	V

Table 16. 1.71V to 2.4V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		0.65 x Vdd	–		V
V_H	Input Hysteresis Voltage		–	80	–	mV
I_{IL}	Input Leakage (Absolute Value)		–	0.001	1	µA
C_{PIN}	Capacitive Load on Pins	Package and pin dependent Temp = 25°C	0.5	1.7	5	pF

Table 17.DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ Pull Up Resistance	With idle bus	0.900	-	1.575	kΩ
Rusba	USB D+ Pull Up Resistance	While receiving traffic	1.425	-	3.090	kΩ
Vohusb	Static Output High		2.8	-	3.6	V
Volusb	Static Output Low			-	0.3	V
Vdi	Differential Input Sensitivity		0.2	-		V
Vcm	Differential Input Common Mode Range		0.8	-	2.5	V
Vse	Single Ended Receiver Threshold		0.8	-	2.0	V
Cin	Transceiver Capacitance			-	50	pF
Iio	Hi-Z State Data Line Leakage	On D+ or D- line	-10	-	+10	µA
Rps2	PS/2 Pull Up Resistance		3	5	7	kΩ
Rext	External USB Series Resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch Resistance to Common Analog Bus		–	–	800	Ω
R_{GND}	Resistance of Initialization Switch to Vss		–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8V

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low Power Comparator (LPC) common mode	Maximum voltage limited to Vdd	0.0	–	1.8	V
I_{LPC}	LPC supply current		–	10	40	µA
V_{OSLPC}	LPC voltage offset		–	2.5	30	mV

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
 V_{PPOR0} V_{PPOR1} V_{PPOR2} V_{PPOR3}	Vdd Value for PPOR Trip PORLEV[1:0] = 00b, HPOR = 0 PORLEV[1:0] = 00b, HPOR = 1 PORLEV[1:0] = 01b, HPOR = 1 PORLEV[1:0] = 10b, HPOR = 1	Vdd must be greater than or equal to 1.71V during startup, reset from the XRES pin, or reset from watchdog.	 1.61 – 	 1.66 2.36 2.60 2.82	 1.71 2.41 2.66 2.95	 V V V V
 V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	Vdd Value for LVD Trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b		 2.40[5] 2.64[6] 2.85[7] 2.95 3.06 1.84 1.75[8] 4.62	 2.45 2.71 2.92 3.02 3.13 1.90 1.80 4.73	 2.51 2.78 2.99 3.09 3.20 2.32 1.84 4.83	 V V V V V V V V

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 21. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations		1.71	–	–	V
I_{DDP}	Supply Current During Programming or Verify		–	5	25	mA
V_{ILP}	Input Low Voltage During Programming or Verify	See the appropriate DC General Purpose IO Specifications on page 17	–	–	V_{IL}	V
V_{IHP}	Input High Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications on page 17 table on pages 15 or 16	V_{IH}	–	–	V
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	–	–	0.2	mA
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	Driving internal pull down resistor	–	–	1.5	mA
V_{OLP}	Output Low Voltage During Programming or Verify		–	–	Vss + 0.75	V
V_{OHP}	Output High Voltage During Programming or Verify	See appropriate DC General Purpose IO Specifications on page 17 table on page 16. For Vdd > 3V use V_{OH4} in Table 12 on page 16.	V_{OH}	–	Vdd	V
$Flash_{ENPB}$	Flash Write Endurance	Erase/write cycles per block	50,000	–	–	Cycles
$Flash_{DR}$	Flash Data Retention	Following maximum Flash write cycles; ambient temperature of 55°C	10	20	–	Years

Notes

5. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
6. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
7. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
8. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{MAX}	Maximum Operating Frequency		24	–	–	MHz
F_{CPU}	Maximum Processing Frequency		24	–	–	MHz
F_{32K1}	Internal Low Speed Oscillator Frequency		19	32	50	kHz
F_{IMO24}	Internal Main Oscillator Frequency at 24 MHz Setting		22.8	24	25.2	MHz
F_{IMO12}	Internal Main Oscillator Frequency at 12 MHz Setting		11.4	12	12.6	MHz
F_{IMO6}	Internal Main Oscillator Frequency at 6 MHz Setting		5.7	6.0	6.3	MHz
DC_{IMO}	Duty Cycle of IMO		40	50	60	%
T_{RAMP}	Supply Ramp Time		0	–	–	µs
T_{XRST}	External Reset Pulse Width at Power Up	After supply voltage is valid	1			ms
T_{XRST2}	External Reset Pulse Width after Power Up	Applies after part has booted	10			µs

AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO Operating Frequency	Normal Strong Mode Port 0, 1	0 0	– –	6 MHz for 1.71V<Vdd<2.4V 12 MHz for 2.4V<Vdd<5.5V	MHz
TRise23	Rise Time, Strong Mode, Cload = 50 pF Ports 2 or 3	Vdd = 3.0 to 3.6V, 10% – 90%	15	–	80	ns
TRise23L	Rise Time, Strong Mode Low Supply, Cload = 50 pF Ports 2 or 3	Vdd = 1.71 to 3.0V, 10% – 90%	15	–	80	ns
TRise01	Rise Time, Strong Mode, Cload = 50 pF Ports 0 or 1	Vdd = 3.0 to 3.6V, 10% – 90% LDO enabled or disabled	10	–	50	ns
TRise01L	Rise Time, Strong Mode Low Supply, Cload = 50 pF Ports 0 or 1	Vdd = 1.71 to 3.0V, 10% – 90% LDO enabled or disabled	10	–	80	ns
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	Vdd = 3.0 to 3.6V, 10% – 90%	10	–	50	ns
TFallL	Fall Time, Strong Mode Low Supply, Cload = 50 pF All Ports	Vdd = 1.71 to 3.0V, 10% – 90%	10	–	70	ns

Figure 10. GPIO Timing Diagram

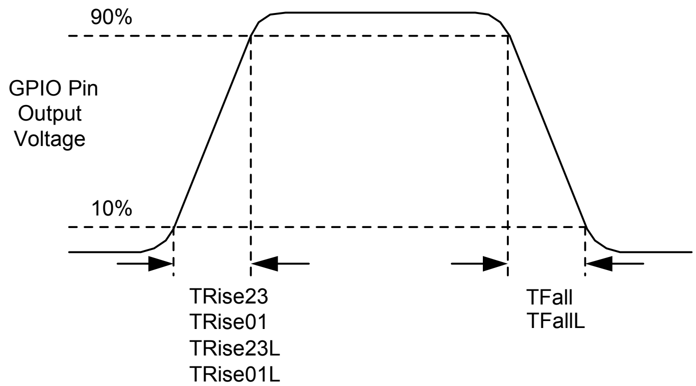


Table 24.AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full speed data rate	Average bit rate	12–0.25%	12	12 + 0.25%	MHz
Tdjr1	Receiver data jitter tolerance	To next transition	-18.5	–	18.5	ns
Tdjr2	Receiver data jitter tolerance	To pair transition	-9	–	9	ns
Tudj1	Driver differential jitter	To next transition	-3.5	–	3.5	ns
Tudj2	Driver differential jitter	To pair transition	-4.0	–	4.0	ns
Tfdeop	Source jitter for differential transition	To SE0 transition	-2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–		ns
Tfst	Width of SE0 interval during differential transition			–	14	ns

Table 25.AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time	50 pF	4	–	20	ns
Tf	Transition fall time	50 pF	4	–	20	ns
TR	Rise/fall time matching		90.00	–	111.1	%
Vcrs	Output signal crossover voltage		1.3	–	2.0	V

AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LPC}	Comparator Response Time, 50 mV Overdrive	50 mV overdrive does not include offset voltage.			100	ns

AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 27. AC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SW}	Switch Rate	Maximum pin voltage when measuring switch rate is 1.8Vp-p	–	–	6.3	MHz

AC External Clock Specifications

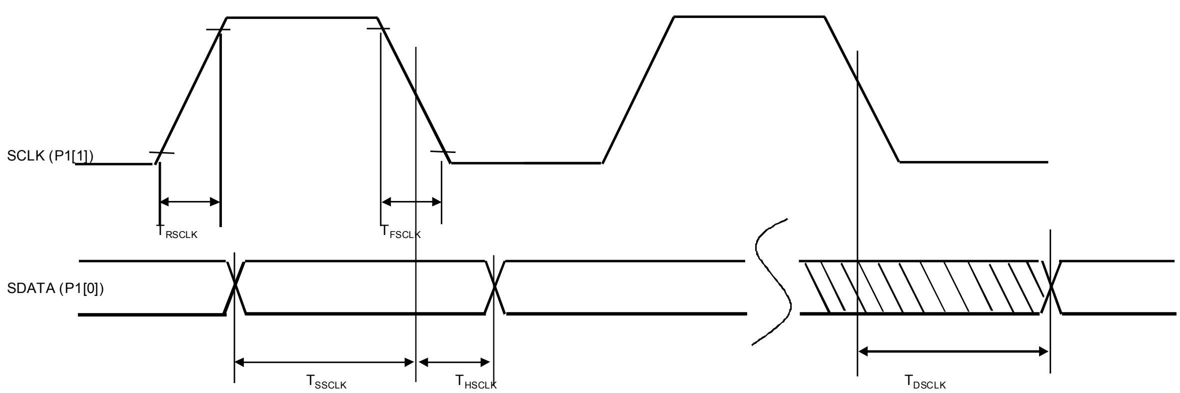
The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 28. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency		0.750	–	25.2	MHz
–	High Period		20.6	–	5300	ns
–	Low Period		20.6	–	–	ns
–	Power Up IMO to Switch		150	–	–	µs

AC Programming Specifications

Figure 11. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{RSCLK}	Rise Time of SCLK		1	–	20	ns
T_{FSCLK}	Fall Time of SCLK		1	–	20	ns
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK		40	–	–	ns
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK		40	–	–	ns
F_{SCLK}	Frequency of SCLK		0	–	8	MHz
T_{ERASEB}	Flash Erase Time (Block)		–	–	18	ms
T_{WRITE}	Flash Block Write Time		–	–	25	ms
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	$3.6 < Vdd$	–	–	60	ns
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	$3.0 \leq Vdd \leq 3.6$	–	–	85	ns
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	$1.71 \leq Vdd \leq 3.0$	–	–	130	ns

AC SPI Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 30. AC SPI Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SPIM}	Maximum Input Clock Frequency Selection, Master 2.4V<Vdd<5.5V	Output clock frequency is half of input clock rate.	–	–	12	MHz
	Maximum Input Clock Frequency Selection, Master(21)1.71V<Vdd<2.4V	Output clock frequency is half of input clock rate			6	MHz
F_{SPIS}	Maximum Input Clock Frequency Selection, Slave 2.4<Vdd<5.5V		–	–	12	MHz
	Maximum Input Clock Frequency Selection, Slave 1.71V<Vdd<2.4V				6	MHz
T_{SS}	Width of SS_ Negated Between Transmissions		50	–	–	ns

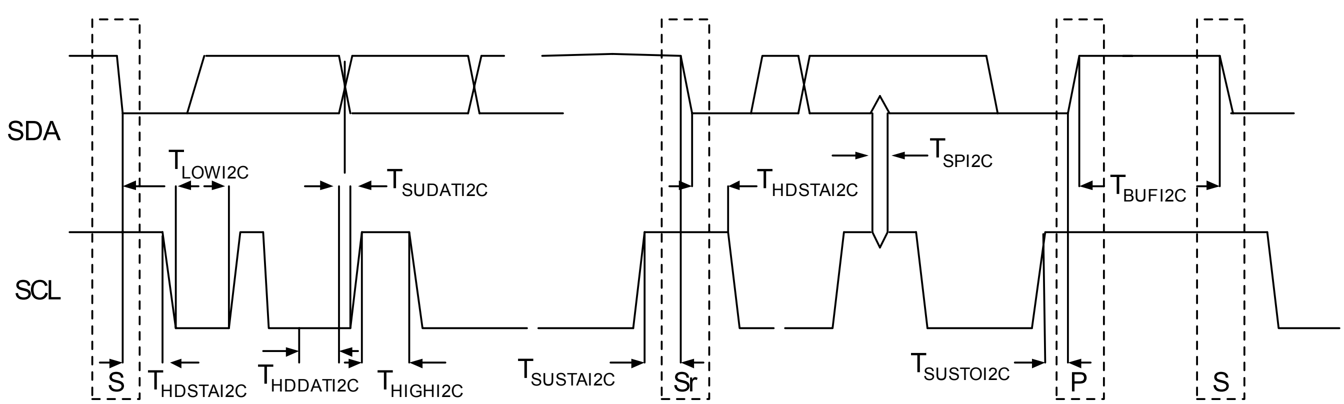
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Conditions	Standard Mode		Fast Mode		Units
			Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency		0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.		4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock		4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock		4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition		4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time		0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time		250	–	100[9]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition		4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition		4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.		–	–	0	50	ns

Figure 12. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

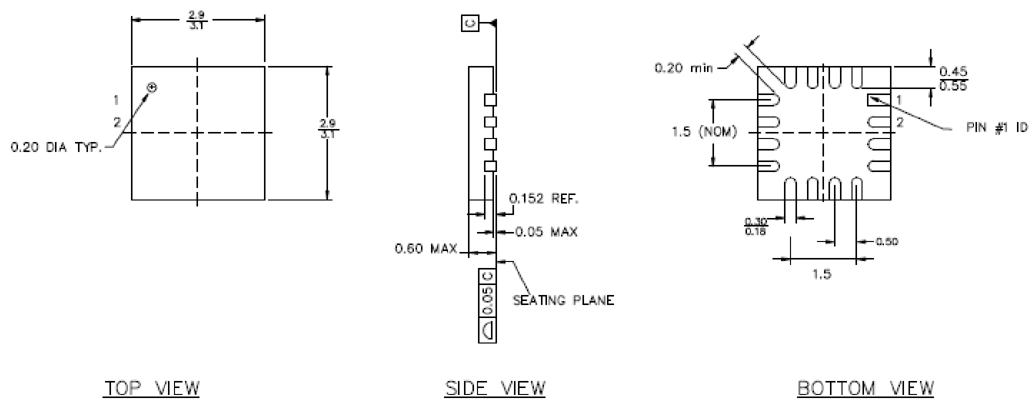
9. A Fast-Mode I2C-bus device can be used in a Standard Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the CY8C20x46/CY8C20x66 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 13. 16-Pin Chip On Lead 3x3 mm (Sawn)

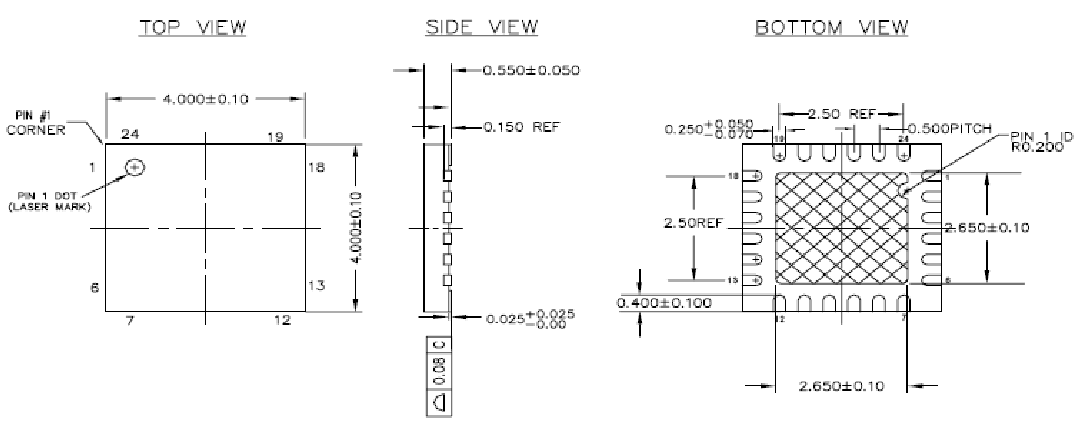


PART NO.	DESCRIPTION
LG16A	LEAD–FREE
LD16A	STANDARD

NOTES:
1. JEDEC # MO–220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN/MAX

001-09116 *D

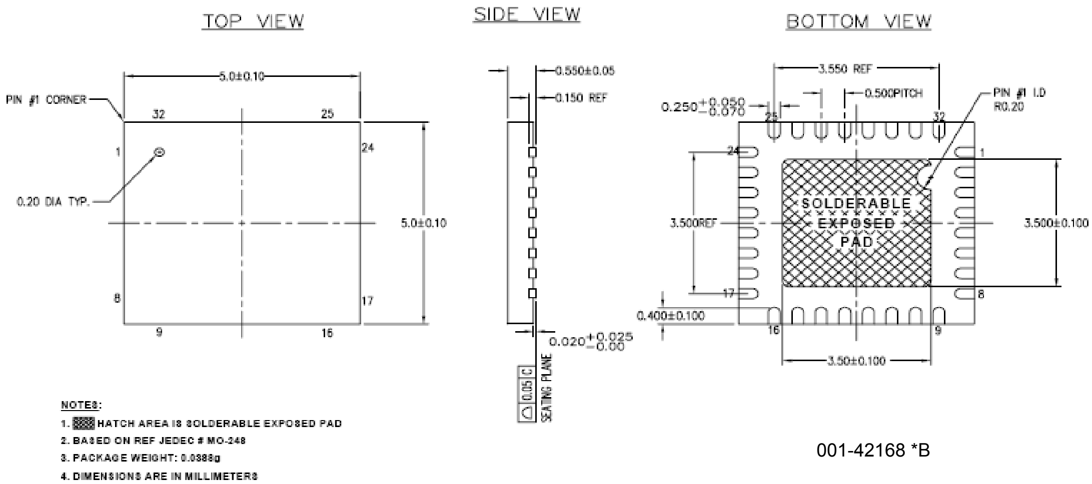
Figure 14. 24-Pin (4x4 x 0.6 mm) QFN



NOTES :
1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. UNIT PACKAGE WEIGHT : 0.024 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

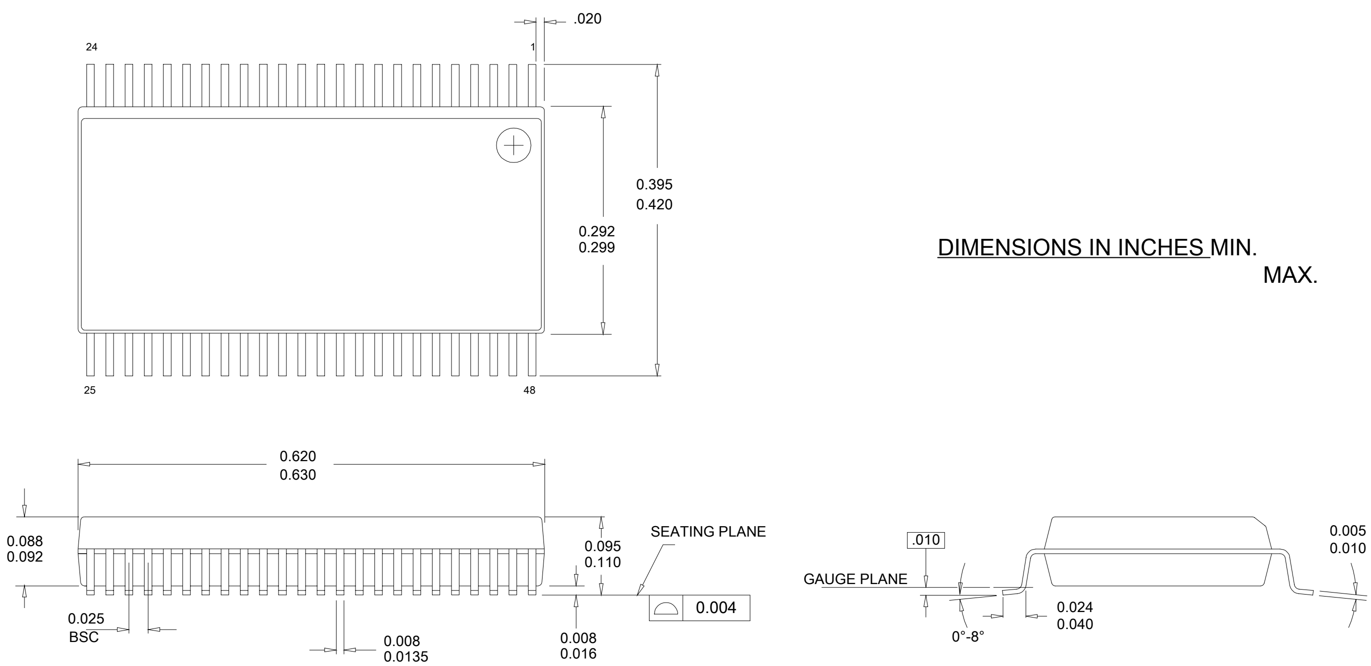
001-13937 *B

Figure 15. 32-Pin (5x5 x 0.6 mm) QFN



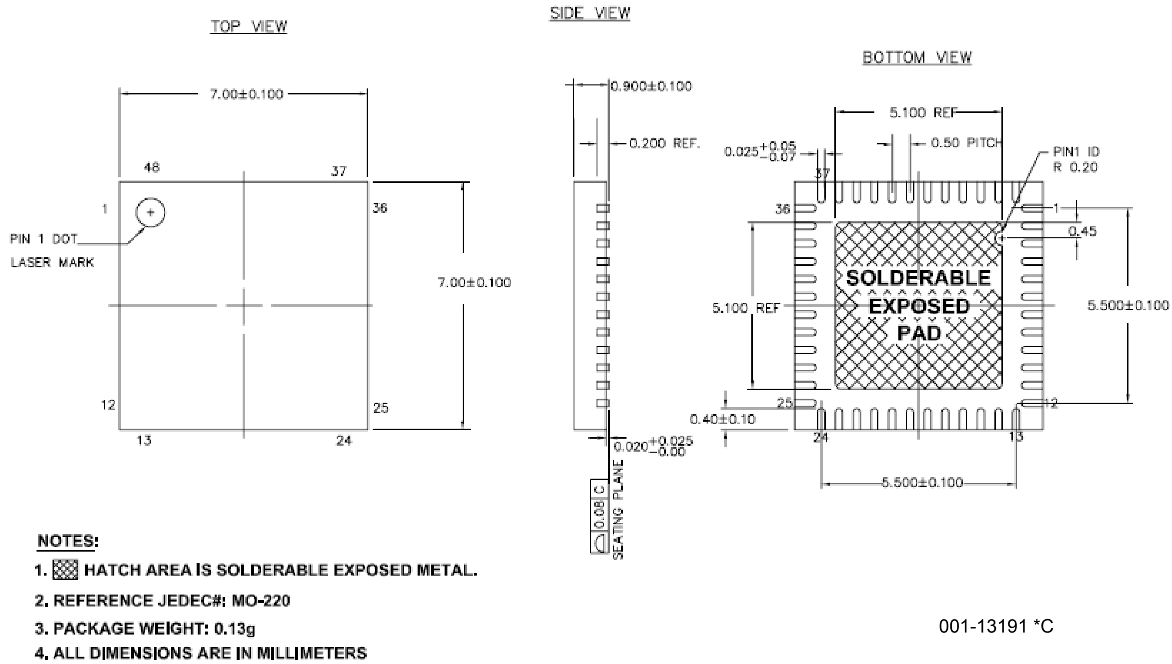
001-42168 *B

Figure 16. 48-Pin (300 MIL) SSOP



51-85061 *C

Figure 17. 48-Pin (7x7 mm) QFN



Important Note

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 32. Thermal Impedances per Package

Package	Typical θ_{JA} [10]
16 QFN	32.69°C/W
24 QFN[11]	20.90°C/W
32 QFN[11]	19.51°C/W
48 SSOP	69°C/W
48 QFN[11]	17.68°C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 33. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[12]	Maximum Peak Temperature
16 QFN	240°C	260°C
24 QFN	240°C	260°C
32 QFN	240°C	260°C
48 SSOP	220°C	260°C
48 QFN	240°C	260°C

Notes

10. $T_J = T_A + \text{Power} \times \theta_{JA}$.
11. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
12. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C20x46/ CY8C20x66 family.

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under Software.

PSoC Express™

As the newest addition to the PSoC development software suite, PSoC Express is the first visual embedded system design tool that allows a user to create an entire PSoC project and generate a schematic, BOM, and data sheet without writing a single line of code. Users work directly with application objects such as LEDs, switches, sensors, and fans. PSoC Express is available free of charge at http://www.cypress.com/psocexpress.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com/shop/ under Product Categories, click PSoC® Mixed Signal Arrays to view a current list of available items.

Development Kits

All development kits can be purchased from the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

CY3210-ExpressDK PSoC Express Development Kit

The CY3210-ExpressDK is for advanced prototyping and development with PSoC Express (may be used with ICE-Cube In-Circuit Emulator). It provides access to I^2C buses, voltage reference, switches, upgradeable modules and more. The kit includes:

- PSoC Express Software CD
- Express Development Board
- 4 Fan Modules
- 2 Proto Modules
- MiniProg In-System Serial Programmer
- MiniEval PCB Evaluation Board
- Jumper Wire Kit
- USB 2.0 Cable
- Serial Cable (DB9)
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- 2 CY8C24423A-24PXI 28-PDIP Chip Samples
- 2 CY8C27443-24PXI 28-PDIP Chip Samples
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 34. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[13]	Foot Kit[14]	Adapter[15]
CY8C20246-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-FK	See note 15
CY8C20266-24LKXI	16 QFN	CY3250-20266QFN	CY3250-16QFN-FK	See note 15
CY8C20346-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 15
CY8C20366-24LQXI	24 QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 15
CY8C20446-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 15
CY8C20466-24LQXI	32 QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 15
CY8C20546-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 15
CY8C20566-24PVXI	48 SSOP	CY3250-20X66	CY3250-48SSOP-FK	See note 15
CY8C20666-24LTXI	48 QFN	CY3250-20666QFN	CY3250-48QFN-FK	See note 15

Third-Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "*Debugging - Build a PSoC Emulator into Your Board - AN2323*" at http://www.cypress.com/AN2323.

Notes

13. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
14. Foot kit includes surface mount feet that can be soldered to the target PCB.
15. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the CY8C20x46 and CY8C20x66 PSoC devices key package features and ordering codes.

Table 35. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital IO Pins	Analog Inputs	XRES Pin	USB
16 Pin (3x3 x 0.6 mm) QFN	CY8C20246-24LKXI	16K	2048	1	13	13[16]	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20246-24LKXIT	16K	2048	1	13	13[16]	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20346-24LQXI	16K	2048	1	20	20[16]	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20346-24LQXIT	16K	2048	1	20	20[16]	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20446-24LQXI	16K	2048	1	28	28[16]	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20446-24LQXIT	16K	2048	1	28	28[16]	Yes	No
48-Pin SSOP	CY8C20546-24PVXI	16K	2048	1	36	36[16]	Yes	Yes
48-Pin SSOP (Tape and Reel)	CY8C20546-24PVXIT	16K	2048	1	36	36[16]	Yes	Yes
16 Pin (3x3 x 0.6 mm) QFN	CY8C20266-24LKXI	32K	2048	1	13	13[16]	Yes	No
16 Pin (3x3 x 0.6 mm) QFN (Tape and Reel)	CY8C20266-24LKXIT	32K	2048	1	13	13[16]	Yes	No
24 Pin (4x4 x 0.6 mm) QFN	CY8C20366-24LQXI	32K	2048	1	20	20[16]	Yes	No
24 Pin (4x4 x 0.6 mm) QFN (Tape and Reel)	CY8C20366-24LQXIT	32K	2048	1	20	20[16]	Yes	No
32 Pin (5x5 x 0.6 mm) QFN	CY8C20466-24LQXI	32K	2048	1	28	28[16]	Yes	No
32 Pin (5x5 x 0.6 mm) QFN (Tape and Reel)	CY8C20466-24LQXIT	32K	2048	1	28	28[16]	Yes	No
48-Pin SSOP	CY8C20566-24PVXI	32K	2048	1	36	36[16]	Yes	Yes
48-Pin SSOP (Tape and Reel)	CY8C20566-24PVXIT	32K	2048	1	36	36[16]	Yes	Yes
48 Pin (7x7 mm) QFN	CY8C20666-24LTXI	32K	2048	1	36	36[16]	Yes	Yes
48 Pin (7x7 mm) QFN (Tape and Reel)	CY8C20666-24LTXIT	32K	2048	1	36	36[16]	Yes	Yes
48 Pin (7x7 mm) QFN (OCD)(4)	CY8C20066-24LTXI	32K	2048	1	36	36[16]	Yes	Yes

Notes
16. Dual-function Digital IO Pins also connect to the common analog mux.

Document History Page

Revision	ECN	Origin of Change	Submission Date	Description of Change
Document Title: CY8C20x46 CY8C20x66 CapSense™ Applications Document Number: 001-12696				
**	766857	HMT	See ECN	New silicon and document (Revision **).
*A	1242866	HMT	See ECN	Add features. Update all applicable sections. Update specs. Fix 24-pin QFN pinout moving pins inside. Update package revisions. Update and add to Emulation and Programming Accessories table.
*B	2174006	AESA	See ECN	Added 48-Pin SSOP Part Pinout Modified symbol R_{VDD} to R_{GND} in Table DC Analog Mux Bus Specification Added footnote in Table DC Analog Mux Bus Specification Added 16K FLASH Parts. Updated Notes, Package Diagrams and Ordering Information table. Updated Thermal Impedance and Solder Reflow tables
*C	2587518	TOF/JASM/MNU/ HMT	10/13/08	Converted from Preliminary to Final Fixed broken links. Updated data sheet template. Added operating voltage ranges with USB ADC resolution changed from 10-bit to 8-bit Included ADC specifications table Included Comparator specification table Included Voh7, Voh8, Voh9, Voh10 specs Flash data retention – condition added to Note Input leakage spec changed to 1 μA max GPIO rise time for ports 0,1 and ports 2,3 made common AC Programming specifications updated Included AC Programming cycle timing diagram AC SPI specification updated The VIH for 3.0<Vdd<2.4 changed to 1.6 from 2.0 Added USB specification Added SPI CLK to P1[0] Updated package diagrams Updated thermal impedances for QFN packages Updated F_{GPIO} parameter in Table 23 Updated voltage ranges for F_{SPIM} and F_{SPIS} in Table 30 Update Development Tools, add Designing with PSoC Designer. Edit, fix links, notes and table format. Update R_{IN} formula, fix TRise parameter names in GPIO figure, fix Switch Rate note. Update maximum data in Table 20. DC POR and LVD Specifications.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

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