# MOTOROLA

D-Type Flip-Flop With Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/32504

The 54LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

- 8-Bit High-Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip-Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diode Limits High-Speed Termination Effects

MPO
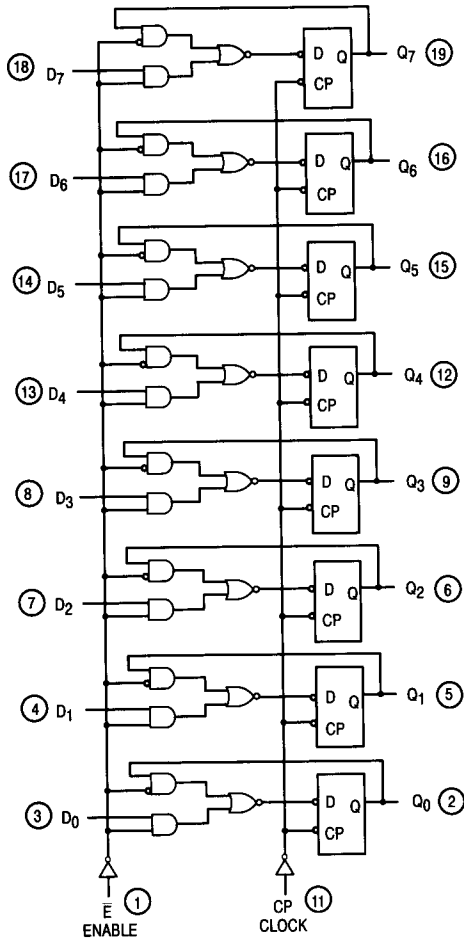
AVAILABLE AS:

1) JAN: JM38510/32504BXA
2) SMD: N/A
3) 883: 54LS377/BXAJC

X = CASE OUTLINE AS FOLLOWS:
  PACKAGE: CERDIP: R
         CERFLAT: S
           LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

LOGIC DIAGRAM

	PIN ASSIGNMENTS			
FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}$	1	1	1	GND
Q_0	2	2	2	V_{CC}
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
Q_1	5	5	5	V_{CC}
Q_2	6	6	6	V_{CC}
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
Q_3	9	9	9	V_{CC}
GND	10	10	10	GND
CP	11	11	11	CP1
Q_4	12	12	12	V_{CC}
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
Q_5	15	15	15	V_{CC}
Q_6	16	16	16	V_{CC}
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
Q_7	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE				
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⤒	X	No Change	No Change
L	⤒	H	H	L
L	⤒	L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

5

CONNECTION DIAGRAM

Pin		Pin
$\overline{E}$	1	20 V_{CC}
Q_0	2	19 Q_7
D_0	3	18 D_7
D_1	4	17 D_6
Q_1	5	16 Q_6
Q_2	6	15 Q_5
D_2	7	14 D_5
D_3	8	13 D_4
Q_3	9	12 Q_4
GND	10	11 CP
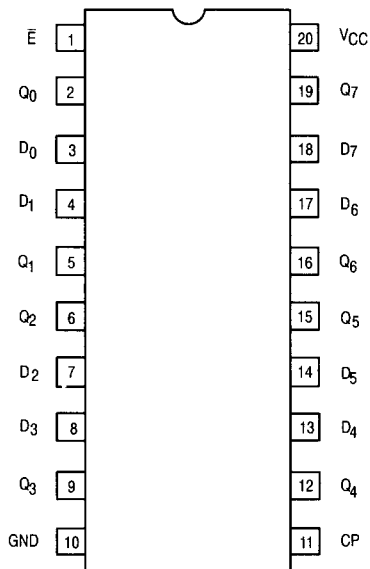
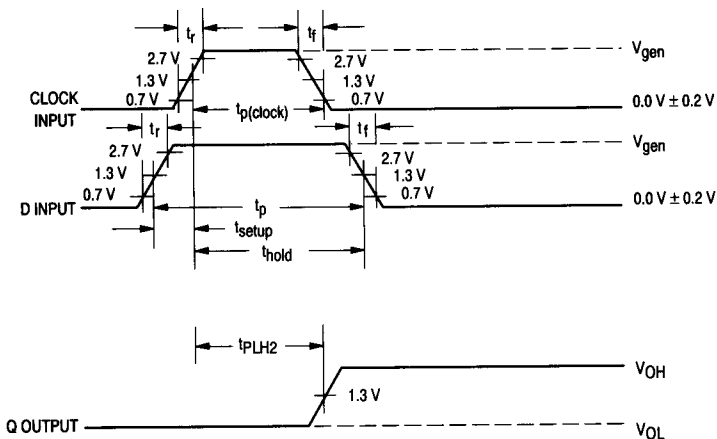| Pin Names		Loading (Note a)	
		HIGH	LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
Q_0-Q_3	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

5

AC TEST CIRCUIT

$V_{CC} = 5.0$ V

R_L (SEE NOTE 5)

C_L (SEE NOTE 4)

SEE NOTE 2   SEE NOTE 1

CLEAR INPUT

CLEAR INPUT

D
CLEAR
GND
Q

CLOCK
V_{CC}

TEST OUTPUT

HIGH-LEVEL SWITCHING WAVEFORMS

CLOCK INPUT

t_r t_f
2.7 V   2.7 V
1.3 V   1.3 V
0.7 V $t_{p(clock)}$ 0.7 V V_{gen}
0.0 V ± 0.2 V

D INPUT

t_r t_f
2.7 V   2.7 V
1.3 V   1.3 V
0.7 V t_p 0.7 V V_{gen}
0.0 V ± 0.2 V

t_{setup}
t_{hold}

Q OUTPUT

t_{PLH2}
1.3 V

V_{OH}
V_{OL}

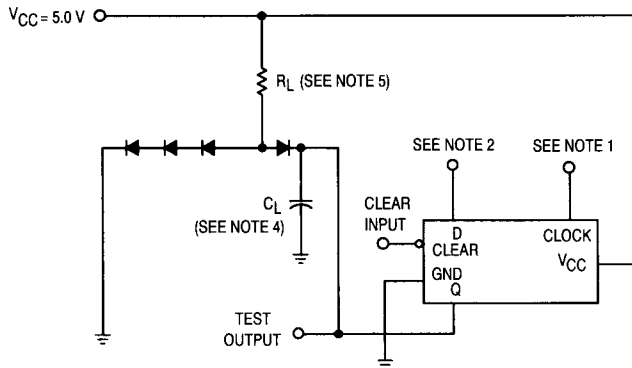**NOTES:**
1. Clock input pulse has the following characteristics:
   $V_{gen} = 3.0$ V ± 0.2 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{p(clock)} = 30$ ns, and PRR ≤ 1.0 MHz.
2. D input has the following characteristics:
   $V_{gen} = 3.0$ V ± 0.2 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{setup} = 20$ ns, $t_{hold} = 5.0$ ns, $t_p = 25$ ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50$ pF ± 10% (including jig and probe capacitance).
5. $R_L = 2.0$ kΩ ± 5.0%.

AC TEST CIRCUIT

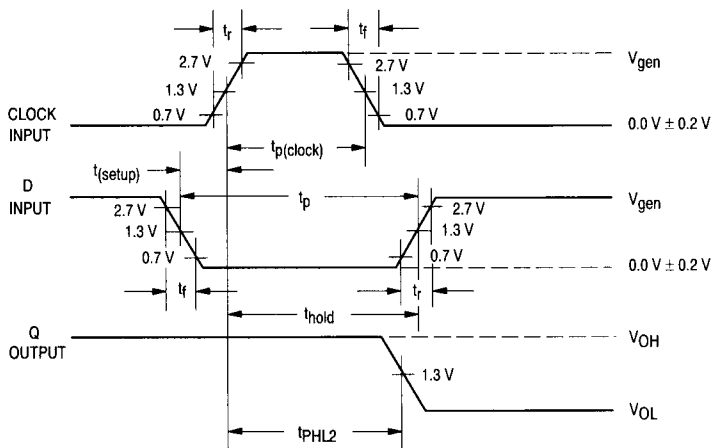## LOW-LEVEL SWITCHING WAVEFORMS

NOTES:
1. Clock input pulse has the following characteristics:
   $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_p(\text{clock}) = 30 \text{ ns}$, and PRR ≤ 1.0 MHz. When testing f_{MAX}, PRR = see table, and $t_0 = t_1 \leq 6.0 \text{ ns}$.
2. D input has the following characteristics:
   $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$, $t_{setup} = 20 \text{ ns}$, $t_{hold} = 5.0 \text{ ns}$, $t_p = 25 \text{ ns}$, and PRR is 50% of the clock PRR. For f_{MAX}, $t_0 = t_1 \leq 6.0 \text{ ns}$.
3. All diodes are 1N3064, or equivalent.
4. $C_L = 50 \text{ pF} \pm 10\%$ (including jig and probe capacitance).
5. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.

54LS377

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	$V_{CC} = 4.5$ V, $I_{OH} = -0.4$ mA, $V_{IH} = 2.0$ V, $\overline{E} = 0.7$ V, other inputs are open, CLK = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	$V_{CC} = 4.5$ V, $I_{OL} = 4.0$ mA, $V_{IL} = 0.7$ V, $\overline{E} = 0.7$ V, other inputs are open, CLK = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.5					V	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	$V_{CC} = 5.5$ V, $V_{IH} = 2.7$ V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	$V_{CC} = 5.5$ V, $V_{IHH} = 5.5$ V, other inputs are open.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	$V_{CC} = 5.5$ V, $V_{IN} = 4.5$ V, $\overline{E} = 0.7$ V, CLK = (See Note 2), $V_{OUT} = $ GND.
I_{IL1}	Logical "0" Input Current	−105	−345	−105	−345	−105	−345	μA	$V_{CC} = 5.5$ V, $V_{IL} = 0.4$ V ($\overline{E}$), other inputs are open.
I_{IL2}	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	μA	$V_{CC} = 5.5$ V, $V_{IL} = 0.4$ V, other inputs are open.
I_{CC}	Power Supply Current Off		32		32		32	mA	$V_{CC} = 5.5$ V, $V_{IN} = $ GND (all inputs), CLK = (See Note 2).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	$V_{CC} = 4.5$ V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	$V_{CC} = 4.5$ V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with $V_{CC} = 5.0$ V, $V_{INL} = 0.4$ V, and $V_{INH} = 2.5$ V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output High-Low	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Low-High	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.
f_{MAX}	Maximum Clock Frequency	30 30		25		25		MHz	$V_{CC} = 5.0$ V, $C_L = 50$ pF, $R_L = 2.0$ kΩ. $V_{CC} = 5.0$ V, $C_L = 15$ pF.

NOTES:

1. ‾‾ 2.5 V minimum/5.5 V maximum / 0.0 V

2. ‾‾ 2.5 V minimum/5.5 V maximum / 0.0 V

5