FAIRCHILD SEMICONDUCTOR®

November 2009

FAN7081_GF085
High Side Gate Driver

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation up fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- dV/dt immune.
- Gate drive supply range from 10V to 20V
- Under-voltage lockout
- CMOS Schmit-triggered inputs with pull-up
- High side output out of phase with input (Inverted input)

Typical Applications

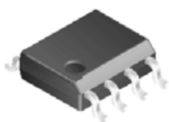
- Diesel and gasoline Injectors/Valves
- MOSFET-and IGBT high side driver applications

For Fairchild's definition of "green" Eco Status, please visit:
http://www.fairchildsemi.com/company/green/rohs_green.html

Description

The FAN7081_GF085 is a high-side gate drive IC designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to VS=-5V (typical) at VBS=15V. Logic input is compatible with standard CMOS outputs. The UVLO circuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 500mA respectively, which is suitable for magnetic- and piezo type injectors and general MOSFET/IGBT based high side driver applications.

SOIC-8

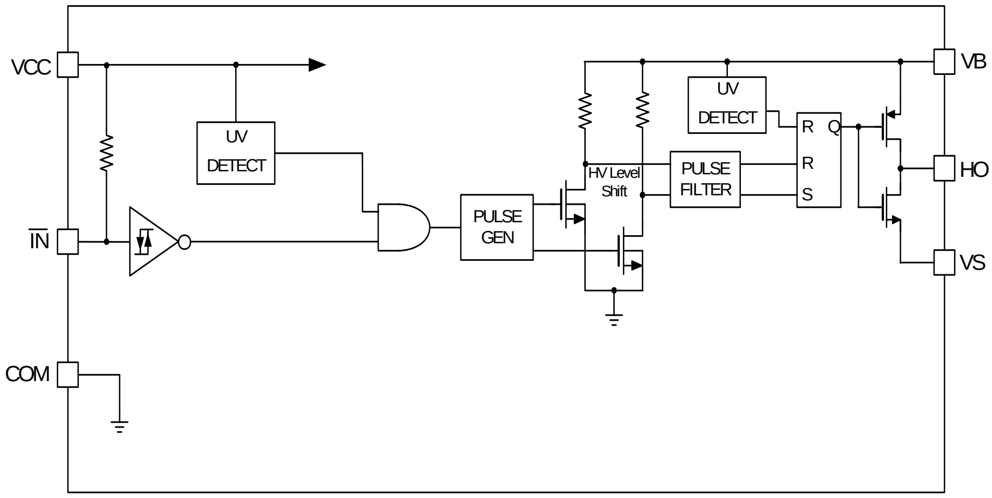


Ordering Information

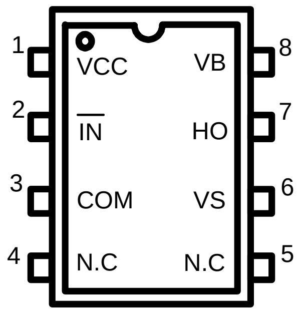
Device	Package	Operating Temp.
FAN7081M	SOIC-8	-40 °C ~ 125 °C
FAN7081MX	SOIC-8	-40 °C ~ 125 °C

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

Pine Number	Pin Name	I/O	Pin Function Description
1	VCC	P	Driver supply voltage
2	$\overline{\text{IN}}$	I	Logic input for high side gate drive output, out of phase with HO
3	COM	P	Ground
4	NC	-	NC
5	NC	-	NC
6	VS	P	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	VB	P	Driver output stage supply

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Parameter	Symbol	Min.	Max.	Unit
High side floating supply offset voltage	VS	VB-25	VB+0.3	V
High side floating supply voltage	VB	-0.3	625	V
High side floating output voltage	VHO	Vs-0.3	VB+0.3	V
Supply voltage	VCC	-0.3	25	V
Input voltage for $\overline{IN}$	VIN	-0.3	Vcc+0.3	V
Power Dissipation 1)	Pd		0.625	W
Thermal resistance, junction to ambient 1)	Rthja		200	°C/W
Electrostatic discharge voltage (Human Body Model)	V_{ESD}	1K		V
Charge device model	V_{CDM}	500		V
Junction Temperature	Tj		150	°C
Storage Temperature	T_S	-55	150	°C

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural codition(StillAir)

JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operations the device should be used within the recommended conditions. -40°C <= Ta <= 125°C

Parameter	Symbol	Min.	Max.	Unit
High side floating supply voltage(DC) Transient:-10V@ 0.2 us	VB	VS + 10	VS + 20	V
High side floating supply offset voltage(DC)	VS	-4 (@VBS >= 10V) -5 (@VBS >= 11.5V)	600	V
High side floating supply offset voltage(Transient)	VS	-25 (~200ns) -20(200ns ~240ns) -7(240ns~400ns)	600	V
High side floating output voltage	VHO	VS	VB	V
Allowable offset voltage Slew Rate 1)	dv/dt	-	50	V/ns
Supply voltage	VCC	10	20	V
Input voltage for $\overline{IN}$	VIN	0	Vcc	V
Switching Frequency 2)	Fs		200	KHz
Ambient Temperature	Ta	-40	125	°C

Note: 1) Guaranteed by design.

2) Duty = 0.5

Statics Electrical Characteristics

Unless otherwise specified, -40°C <= Ta <= 125°C,VCC = 15V, VBS = 15V, VS = 0V, RL = 50Ω, CL = 2.5nF.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Vcc and VBS supply Characteristics						
VCC and VBS supply under voltage positive going threshold	VCCUV+ VBSUV+		-	8.7	9.8	V
VCC and VBS supply under voltage negative going threshold	VCCUV- VBSUV-		7.4	8.2	-	V
VCC and VBS supply under voltage hysteresis	VCCUVH VBSUVH	-	0.2	0.5	-	V
Under voltage lockout response time	tduvcc tduvbs	VCC: 10V-->7.3V or 7.3V-->10V VBS: 10V-->7.3V or 7.3V-->10V	0.5 0.5		20 20	us us
Offset supply leakage current	ILK	VB=VS=600V	-	-	50	uA
Quiescent VBS supply current	IQBS	VIN=0	-	23	250	uA
Quiescent Vcc supply current	IQCC1	VIN= 0V	-	42	120	uA
Quiescent Vcc supply current	IQCC2	VIN=15V	-	25	100	uA
Input Characteristics						
High logic level input voltage	VIH		0.63VCC	-	-	V
Low logic level input voltage	VIL		-	-	0.4VCC	V
Low logic level input bias current for IN	IIN+	VIN=0	-	15	50	uA
High logic level input bias current for IN	IIN-	VIN=15V	-	0	1	uA
Output characteristics						
High level output voltage, VBIAS-VO	VOH	IO=0	-	-	0.1	V
Low level output voltage, VO	VOL	IO=0	-	-	0.1	V
Peak output source current	IO1+		250	-	-	mA
Peak output sink current	IO1-		500	-	-	mA
Equivalent output resistance	ROP			40	60	Ω
	RON			20	30	Ω

Note: The input parameter are referenced to COM. The VO and IO parameters are referenced to COM.

Dynamic Electrical Characteristics

Unless otherwise specified, -40°C <= Ta <= 125°C, VCC = 15V, VBS = 15V, VS = 0V, RL = 50Ω, CL = 2.5nF.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input-to-output turn-on propagation delay	t_{plh}	50% input level to 10% output level, V_S = 0V		130	300	ns
Input-to-output turn-off propagation delay	t_{phl}	50% input level to 90% output level V_S = 0V	-	140	300	ns
Output rising time	tr1	10% to 90%, Tj=25°C,V_{BS}=15V	-	15	400	ns
	tr2	10% to 90%		-	500	ns
Output falling time	tf1	90% to 10%, Tj=25°C,V_{BS}=15V	-	10	150	ns
	tf2	90% to 10%		-	500	ns

Application Information

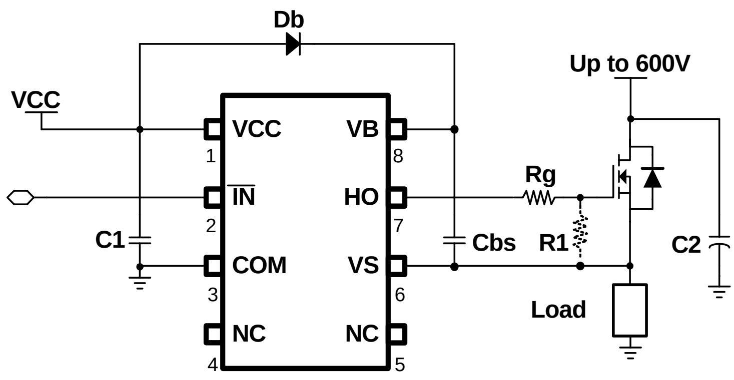
1. Relationship in input/output and supplies

Table.1 Truth table for Vcc, VBS,VIN, and VHO

VCC	VBS	$\overline{IN}$	HO
< VCCUVLO-	X	X	OFF
X	< VBSUVLO-	X	OFF
X	X	HIGH	OFF
> VCCUVLO+	> VBSUVLO+	LOW	ON

Notes:
X means independent from signal

Typical Application Circuit



Typical Waveforms

1. Input/Output Timing

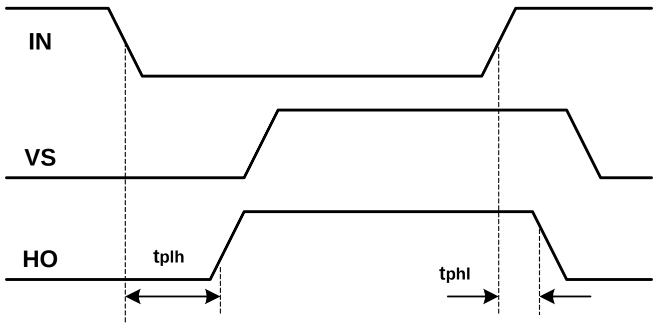


Figure 1. Input /output Timing Diagram

2. Ouput(HO) Switching Timing

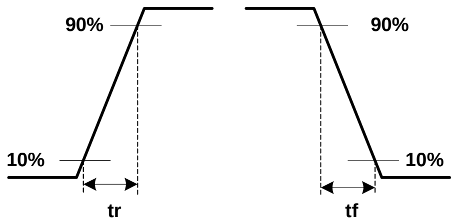


Figure 2. Switching Time Waveform Definitions

3.VB Drop Voltage Diagram

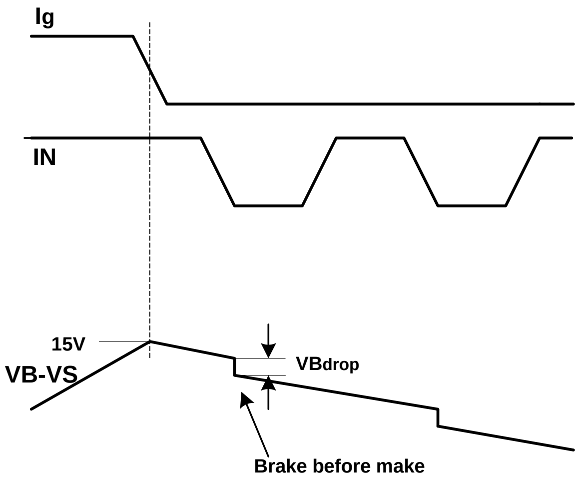


Figure 3a. VB Drop Voltage Diagram

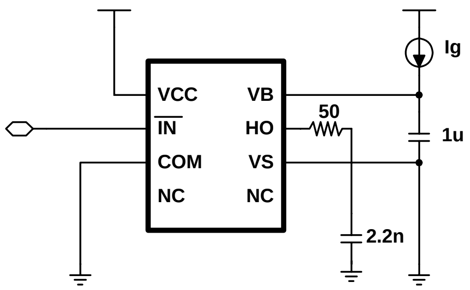


Figure3b. VB Drop Voltage Test Circuit

Performance Graphs

This performance graphs based on ambient temperature -40°C ~125°C

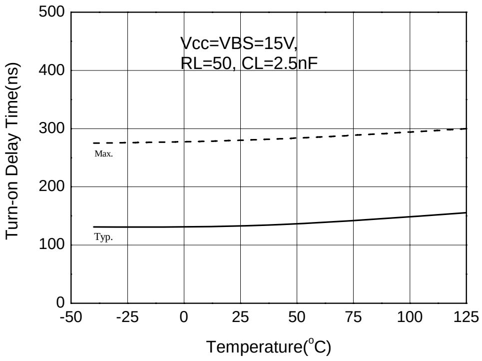


Figure 4a. Turn-On Delay Time vs Temperature

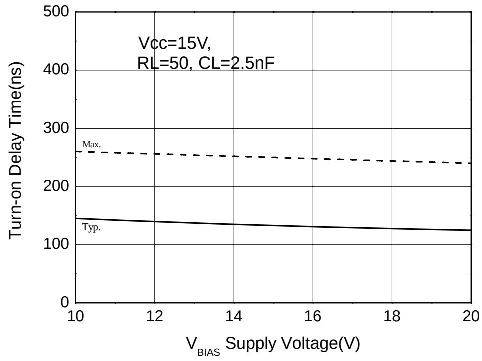


Figure 4b. Turn-On Delay Time vs VBS Supply Voltage

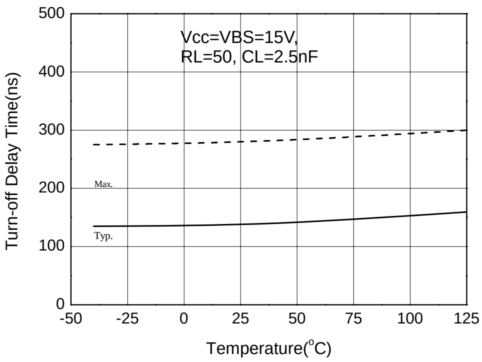


Figure 5a. Turn-Off Delay Time vs Temperature

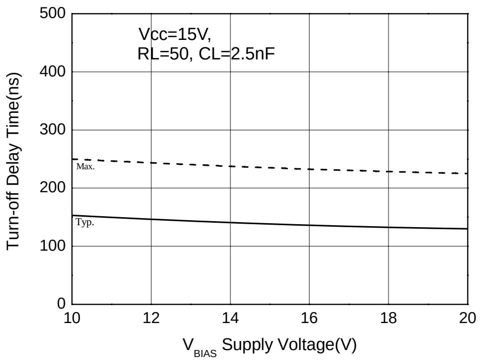


Figure5b. Turn-Off Delay Time vs VBS Supply Voltage

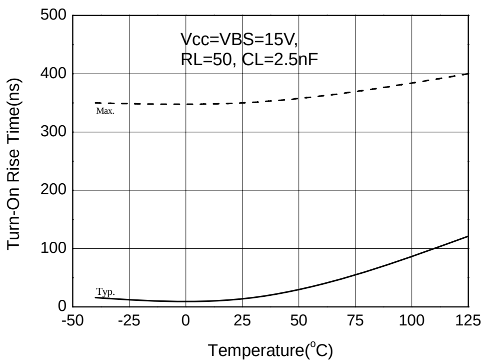


Figure 6a.Turn-On Rising Time vs Temperature

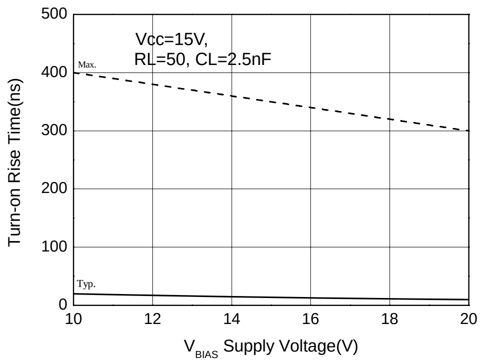


Figure 6b. Turn-ON Rising Time vs VBS Supply Voltage

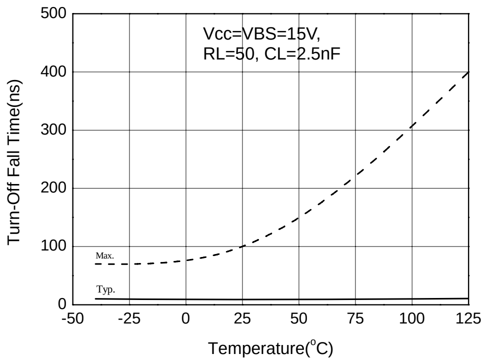


Figure 7a. Turn-Off Falling Time vs Temperature

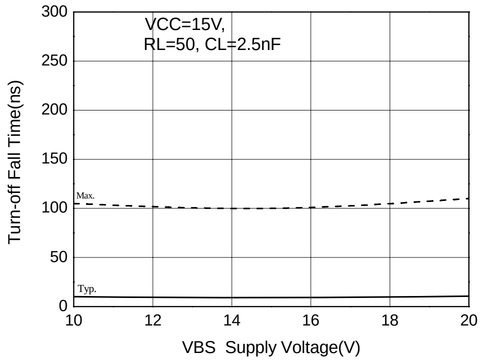


Figure 7b. Turn-Off Falling Time vs VBS Supply Voltage

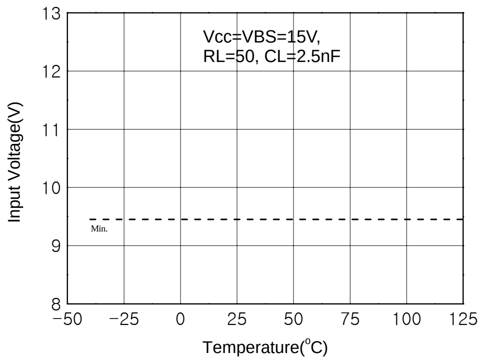


Figure 8a. Logic “1” IN Voltage vs Temperature

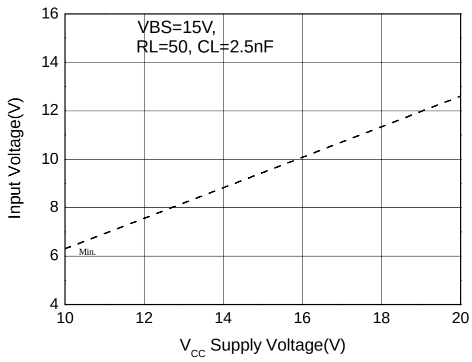


Figure8b. Logic “1” IN Voltage vs VCC Supply Voltage

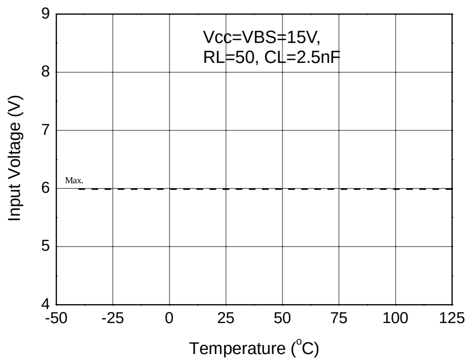


Figure 9a. Logic “0” IN Voltage vs Temperature

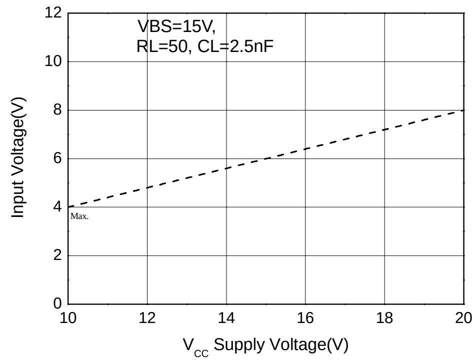


Figure 9b. Logic “0” IN Voltage vs VCC Supply Voltage

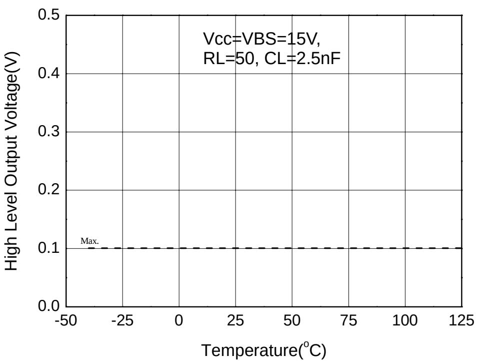


Figure 10a. High Level Output vs Temperature

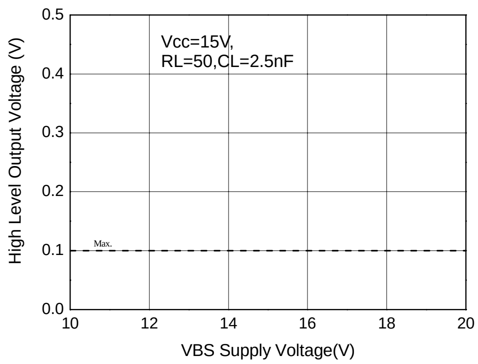


Figure 10b. High Level Output vs VBS Supply Voltage

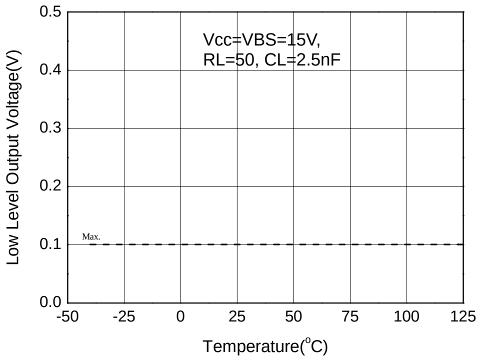


Figure 11a. Low Level Output vs Temperature

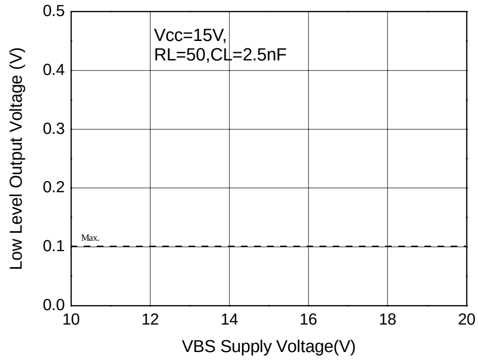


Figure 11b. Low Level Output vs VBS Supply Voltage

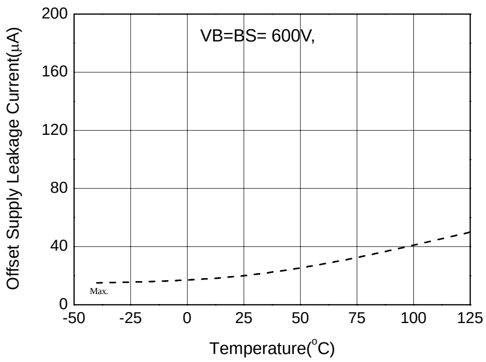


Figure 12a. Offset Supply Leakage Current vs Temperature

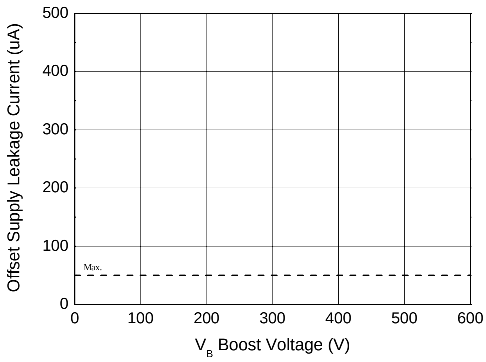


Figure 12b. Offset Supply Leakage Current vs VB Boost Voltage

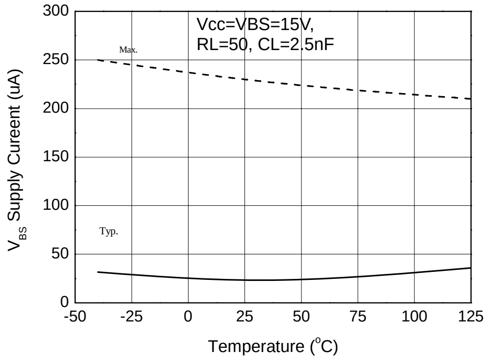


Figure 13a. VBS Supply Current vs Temperature

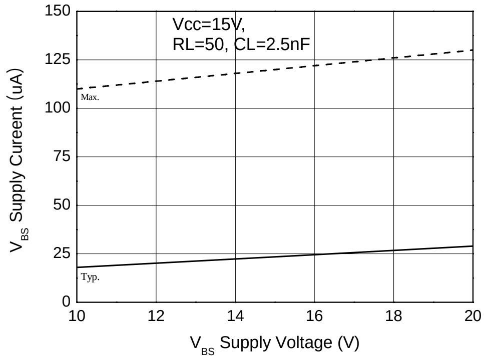


Figure 13b. VBS Supply Current vs VBS Supply Voltage

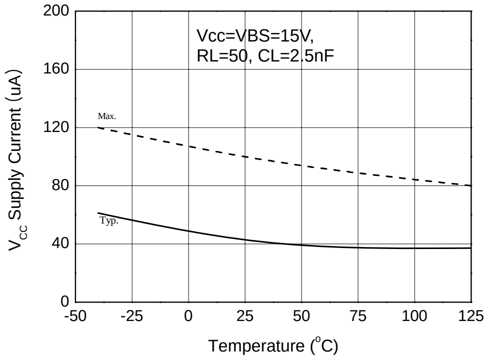


Figure 14a.VCC Supply Current vs Temperature

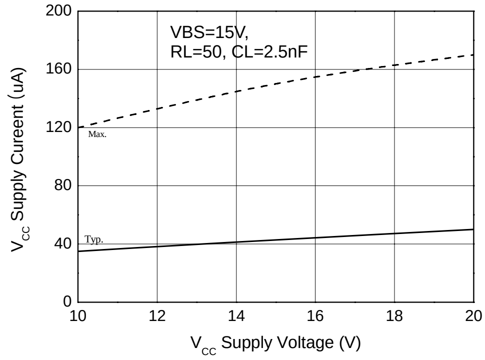


Figure 14b. VCC Supply Current vs VCC Supply Voltage

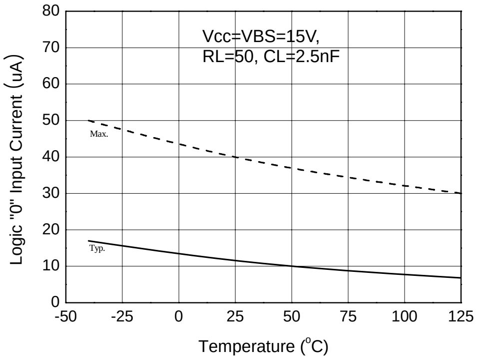


Figure 15a. Logic “0” IN Current vs Temperature

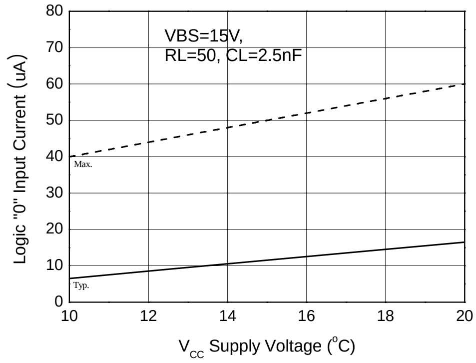


Figure 15b. Logic “0” IN Current vs VCC Supply Voltage

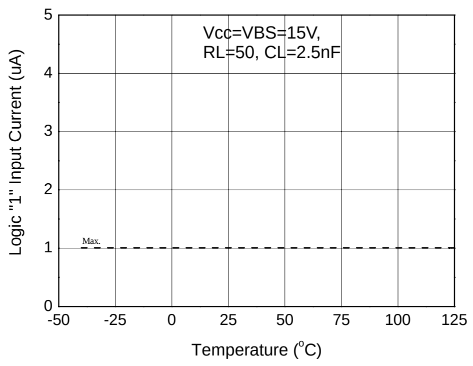


Figure 16a. Logic “1” IN Current vs Temperature

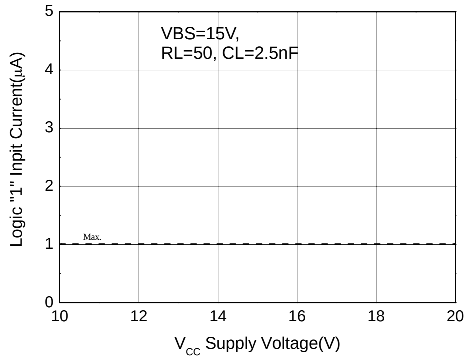


Figure 16b. Logic “1” IN Current vs VCC Supply Voltage

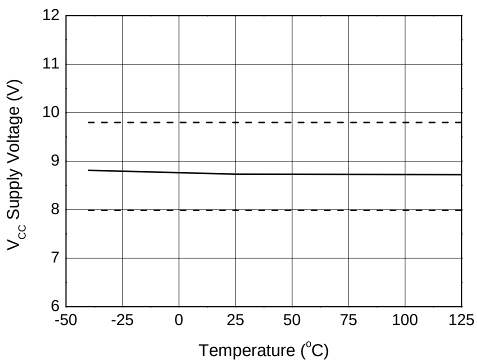


Figure 17a. VCC Under voltage Threshold(+) vs Temperature

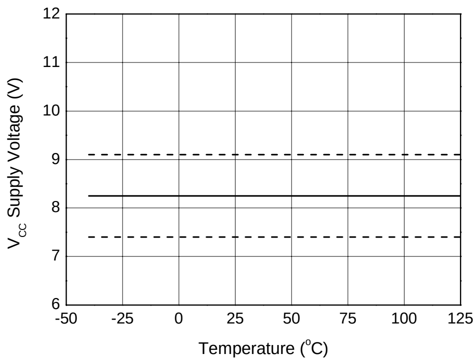


Figure 17b. VCC Under voltage Threshold(-) vs Temperature

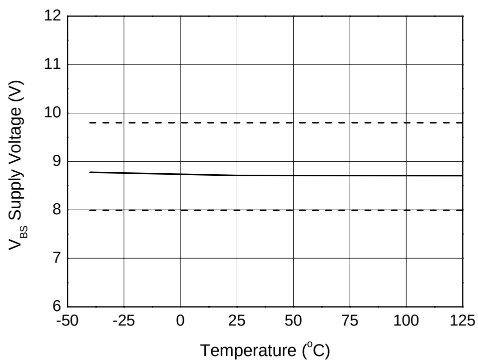


Figure 18a. VBS Under voltage Threshold(+) vs Temperature

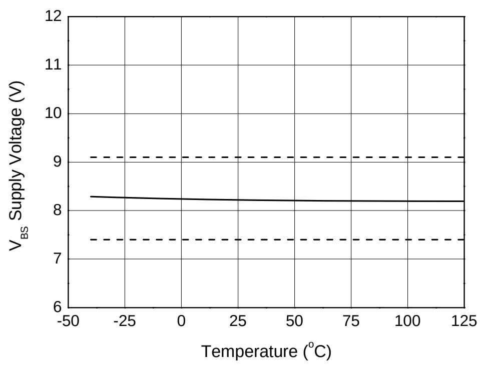


Figure 18b. VBS Under voltage Threshold(-) vs Temperature

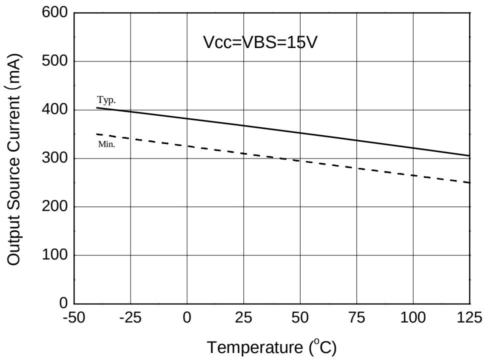


Figure 19a. Output Source Current vs Temperature

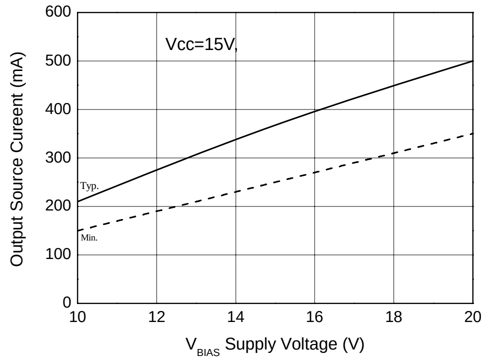


Figure 19b. Output Source Current vs VBS Supply Voltage

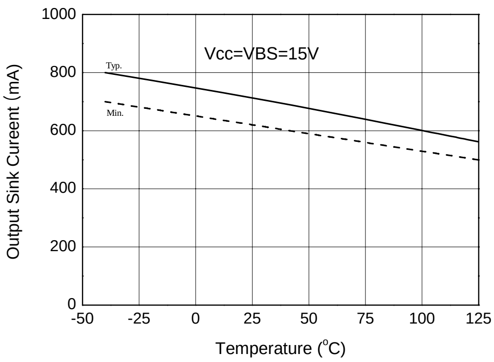


Figure 20a. Output Sink Current vs Temperature

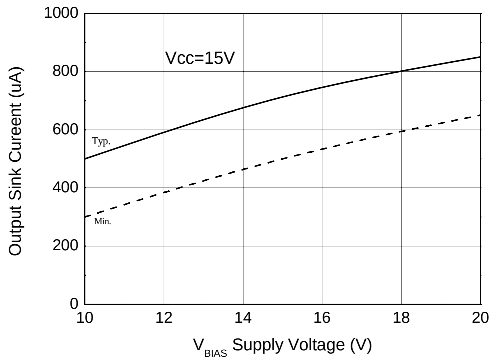


Figure 20b. Output Sink Current vs VBS Supply Voltage

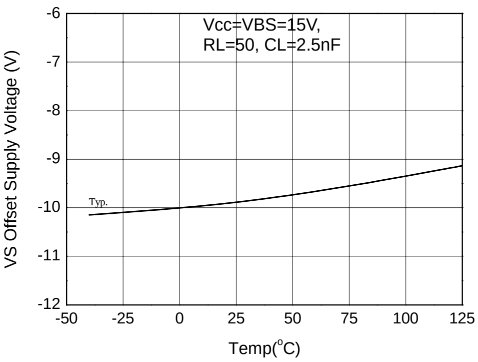


Figure 21a. Maximum VS Negative Voltage vs Temperature

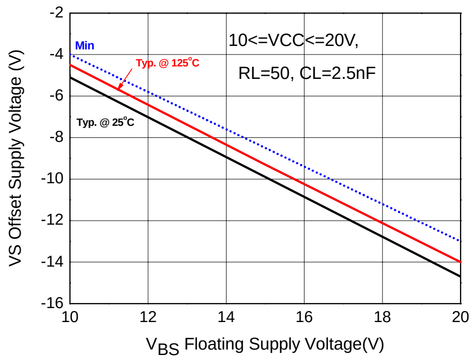
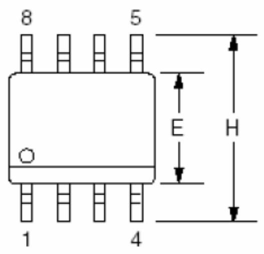


Figure 21b. Maximum VS Negative Voltage vs VBS Supply Voltage

Package Dimensions

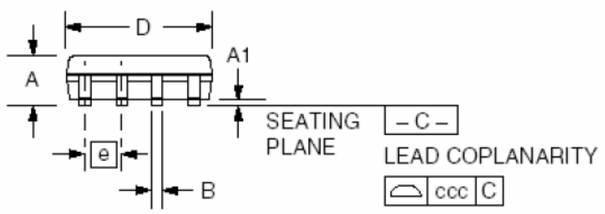
8-SOP

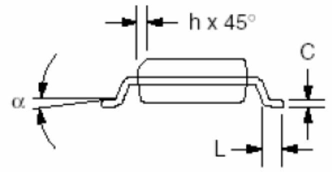
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.0075	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	



Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





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