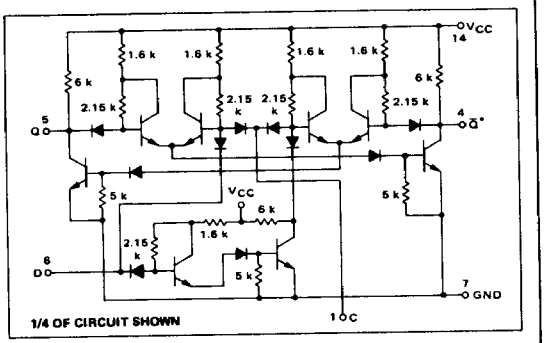
QUAD LATCH

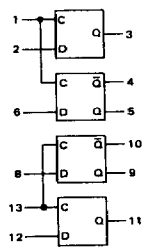
MC1914F · MC1814F,P

The MDTL Quad Latch may be used in any application requiring temporary bit storage. An enable line is included so that only the desired information will be "clocked in." Each enable line operates two latches. When the enable line is high the Q output is forced to follow the D input. Once the enable line returns to a low level the information present on the outputs is fixed and independent of any future change on the D input.

For those applications requiring $\overline{Q}$ outputs, the MC1813P 16 pin dual-in-line plastic package is also available.



1/4 OF CIRCUIT SHOWN



Input Loading Factor = 2
Output Loading Factor = 8
Total Power Dissipation = 220 mW typ/pkg
Propagation Delay Time = 35 ns typ

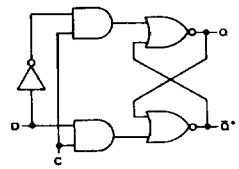
TRUTH TABLE

t_n	t_{n+1}	
D	Q	Q*
1	1	0
0	0	1

*As Applicable (See Loading Diagram)

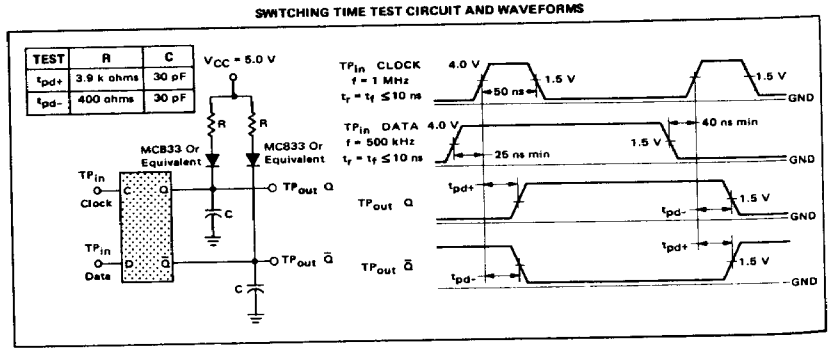
Information present at the data input D is transferred to the Q output when the clock is high, and the Q output will follow the state of the data input as long as the clock remains high. Information present at the outputs will be retained as the clock goes low until such time as the clock is permitted to go high.

LOGIC DIAGRAM



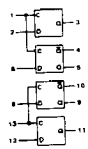
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST	R	C
t_{pd+}	3.9 k ohms	30 pF
t_{pd-}	400 ohms	30 pF



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only 1/2 the quad latch. The other half is tested in the same manner.



@ Test Temperature		TEST CURRENT / VOLTAGE VALUES										
		mA		Volts								
		I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}
MC1914	−55°C	11.4	-0.12	1.40	2.10	0	4.00	-	-	4.50	5.50	-
	+25°C	12.0	-0.12	1.10	2.00	0	4.00	4.50	5.00	4.50	5.50	8.00
	+125°C	10.8	-0.12	0.80	2.00	0	4.00	-	-	4.50	5.50	-
MC1814	0°C	12.0	-0.12	1.20	2.00	0.45	4.00	-	-	5.00	5.00	-
	+25°C	12.0	-0.12	1.10	1.90	0.45	4.00	5.00	5.00	5.00	5.00	8.00
	+75°C	11.4	-0.12	0.95	1.80	0.50	4.00	-	-	5.00	5.00	-

Characteristic	Symbol	Pin Under Test	MC1914 Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit	MC1814 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_{max}	Gnd
Output Voltage	V_{OL}	3	-	0.40	-	0.40	-	0.45	Vdc	-	0.45	-	0.45	-	0.50	Vdc	3	-	2	1	-	-	-	-	14	-	-	7
		4	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		4	-	-	1.6	-	-	-	-		-	-	
		5	-	0.40	-	0.40	-	0.45		-	0.45	-	0.45	-	0.50		5	-	6	1	-	-	-	-		-	-	
	V_{OH}	3	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	3	-	1.2	-	-	-	-		-	-	
		4	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	4	6	1	-	-	-	-		-	-	
		5	2.50	-	2.60	-	2.50	-		2.60	-	2.60	-	2.50	-		-	5	-	1.6	-	-	-	-		-	-	
Short-Circuit Current	I_{SC}	3	-	-2.75	-	-2.75	-	-2.65	mAdc	-	-2.95	-	-2.95	-	-2.80	mAdc	-	-	-	-	-	-	-	-	14	-	-	3,7
		4	-	-2.75	-	-2.75	-	-2.65	mAdc	-	-2.95	-	-2.95	-	-2.80	mAdc	-	-	-	-	-	-	-	-	14	-	-	1,4,5,7
		5	-	-2.75	-	-2.75	-	-2.65	mAdc	-	-2.95	-	-2.95	-	-2.80	mAdc	-	-	-	-	-	-	-	-	14	-	-	1,4,5,7
Reverse Current	$2\ I_R$	2	-	4.0	-	4.0	-	4.0	μAdc	-	10	-	10	-	20	μAdc	-	-	-	-	-	2	-	-	14	-	-	1,7
		6	-	4.0	-	4.0	-	4.0	μAdc	-	10	-	10	-	20	μAdc	-	-	-	-	-	6	-	-	14	-	-	1,7
	$4\ I_R$	1	-	8.0	-	8.0	-	8.0	μAdc	-	20	-	20	-	40	μAdc	-	-	-	-	-	1	-	-	14	-	-	2,6,7
Output Leakage Current	I_{CEX}	3	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	3	-	14	-	-	7
		4	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	4	-	14	-	-	1,5,7
		5	-	-	-	50	-	-	μAdc	-	-	-	100	-	-	μAdc	-	-	-	-	-	-	5	-	14	-	-	1,4,7
Forward Current	$2\ I_F$	2	-	-3.20	-	-3.20	-	-3.00	mAdc	-	-2.80	-	-2.80	-	-2.66	mAdc	-	-	-	-	-	2	-	-	-	14	-	7
		6	-	-3.20	-	-3.20	-	-3.00	mAdc	-	-2.80	-	-2.80	-	-2.66	mAdc	-	-	-	-	-	6	-	-	-	14	-	7
	$4\ I_F$	1	-	-6.40	-	-6.40	-	-6.00	mAdc	-	-5.60	-	-5.60	-	-5.32	mAdc	-	-	2.6	-	1	-	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{PDH}	14	-	-	-	46.0	-	-	mAdc	-	-	-	54.0	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	14	1,2,6,7,8,12,13
	I_{Max}	14	-	-	-	65.0	-	-	mAdc	-	-	-	80.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-		
Switching Times	t_{pd-}	1,5	-	-	25	80	-	-	ns	-	-	25	80	-	-	ns	Pulse In 1.6	Pulse Out 5	-	-	-	-	-	14	-	-	-	7
	t_{pd-}	1,5	-	-	10	30	-	-		-	-	10	30	-	-		1.6	5	-	-	-	-	-		-	-	-	
	t_{pd-}	1,4	-	-	25	80	-	-		-	-	25	80	-	-		1.6	4	-	-	-	-	-		-	-	-	
	t_{pd-}	1,4	-	-	10	30	-	-		-	-	10	30	-	-		1.6	4	-	-	-	-	-		-	-	-	

Pins not listed are left open.

PRODUCT DOCUMENTATION

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

See the **Additional Support** section of the *DSP56300 Family Manual* for detailed information on the multiple support options available to you.

Table 1 DSP56301 Documentation

Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/AD
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301/D

6367248 0157042 028