UNITRODE

UCC1921
UCC2921
UCC3921

Latchable Negative Floating Hot Swap Power Manager

FEATURES

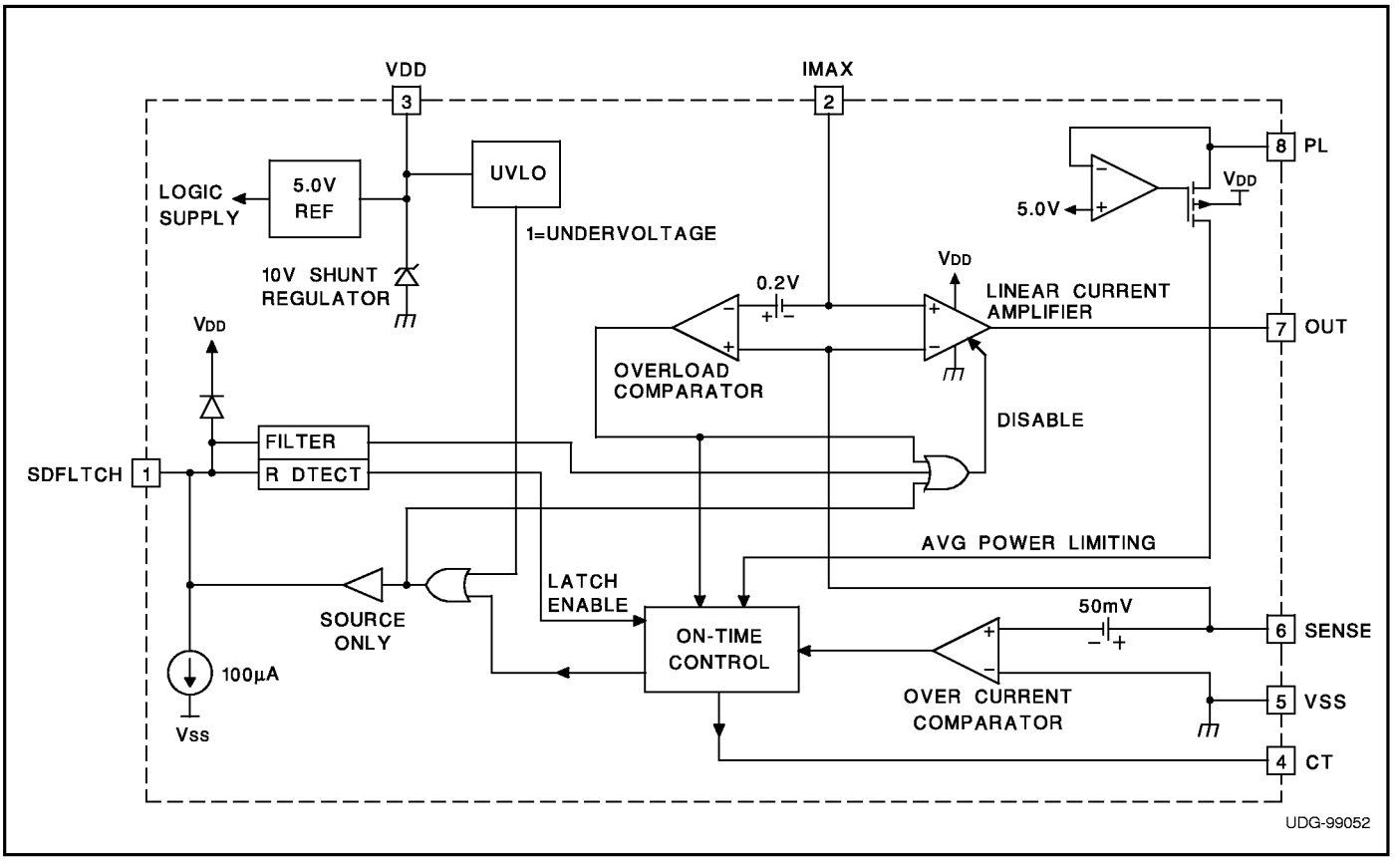
- Precision Fault Threshold
- Programmable:
  Average Power Limiting, Linear Current Control, Overcurrent Limit and Fault Time
- Fault Output Indication Signal
- Automatic Retry Mode or Latched Operation Mode
- Shutdown Control
- Undervoltage Lockout
- 250µs Glitch Filter on the SDFLTCH pin
- 8-Pin DIL and SOIC

DESCRIPTION

The UCC3921 family of negative floating hot swap power managers provides complete power management, hot swap, and fault handling capability. The IC is referenced to the negative input voltage and is powered through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The onboard 10V shunt regulator protects the IC from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, selection of Retry or Latched mode, soft start time, and average power limiting. In the event of a constant fault, the internal timer will limit the on time from less than 0.1% to a maximum of 3% duty cycle. The duty cycle modulation depends on the current into PL, which is a function of the voltage across the FET, thus limiting average power dissipation in the FET. The fault level is fixed at 50mV across the current sense amplifier to minimize total

(continued)

BLOCK DIAGRAM



DESCRIPTION (continued)

dropout. The fault current level is set with an external current sense resistor, while the maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on IMAX. The current level, when the output acts as a current source, is equal to VIMAX/RSENSE. If desired, a controlled current start up can be programmed with a capacitor on IMAX.

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and performs a retry some time later (provided that the selected mode of operation is Automatic Retry Mode). When the output current reaches the maximum sourcing current level, the output acts as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCC3921 include undervoltage lockout, 8-pin Small Outline (SOIC) and Dual-In-Line (DIL) packages, and a Latched Operation Mode option, in which the output is latched off once CT charges to 2.5V and stays off until either SDFLTCH is toggled (for greater than 1ms) or the IC is powered down and then back up.

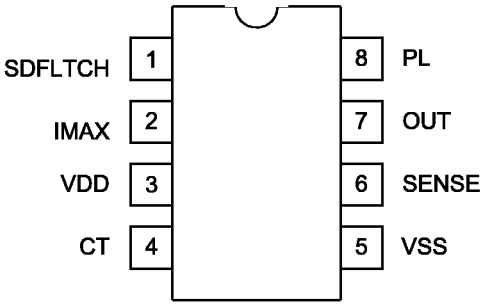
ABSOLUTE MAXIMUM RATINGS

IVDD 50mA
SDFLTCH Current 10mA
PL Current 10mA
IMAX Input Voltage . . . . . VDD
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to V_{SS} (the most negative voltage). Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8 , SOIC-8 (Top View)
N or J, D Packages



ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to 70°C for the UCC3921 and –40°C to 85°C for the UCC2921, and –55°C to 125°C for the UCC1921; I_{VDD} = 2mA, C_T = 1nF (the minimum allowable value), there is no resistor connected between the SDFLTCH and VSS pins. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD			1	2	mA
Regulator Voltage	I_{SOURCE} = 2mA	9	9.5	10.0	V
	I_{SOURCE} = 10mA	9.15	9.6	10.15	V
UVLO Off Voltage		6	7	8	V
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C	47.5	50	53.5	mV
	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	V_{CT} = 1V, I_{PL} = 0	–50	–36	–22	µA
	Overload Condition, V_{SENSE} - V_{IMAX} = 300mV	–1.7	–1.2	–0.7	mA
CT Discharge Current	V_{CT} = 1V, I_{PL} = 0	0.6	1	1.5	µA
CT Fault Threshold		2.2	2.45	2.6	V
CT Reset Threshold		0.41	0.49	0.57	V
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to 70°C for the UCC3921 and –40°C to 85°C for the UCC2921, and –55°C to 125°C for the UCC1921; V_{DD} = 2mA, C_T = 1nF (the minimum allowable value), there is no resistor connected between the SDFLTCH and VSS pins. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output High Voltage	I_{OUT} = 0mA	8.5	10		V
	I_{OUT} = –1mA	6	8		V
Output Low Voltage	I_{OUT} = 0mA, $V_{SENSE} - V_{IMAX}$ = 100mV		0	10	mV
	I_{OUT} = 2mA, $V_{SENSE} - V_{IMAX}$ = 100mV		200	600	mV
Linear Amplifier Section					
Sense Control Voltage	V_{IMAX} = 100mV	85	100	115	mV
	V_{IMAX} = 400mV	370	400	430	mV
Input Bias			50	500	nA
Power Limiting Section					
V_{SENSE} Regulator Voltage	I_{PL} = 64µA	4.35	4.85	5.35	V
Duty Cycle Control	I_{PL} = 64µA	0.6	1.2	1.7	%
	I_{PL} = 1mA	0.045	0.1	0.17	%
Overload Section					
Delay to Output	Note 1		300	500	ns
Output Sink Current	$V_{SENSE} - V_{IMAX}$ = 300mV	40	100		mA
Threshold	Relative to IMAX	140	200	260	mV
Shutdown/Fault/Latch Section					
Shutdown Threshold		3	5	VDD+1	V
Input Current	$V_{SDFLTCH}$ = 5V	50	110	250	µA
Filter Delay Time (Delay to Output)		250	500	1000	µs
Fault Output High		6	9.5		V
	$I_{SDFLTCH}$ = –100µA	5	8.5		V
Fault Output Low			0	10	mV
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%
	$I_{SDFLTCH}$ = –100µA, Fault Condition, I_{PL} = 0			0	%

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the fault time. The fault time must be longer than the time to charge external load capacitance. The fault time is defined as:

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}}$$

where I_{CH} = 36µA + I_{PL}, and I_{PL} is the current into the power limit pin. Once the maximum fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 2 \bullet 10^6 \bullet C_T$$

IMAX: This pin programs the maximum allowable sourcing current. Since VDD is a regulated voltage, a voltage divider can be derived from VDD to generate the program level for IMAX. The current level at which the output appears as a current source is equal to the voltage on IMAX over the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on IMAX, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUT: This pin provides gate output drive to the MOSFET pass element.

PL: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When I_{PL}>>36µA, then the average MOSFET power dissipation is given by:

$$P_{MOSFET}avg = IMAX \bullet 1 \bullet 10^{-6} \bullet R_{PL}$$

PIN DESCRIPTIONS (continued)

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VSS, then a fault is sensed, and C_T starts to charge.

SDFLTCH: This pin provides fault output indication, shutdown control, and operating mode selection. Interface into and out of this pin is usually performed through level shift transistors. When open, and under a non-fault condition, this pin pulls to a low state with respect to VSS. When a fault is detected by the fault timer, or undervoltage lockout, this pin will drive to a high state with respect fo VSS, indicating the NMOS pass element is OFF. When > 250µA is sourced into this pin for > 1ms, it drives high causing the output to disable the NMOS pass device.

If an 5k < R_{LATCH} < 250kΩ resistor is placed from this pin to VSS, then the latched operating mode will be invoked. Upon the occurrence of a fault, under the latched mode of operation, once the C_T capacitor charges up to 2.5V the NMOS pass element latches off. A retry will not periodically occur. To reset the latched off device, either SDFLTCH is toggled high for a duration greater than 1ms or the IC is powered down and then up.

VDD: Current driven with a resistor to a voltage approximately 10V more positive than VSS. Typically a resistor is connected to ground. The 10V shunt regulator clamps VDD approximately 10V above VSS, and is also used as an output reference to program the maximum allowable sourcing current.

VSS: Ground reference for the IC and the most negative voltage available.

APPLICATION INFORMATION

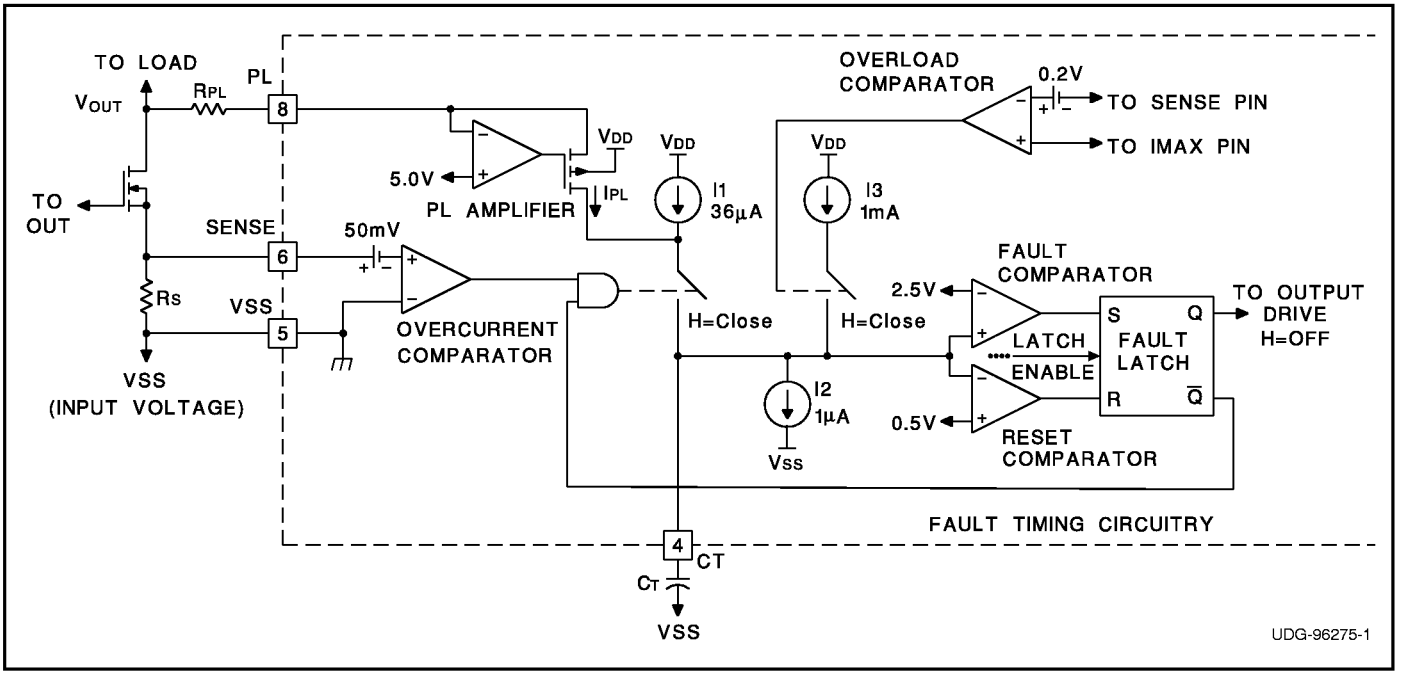


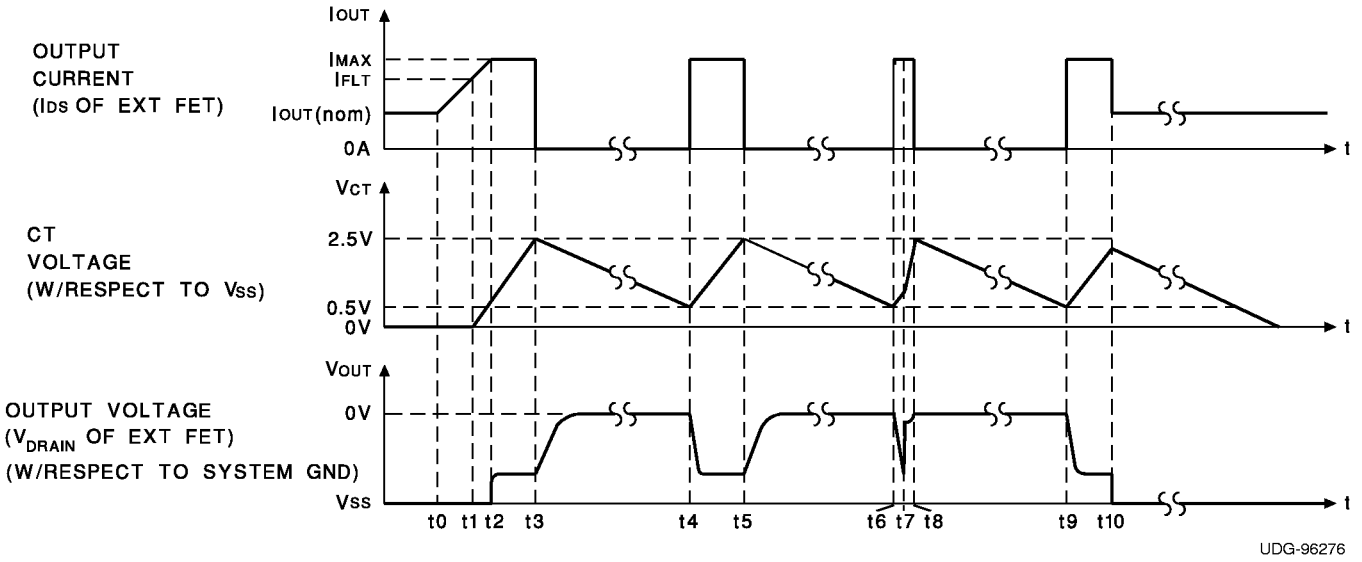
Figure 1. Fault Timing Circuitry for the UCC3921, Including Power Limit Overload

APPLICATION INFORMATION (continued)

Figure 1 shows the detailed circuitry for the fault timing function of the UCC3921. For the time being, we will discuss a typical fault mode, therefore, the overload comparator, and current source I3 does not work into the operation. Once the voltage across the current sense resistor, RS, exceeds 50mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36µA plus the current from the power limiting amplifier. The PL amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{V_{FET} - 5V}{R_{PL}}$$

where V_{FET} is the voltage across the NMOS pass device. Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a condition where the output current is more than the fault level, but less than the max level, $V_{OUT} \approx$ VSS (input voltage), $I_{PL} = 0$, the CT charging current is 36µA.



t0: Safe condition. Output current is nominal, output voltage is at the negative rail, VSS.

t1: Fault control reached. Output current rises above the programmed fault value, CT begins to charge at ~36µA.

t2: Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs. CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground.

t4: Retry. CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down towards VSS.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4: Retry. CT has discharged to 0.5V, but fault is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down towards VSS.

t7: Output short circuit. If VOUT is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and R_{PL}.

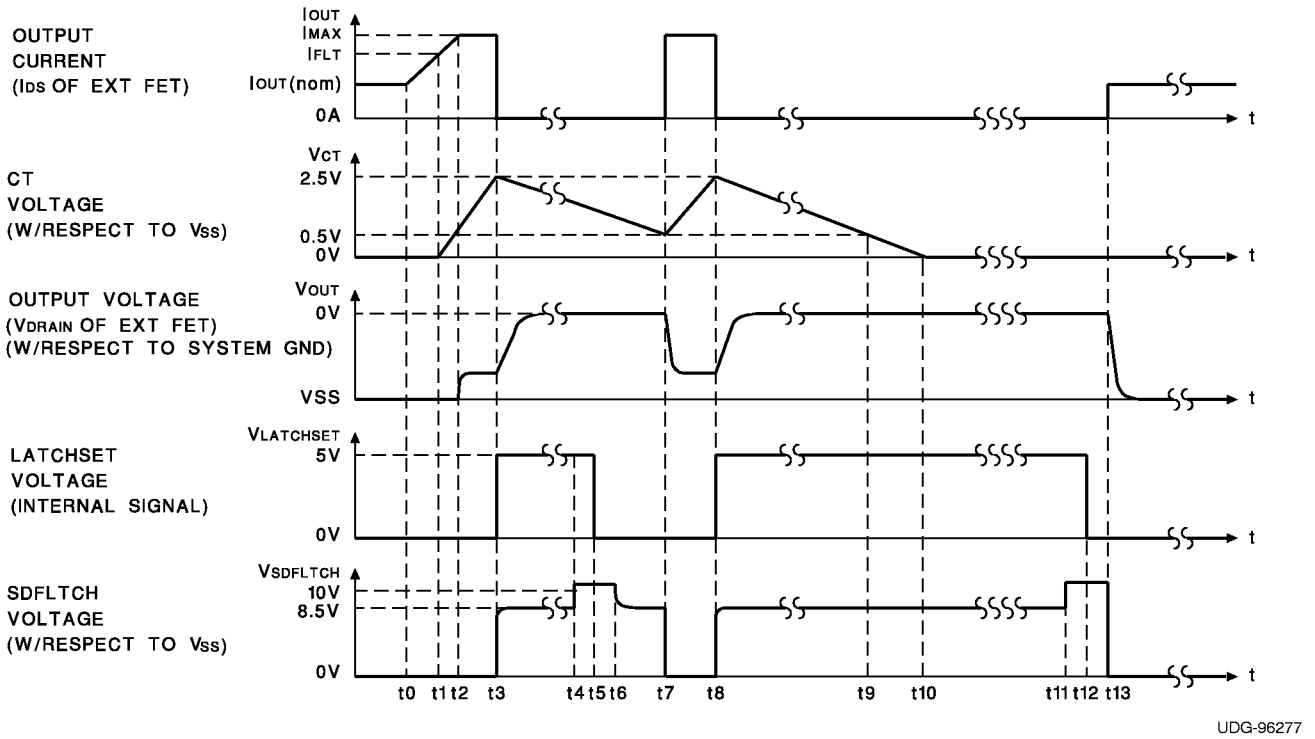
t8: Fault occurs. Output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9 = t4: Output short circuit released, still in fault mode.

t10 = t0: Fault released, safe condition. Return to normal operation of the hot swap power manager.

Figure 2. Retry Operation Mode

APPLICATION INFORMATION (cont.)



t0: Safe condition. Output current is nominal, output voltage is at the negative rail, VSS.

t1: Fault control reached. Output current rises above the programmed fault value, CT begins to charge at ~36µA.

t2: Maximum current reached. Output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs. CT has charged to 2.5V, fault output goes high as indicated by the SDFLTCH voltage. The FET turns off allowing no output current to flow, V_{OUT} floats up to ground, and since there is an 82kΩ resistor from the SDFLTCH pin to VSS, the internal latchset signal goes high.

t4: Since the user does not want the chip to LATCH off during this cycle, he toggles SDFLTCH high for greater than 1ms {t6 - t4 > 1ms}.

t5: The latchset signal is reset.

t6: Forcing of SDFLTCH is released after having been applied for > 1ms.

t7: Retry (since the latchset signal has been reset to its' low state) - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down towards VSS.

t8 = t3: Fault occurs. CT has charged to 2.5V, fault output goes high as indicated by the SDFLTCH voltage, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground, and since there is an 82kΩ resistor from SDFLTCH to VSS, the internal latchset signal goes high.

t9: Output is latched off. Even though CT has discharged to 0.5V, there will not be a retry since the latchset signal was allowed to remain high.

t10: Output remains latched off. CT has discharged all the way to 0V.

t11: The output has been latched off for quite some time. The user now wishes to reset the latched off output, thus toggling SDFLTCH high for greater than 1ms {t13 - t11}.

t12 = t5: The latchset signal is reset.

t13: Forcing of SDFLTCH is released after having been applied for > 1ms. The fault had also been released during the time the output was latched off, safe condition, return to normal operation of the hot swap power manager.

Figure 3. Latched Operation Mode: R_{LATCH} = 82k

APPLICATION INFORMATION (continued)

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capacitor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with the 1µA current source, I2, until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator will close the charging switch causing the cycle to repeat. Under a constant fault, the duty cycle is given by:

$$Duty\ Cycle = \frac{1\mu A}{I_{PL} + 36\mu A}$$

Average power dissipation in the pass element is given by:

$$P_{FET_{AVG}} = V_{FET} \bullet I_{MAX} \bullet \frac{1\mu A}{I_{PL} + 36\mu A}$$

Where V_{FET}>>5V I_{PL} can be approximated as:

$$\frac{V_{FET}}{R_{PL}}$$

and where I_{PL}>>36µA, the duty cycle can be approximated as :

$$\frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = V_{FET} \bullet I_{MAX} \bullet \frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

$$= IMAX \bullet 1\mu A \bullet R_{PL}$$

Notice that in the approximation, V_{FET} cancels, thereby limiting the average power dissipation in the NMOS pass element.

Overload Comparator

The linear amplifier in the UCC3921 ensures that the output NMOS does not pass more than I_{MAX} (which is V_{IMAX}/R_{SENSE}). In the event the output current exceeds the programmed I_{MAX} by 0.2V/R_{SENSE}, which can only occur if the output FET is not responding to a command from the IC, CT will begin charging with I3, 1mA, and continue to charge to approximately 8V. This allows a constant fault to show up on the SDFLTCH pin, and also since the voltage on CT will continue charging past 2.5V in an overload fault mode, it can be used for detection of output FET failure or to build redundancy into the system.

Determining External Component Values

To set R_{VDD} (see Fig. 4) the following must be achieved:

$$\frac{V_{IN}\ min}{R_{VDD}} > \frac{10V}{R1 + R2} + 2mA$$

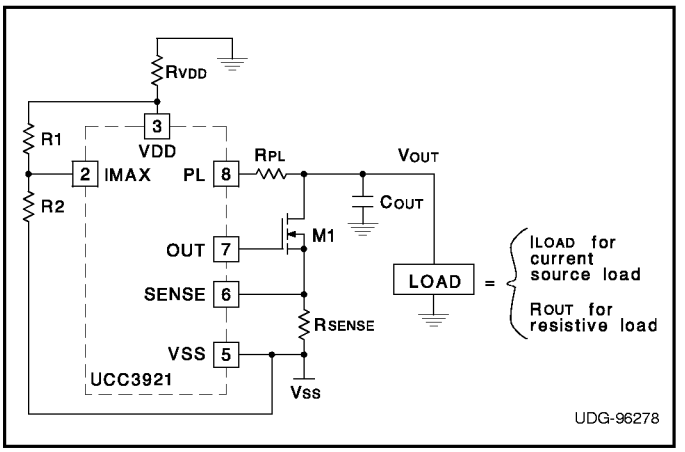


Figure 4.

In order to estimate the minimum timing capacitor, C_T, several things must be taken into account. For example, given the schematic in Figure 4 as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate C_{TMIN}. Now, given the values of C_{OUT}, Load, R_{SENSE}, V_{SS}, and the resistors determining the voltage on the IMAX pin, the user can calculate the approximate startup time of the node V_{OUT}. This startup time must be faster than the time it takes for C_T to charge to 2.5V (relative to V_{SS}), and is the basis for estimating the minimum value of C_T. In order to determine the value of the sense resistor, R_{SENSE}, assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

Next, the variable I_{MAX} must be calculated. I_{MAX} is the maximum current that the UCC3921 will allow through the transistor, M1, and it can be shown that during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value I_{MAX} where

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}}$$ where V_{IMAX} = voltage on pin IMAX.

Given this information, calculation of the startup time is now possible via the following:

APPLICATION INFORMATION (continued)

Current Source Load:

$$T_{START} = \frac{C_{OUT} \bullet |V_{SS}|}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = C_{OUT} \bullet R_{OUT} \bullet \ell n\left(\frac{I_{MAX} \bullet R_{OUT}}{I_{MAX} \bullet R_{OUT} - |V_{SS}|}\right)$$

Once T_{START} is calculated, the power limit feature of the UCC3921 must be addressed and component values derived. Assuming the user chooses to limit the maximum

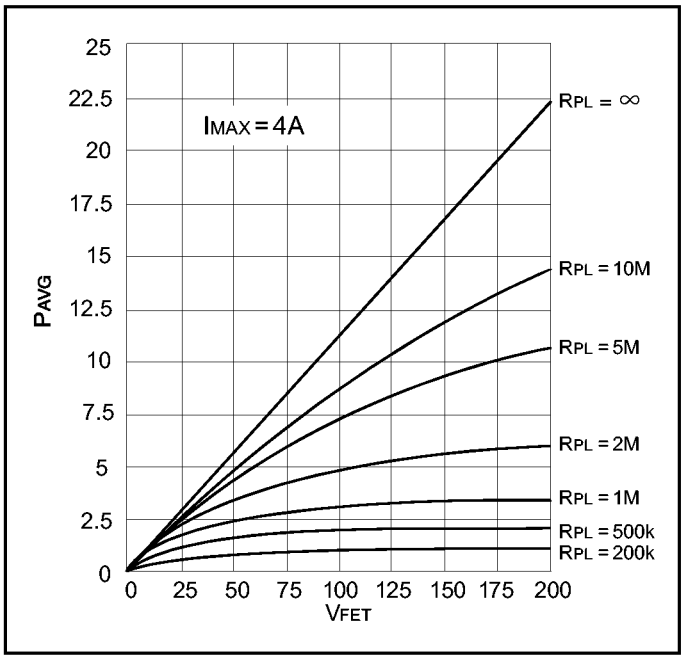


Figure 5. Plot Average Power vs FET Voltage for Increasing Values of R_{PL}

allowable average power that will be associated with the hot swap power manager, the power limiting resistor, RPL, can be easily determined by the following:

$$R_{PL} = \frac{P_{FET}\ avg}{1\mu A \bullet I_{MAX}}$$ where a minimum RPL exists

defined by $R_{PL}\ \text{min} = \frac{|V_{SS}|}{5mA}$ (Refer to Figure 5).

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived as such:

Current Source Load:

$$C_T\ \text{min} = \frac{3 \bullet T_{START} \bullet (72\mu A \bullet R_{PL} + |V_{SS}| - 10V)}{10 \bullet R_{PL}}$$

Resistive Load:

$$C_T\ \text{min} = \frac{3 \bullet T_{START} \bullet (36\mu A \bullet R_{PL} + |V_{SS}| - 5V - I_{MAX} \bullet R_{OUT})}{5 \bullet R_{PL}} + \frac{3 \bullet R_{OUT} \bullet |V_{SS}| \bullet C_{OUT}}{5 \bullet R_{PL}}$$

Level Shift Circuitry to Interface with SDFLTCH

Some type of circuit is needed to interface with the UCC3921 via SDFLTCH, such as opto-couplers or level shift circuitry. Figure 6 depicts one implementation of level shift circuitry that could be used, showing component values selected for a typical –48V telecommunications application. There are three communication conditions which could occur; two of which are Hot Swap Power Manager (HSPM) state output indications, and the third being an External Shutdown.

1) When open, and under a non-fault condition, SDFLTCH is pulled to a low state. In Figure 6, the N-channel level shift transistor is off, and the FAULT OUT signal is pulled to LOCAL VDD through R3. This indicates that the HSPM is not faulted.

2) When a fault is detected by the fault timer or undervoltage lockout, this pin will drive to a high state, indicating that the external power FET is off. In Figure 6, the N-channel level shift transistor will conduct, and the FAULT OUT signal will be pulled to a Schottky Diode voltage drop below LOCAL GND. This indicates that the HSPM is faulted. The Schottky Diode is necessary to ensure that the FAULT OUT signal does not traverse too far below LOCAL GND, making fault detection difficult.

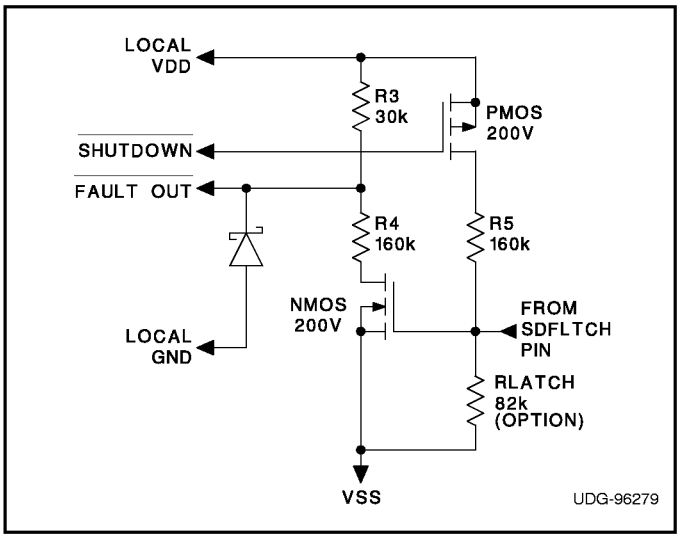


Figure 6. Possible Level Shift Circuitry to Interface to the UCC3921, showing component values selected for a typical telecom application.

APPLICATION INFORMATION (continued)

If a 5k < R_{LATCH} < 250kΩ resistor is tied between SDFLTCH & VSS, as optionally shown in Figure 6, then the latched operating mode (described earlier) will be invoked upon the occurrence of a fault.

3) To externally shutdown the HSPM, the $\overline{\text{SHUTDOWN}}$ signal (typically held at LOCAL VDD) must be pulled to LOCAL GND. Assuming $\overline{\text{SHUTDOWN}}$ is tied to LOCAL GND, the P-channel level shift transistor will conduct, driving SDFLTCH high (to roughly VDD plus a diode). By sourcing > 250µA into SDFLTCH for > 1ms the output to the external power FET will be disabled. The current sourced into SDFLTCH must be limited to 10mA or less: $I_{SDFLTCHMAX}$ < 10mA.

SAFETY RECOMMENDATIONS

Although the UCC3921 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3921 is intended for use in safety critical applications where UL® or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the external power FET. The UCC3921 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

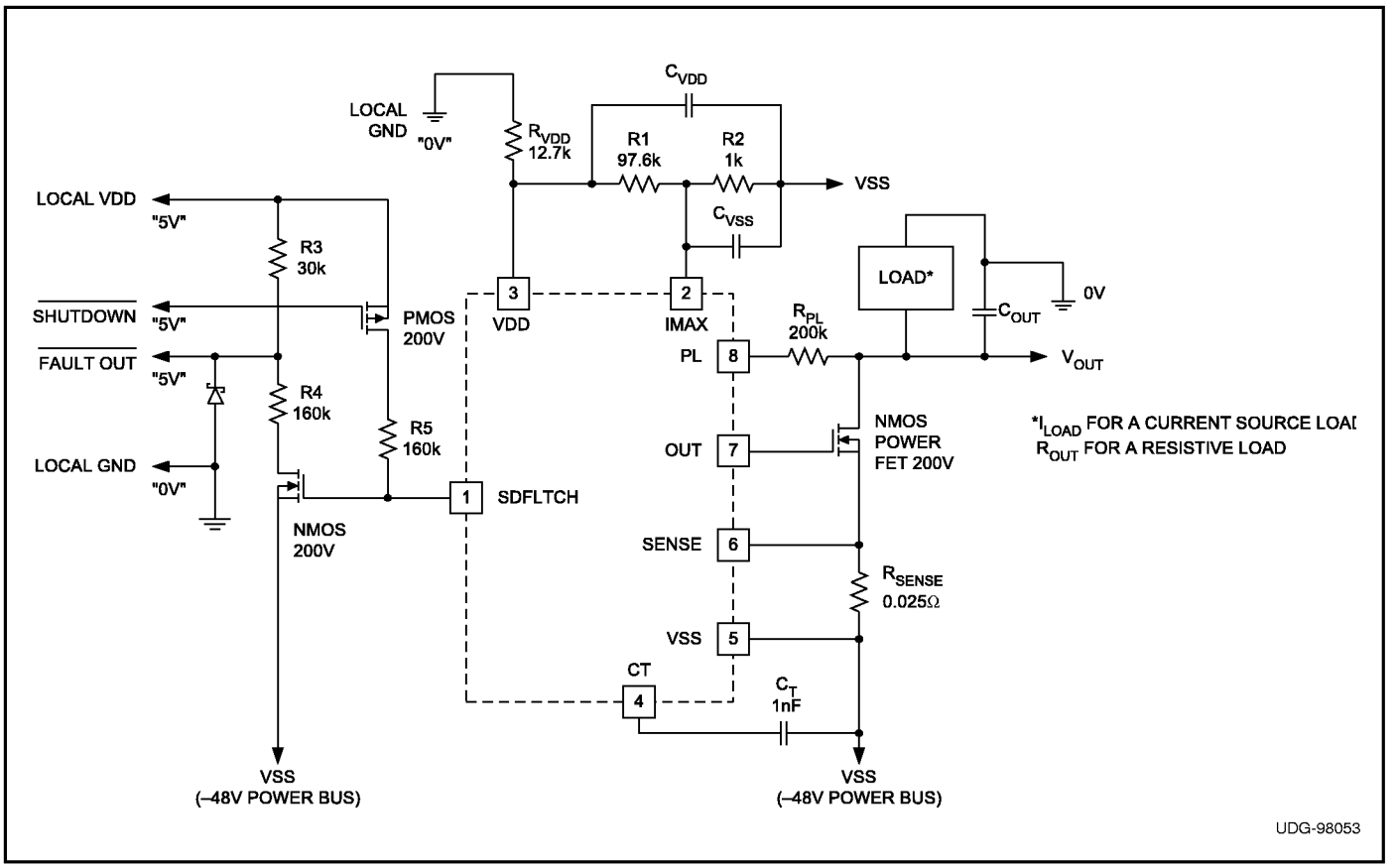


Figure 7. Typical Telecommuications Application

(The "Negative Magnitude-Side" of the Supply is Switched in)

APPLICATION INFORMATION (continued)

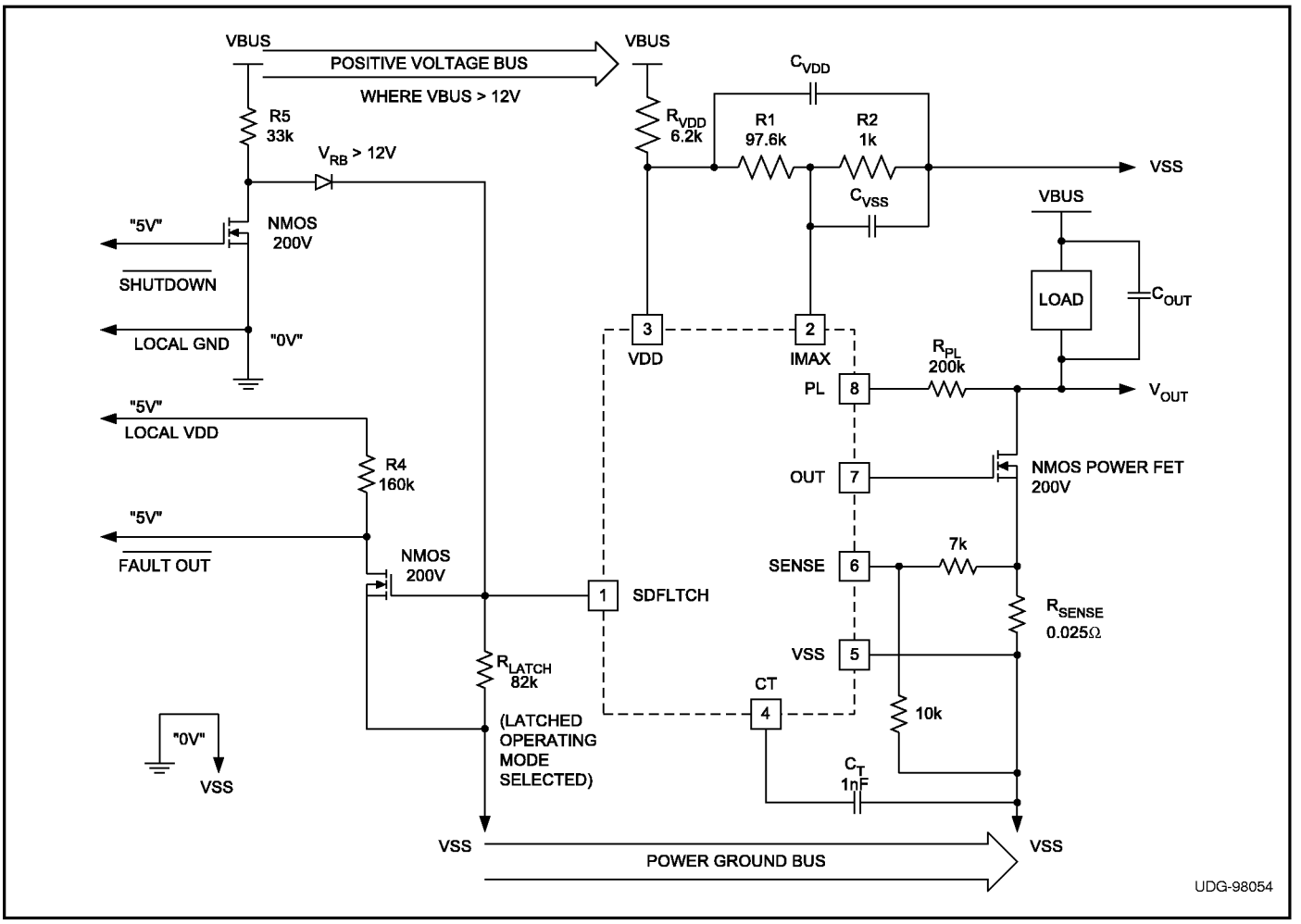


Figure 8. Floating Positive Application

The "Ground-side" of the Supply is Switched In

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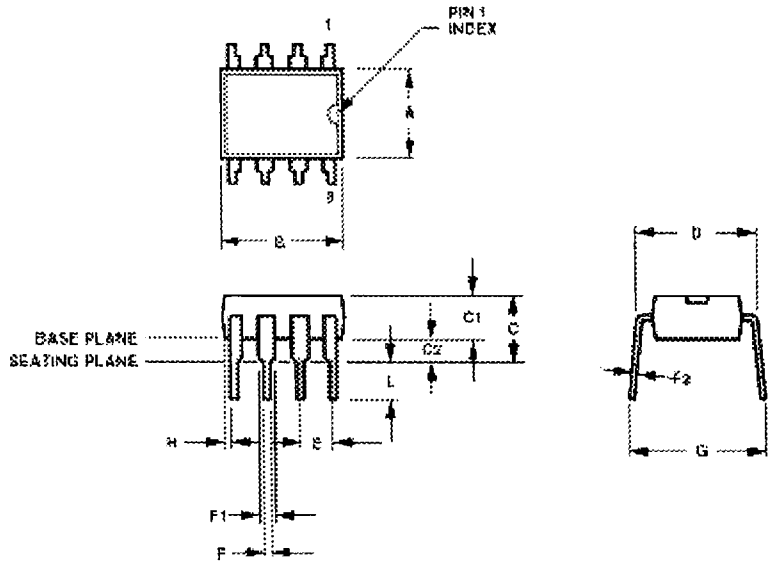
Mechanical Drawings

Back to Packaging Index

8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

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UNITRODE

Mechanical Drawings

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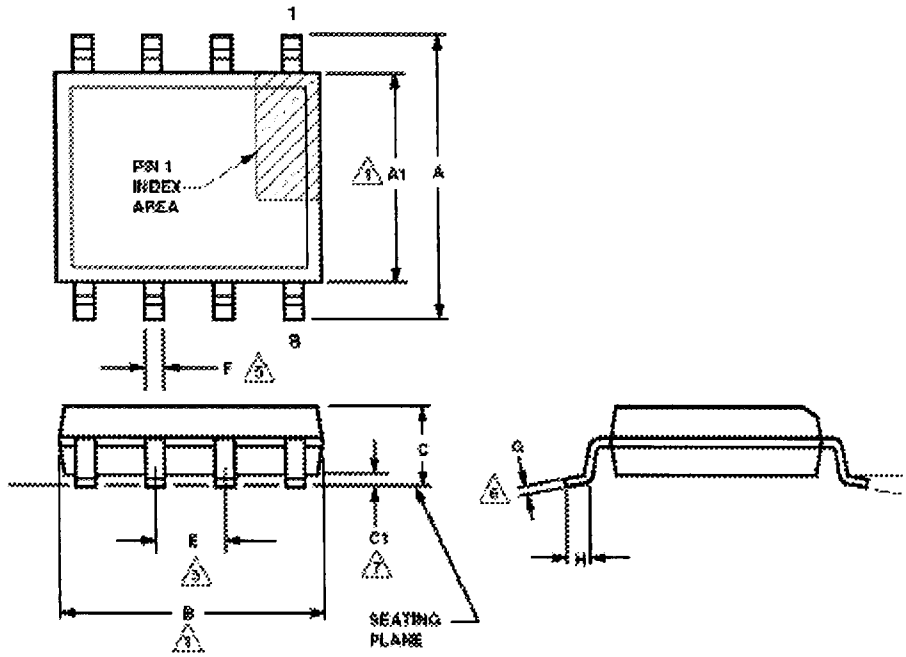
8-PIN SOIC SURFACE MOUNT~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

UNITRODE

Mechanical Drawings

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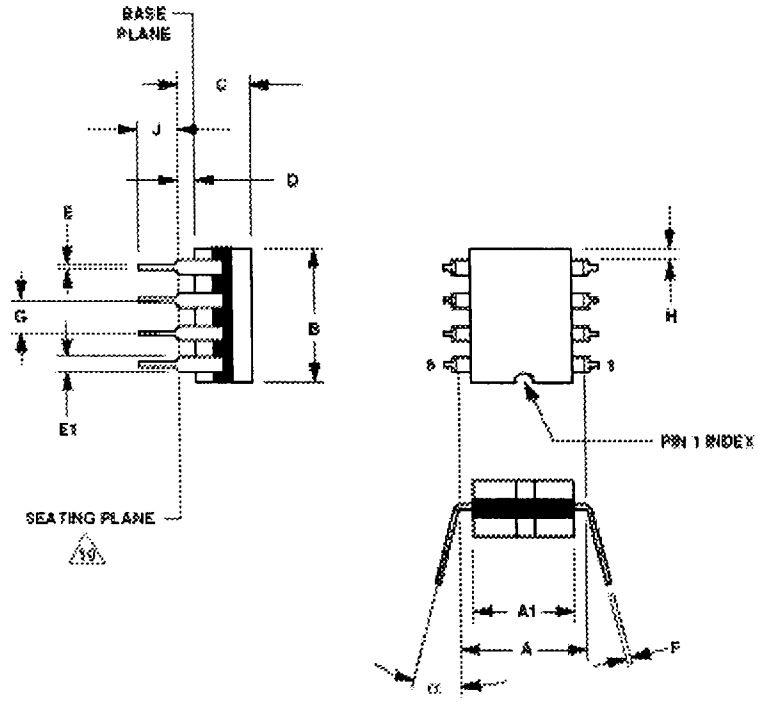
8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.405	-	10.29	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.