

# CD4026A, CD4033A Types

## CMOS Decade Counters/Dividers

With Decoded 7-Segment Display Outputs and:  
 Display Enable – CD4026A  
 Ripple Blanking – CD4033A

The RCA-CD4026A and CD4033A each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display.

These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.

Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026A include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033 are RIPPLE-BLANKING INPUT and LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The CARRY-OUT (C<sub>OUT</sub>) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033A; in the CD4026A these outputs go high only when the DISPLAY ENABLE IN is high.

### CD4026A

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

### CD4033A

The CD4033A has provisions for automatic blanking of the non-significant zeros in a

multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033A associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033A in the next-lower significant position in the display. This procedure is continued for each succeeding CD4033A on the integer side of the display.

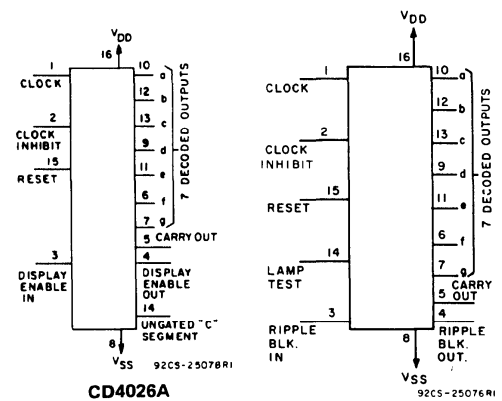
On the fraction side of the display the RBI of the CD4033A associated with the least significant bit is connected to a low level voltage and the RBO of that CD4033A is connected to the RBI terminal of the CD4033A in the next more-significant-bit position. Again, this procedure is continued for all CD4033A's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For Example: optional zero → 0.7346.

Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033A associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033A has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.



CD4026A  
 CD4033A  
 FUNCTIONAL DIAGRAMS

### Features:

- Counter and 7-segment decoding in one package
- Easily interfaced with 7-segment display types
- Fully static counter operation: DC to 2.5 MHz (typ.)
- Ideal for low-power displays
- Display Enable Output (CD4026A)
- "Ripple Blanking" and Lamp Test (CD4033A)
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

### Applications:

- Decade counting/7-segment decimal display
- Frequency division/7-segment decimal displays
- Clock/watches/timers (e.g. ÷ 60, ÷ 60, ÷ 12 counter/display)
- Counter/display driver for meter applications

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |       |                                       |
|---|-------|---------------------------------------|
| STORAGE-TEMPERATURE RANGE (T <sub>stg</sub> )                           | ..... | -65 to +150°C                         |
| OPERATING-TEMPERATURE RANGE (T <sub>A</sub> ):                          |       |                                       |
| PACKAGE TYPES D, F, K, H  | ..... | -55 to +125°C                         |
| PACKAGE TYPE E  | ..... | -40 to +85°C                          |
| DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )                             |       |                                       |
| (Voltages referenced to V <sub>SS</sub> Terminal):                      | ..... | -0.5 to +15 V                         |
| POWER DISSIPATION PER PACKAGE (P <sub>D</sub> )                         |       |                                       |
| FOR T <sub>A</sub> = -40 to +60°C (PACKAGE TYPE E)                      | ..... | .500 mW                               |
| FOR T <sub>A</sub> = +60 to +85°C (PACKAGE TYPE E)                      | ..... | Derate Linearly at 12 mW/°C to 200 mW |
| For T <sub>A</sub> = -55 to +100°C (PACKAGE TYPES D, F, K)              | ..... | 500 mW                                |
| For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPES D, F, K)             | ..... | Derate Linearly at 12 mW/°C to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                |       |                                       |
| FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) | ..... | 100 mW                                |
| INPUT VOLTAGE RANGE, ALL INPUTS   | ..... | -0.5 to V <sub>DD</sub> + 0.5 V       |
| LEAD TEMPERATURE (DURING SOLDERING):                                    |       |                                       |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.   | ..... | +265°C                                |

# CD4026A, CD4033A Types

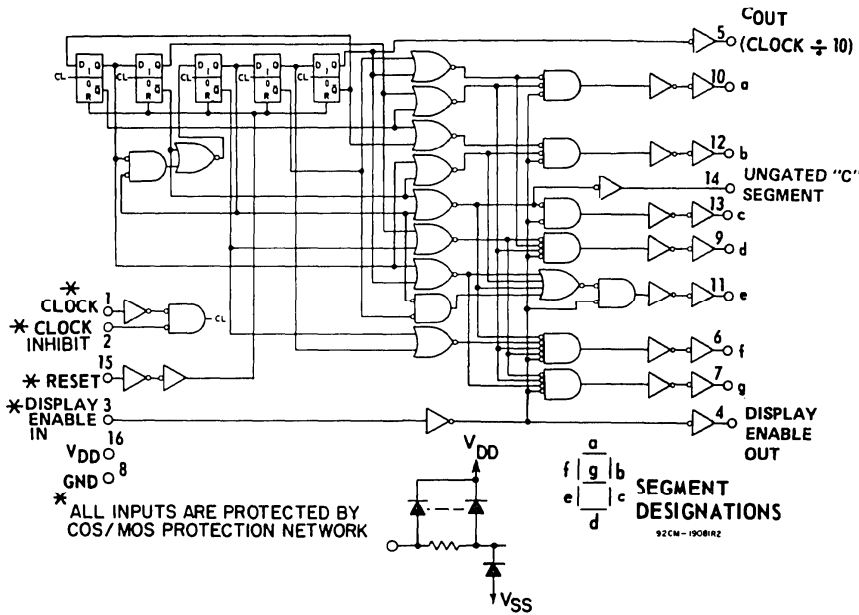


Fig. 1 - CD4026A logic diagram.

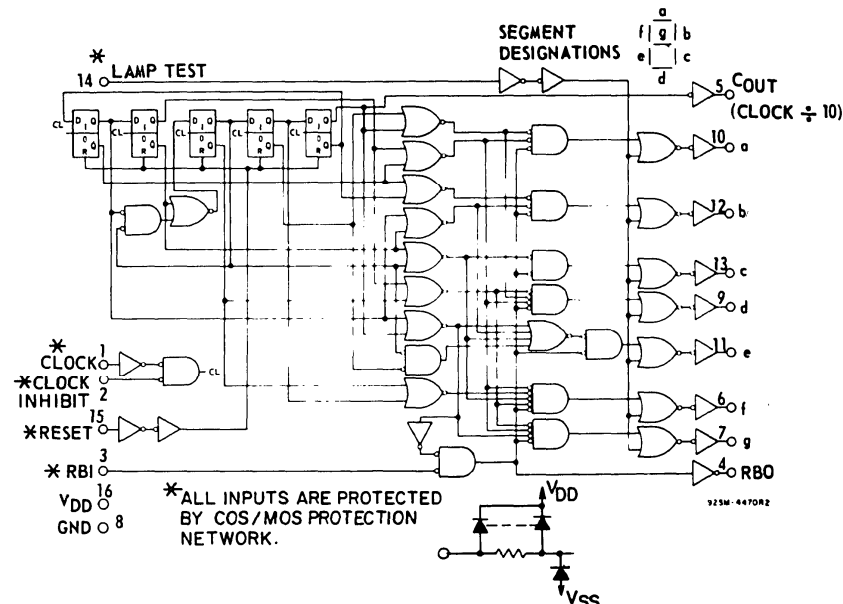


Fig. 3 - CD4033A logic diagram.

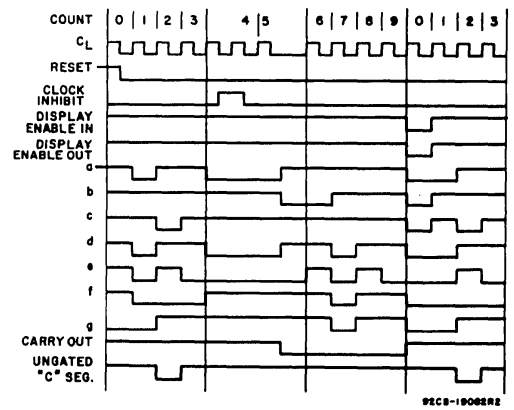


Fig. 2 - CD4026A timing diagram.

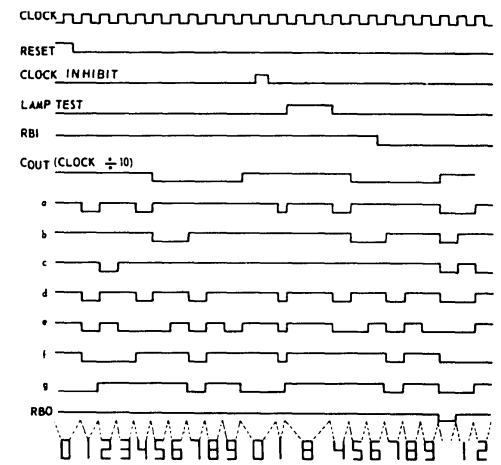


Fig. 4 - CD4033A timing diagram.

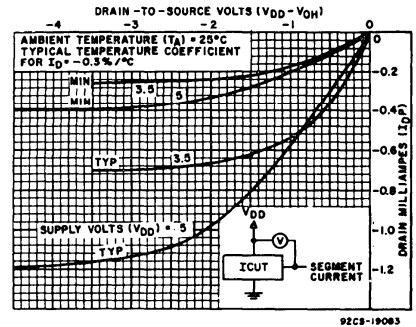


Fig. 5 - Minimum and typical output p-channel decoded drain characteristics @ VDD=3.5 & 5 V.

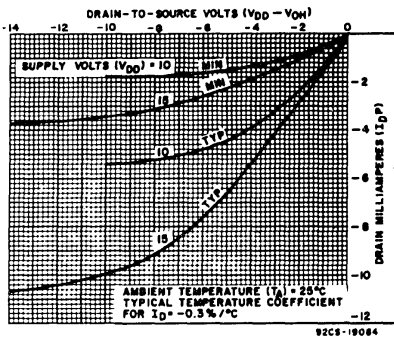


Fig. 6 - Minimum and typical output p-channel decoded drain characteristics @ VDD=10 & 15 V.

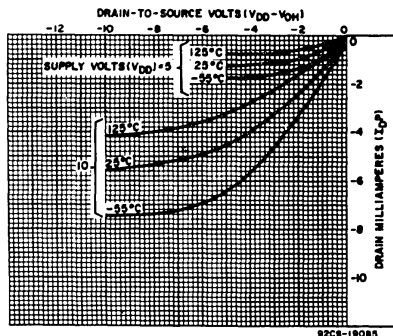


Fig. 7 - Typical output p-channel decoded drain characteristics as a function of temperature.

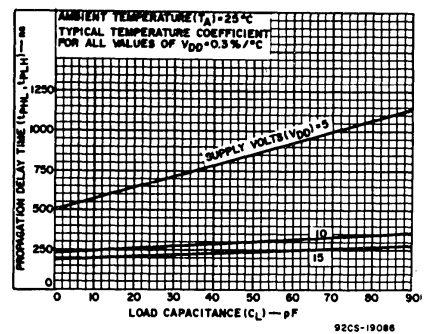


Fig. 8 - Typical propagation delay time vs. CL for decoded outputs.

# CD4026A, CD4033A Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC  | V <sub>DD</sub> (V) | LIMITS              |          |             |          | UNITS         |
|---|---------------------|---------------------|----------|-------------|----------|---------------|
|   |                     | D, F, K, H Packages |          | E Package   |          |               |
|   |                     | Min.                | Max.     | Min.        | Max.     |               |
| Supply-Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ ) |                     | 3                   | 12       | 3           | 12       | V             |
| Clock Inhibit Setup Time, $t_S$   | 5<br>10             | 500<br>200          | —        | 700<br>300  | —        | ns            |
| Clock Pulse Width, $t_W$  | 5<br>10             | 330<br>170          | —        | 500<br>250  | —        | ns            |
| Clock Input Frequency, $f_{CL}$   | 5<br>10             | dc<br>dc            | 1.5<br>3 | dc<br>dc    | 1<br>2   | MHz           |
| Clock Rise or Fall Time, $t_{rCL}$ , $t_{fCL}$                            | 5<br>10             | —<br>—              | 15<br>15 | —<br>—      | 15<br>15 | $\mu\text{s}$ |
| Reset Pulse Width, $t_W$  | 5<br>10             | 330<br>165          | —        | 550<br>250  | —        | ns            |
| Reset Removal Time  | 5<br>10             | 750<br>225          | —        | 1000<br>275 | —        | ns            |

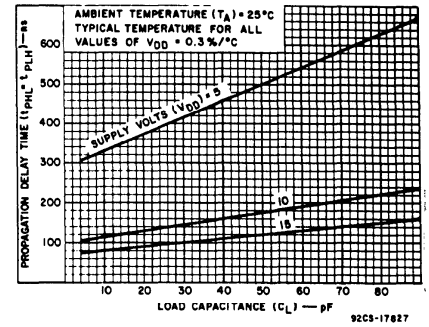


Fig. 9 – Typical propagation delay time vs.  $C_L$  for carry outputs.

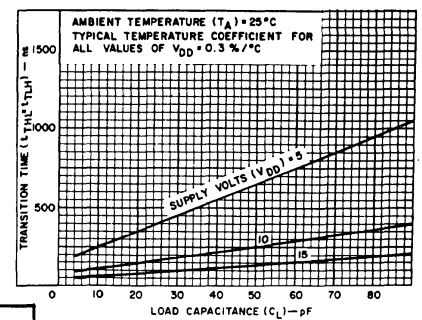


Fig. 10 – Typical transition time vs.  $C_L$  for decoded outputs.

## STATIC ELECTRICAL CHARACTERISTICS

| Characteristic                                       | Conditions         |                     |                     | Limits at Indicated Temperatures ( $^\circ\text{C}$ ) |             |              |       |           |             |              |       | Units         |    |
|--|--------------------|---------------------|---------------------|---|-------------|--------------|-------|-----------|-------------|--------------|-------|---------------|----|
|  |                    |                     |                     | D, F, K, H Packages                                   |             |              |       | E Package |             |              |       |               |    |
|  | V <sub>O</sub> (V) | V <sub>IN</sub> (V) | V <sub>DD</sub> (V) | -55   | +25<br>Typ. | +25<br>Limit | +125  | -40       | +25<br>Typ. | +25<br>Limit | +85   |               |    |
| Quiescent Device Current $I_L$ Max.                  | —                  | —                   | 5                   | 5   | 0.3         | 5            | 300   | 50        | 0.5         | 50           | 700   | $\mu\text{A}$ |    |
|  | —                  | —                   | 10                  | 10  | 0.5         | 10           | 600   | 100       | 1           | 100          | 1400  |               |    |
|  | —                  | —                   | 15                  | 50  | 1           | 50           | 2000  | 500       | 5           | 500          | 5000  |               |    |
| Output Voltage: Low-Level, $V_{OL}$                  | —                  | 5                   | 5                   | 0 Typ.; 0.05 Max.                                     |             |              |       |           |             |              |       | V             |    |
|  | —                  | 10                  | 10                  | 0 Typ.; 0.05 Max.                                     |             |              |       |           |             |              |       |               |    |
| High Level, $V_{OH}$                                 | —                  | 0                   | 5                   | 4.95 Min.; 5 Typ.                                     |             |              |       |           |             |              |       | V             |    |
|  | —                  | 0                   | 10                  | 9.95 Min.; 10 Typ.                                    |             |              |       |           |             |              |       |               |    |
| Noise Immunity: Inputs Low, $V_{NL}$                 | —                  | —                   | 5                   | 1.5 Min.; 2.25 Typ.                                   |             |              |       |           |             |              |       | V             |    |
|  | —                  | —                   | 10                  | 3 Min.; 4.5 Typ.                                      |             |              |       |           |             |              |       |               |    |
| Inputs High, $V_{NH}$                                | —                  | —                   | 5                   | 1.5 Min.; 2.25 Typ.                                   |             |              |       |           |             |              |       | V             |    |
|  | —                  | —                   | 10                  | 3 Min.; 4.5 Typ.                                      |             |              |       |           |             |              |       |               |    |
| Noise Margin: Inputs Low, $V_{NML}$                  | 4.5                | —                   | 5                   | 1 Min.  |             |              |       |           |             |              |       | V             |    |
|  | 9                  | —                   | 10                  | 1 Min.  |             |              |       |           |             |              |       |               |    |
| Inputs High, $V_{NMH}$                               | 0.5                | —                   | 5                   | 1 Min.  |             |              |       |           |             |              |       | V             |    |
|  | 1                  | —                   | 10                  | 1 Min.  |             |              |       |           |             |              |       |               |    |
| Output Drive Current n-Channel (Sink), $I_{DN}$ Min. | Decoded Outputs    | 0.5                 | —                   | 5   | 0.15        | 0.24         | 0.12  | 0.09      | 0.08        | 0.24         | 0.06  | 0.05          | mA |
|  |                    | 0.5                 | —                   | 10  | 0.32        | 0.5          | 0.25  | 0.18      | 0.15        | 0.5          | 0.12  | 0.1           |    |
|  | Carry Output       | 0.5                 | —                   | 5   | 0.12        | 0.4          | 0.15  | 0.1       | 0.095       | 0.4          | 0.08  | 0.06          |    |
|  |                    | 0.5                 | —                   | 10  | 0.45        | 1            | 0.35  | 0.25      | 0.3         | 1            | 0.25  | 0.2           |    |
| p-Channel (Source), $I_{DP}$ Min.                    | Decoded Outputs    | 4.5                 | —                   | 5   | -0.21       | -0.28        | -0.14 | -0.1      | -0.09       | -0.28        | -0.07 | -0.06         | mA |
|  |                    | 9.5                 | —                   | 10  | -0.45       | -0.6         | -0.3  | -0.22     | -0.2        | -0.6         | -0.15 | -0.13         |    |
|  | Carry Output       | 4.5                 | —                   | 5   | -0.12       | -0.4         | -0.15 | -0.1      | -0.095      | -0.4         | -0.08 | -0.06         |    |
|  |                    | 9.5                 | —                   | 10  | -0.45       | -1           | -0.35 | -0.25     | -0.3        | -1           | -0.24 | -0.2          |    |
| Input Leakage Current, $I_{IL}$ , $I_{IH}$           | Any Input          |                     |                     | $\pm 10^{-5}$ Typ., $\pm 1$ Max.                      |             |              |       |           |             |              |       | $\mu\text{A}$ |    |

# CD4026A, CD4033A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 15\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC  | TEST CONDITIONS | LIMITS              |      |      |           |      |      |      | UNITS         |
|---|-----------------|---------------------|------|------|-----------|------|------|------|---------------|
|   |                 | D, F, K, H Packages |      |      | E Package |      |      |      |               |
|   |                 | VDD (V)             | Min. | Typ. | Max.      | Min. | Typ. | Max. |               |
| <b>CLOCKED OPERATION</b>  |                 |                     |      |      |           |      |      |      |               |
| Propagation Delay Time; $t_{PLH}, t_{PHL}$<br>Carry Out Line    |                 | 5                   | —    | 350  | 1000      | —    | 350  | 1300 | ns            |
|   |                 | 10                  | —    | 125  | 250       | —    | 125  | 300  |               |
| Decode Out Lines  |                 | 5                   | —    | 600  | 1700      | —    | 600  | 2200 | ns            |
|   |                 | 10                  | —    | 250  | 500       | —    | 250  | 700  |               |
| Transition Time; $t_{THL}, t_{TLH}$<br>Carry Out Line           |                 | 5                   | —    | 100  | 300       | —    | 100  | 350  | ns            |
|   |                 | 10                  | —    | 50   | 150       | —    | 50   | 200  |               |
| Decode Out Lines  |                 | 5                   | —    | 300  | 900       | —    | 300  | 1200 | ns            |
|   |                 | 10                  | —    | 125  | 350       | —    | 125  | 450  |               |
| Maximum Clock Input Frequency, $f_{CL}^\Delta$                  |                 | 5                   | 1.5  | 2.5  | —         | 1    | 2.5  | —    | MHz           |
|   |                 | 10                  | 3    | 5    | —         | 2    | 5    | —    |               |
| Min. Clock Pulse Width, $t_W$                                   |                 | 5                   | —    | 200  | 330       | —    | 200  | 500  | ns            |
|   |                 | 10                  | —    | 100  | 170       | —    | 100  | 250  |               |
| Clock Rise & Fall Time; $t_{rCL}, t_{fCL}$                      |                 | 5                   | —    | —    | 15        | —    | —    | 15   | $\mu\text{s}$ |
|   |                 | 10                  | —    | —    | 15        | —    | —    | 15   |               |
| Min. Clock Inhibit Set Up Time, $t_S$                           |                 | 5                   | —    | 175  | 500       | —    | 175  | 700  | ns            |
|   |                 | 10                  | —    | 75   | 200       | —    | 75   | 300  |               |
| Average Input Capacitance, $C_I$                                | Any Input       | —                   | 5    | —    | —         | 5    | —    | pF   |               |
| <b>RESET OPERATION</b>  |                 |                     |      |      |           |      |      |      |               |
| Propagation Delay Time; $t_{PLH}, t_{PHL}$<br>To Carry Out Line |                 | 5                   | —    | 350  | 1000      | —    | 350  | 1300 | ns            |
|   |                 | 10                  | —    | 125  | 250       | —    | 125  | 300  |               |
| To Decode Out Lines   |                 | 5                   | —    | 550  | 1400      | —    | 550  | 1900 | ns            |
|   |                 | 10                  | —    | 240  | 500       | —    | 240  | 600  |               |
| Min. Reset Pulse Width $t_W$                                    |                 | 5                   | —    | 200  | 330       | —    | 200  | 500  | ns            |
|   |                 | 10                  | —    | 100  | 165       | —    | 100  | 250  |               |
| Min. Reset Removal Time   |                 | 5                   | —    | 300  | 750       | —    | 300  | 1000 | ns            |
|   |                 | 10                  | —    | 100  | 225       | —    | 100  | 275  |               |

$\Delta$  Measured with respect to carry out line.

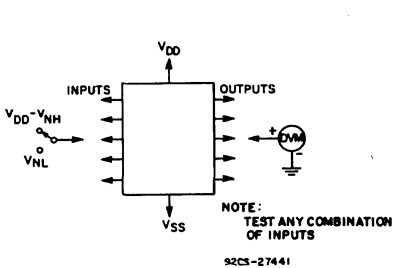


Fig. 14 - Noise immunity test circuit.

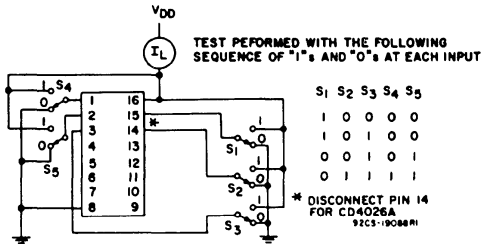


Fig. 15 - Quiescent device current test circuit.

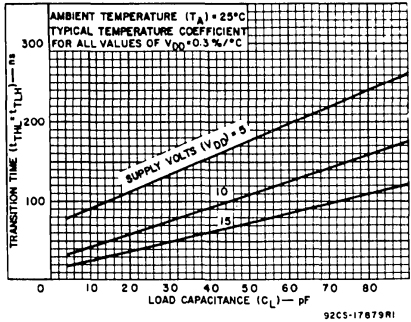


Fig. 11 - Typical transition time vs.  $C_L$  for carry output.

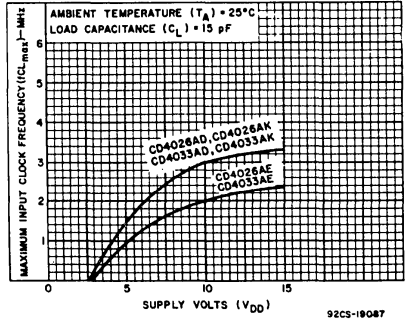


Fig. 12 - Maximum input clock frequency vs.  $V_{DD}$ .

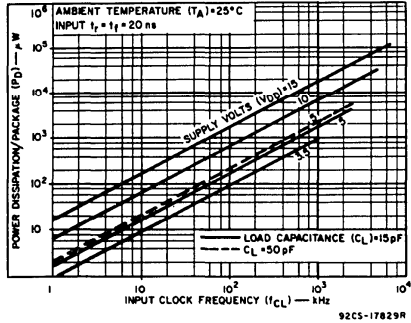


Fig. 13 - Typical dissipation characteristics.

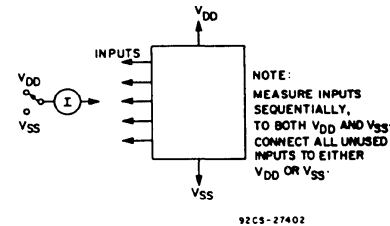


Fig. 16 - Input leakage current test circuit.