December 2012

FL103
Primary-Side-Regulation PWM Controller for LED Illumination

Features

- Low Standby Power: < 30 mW
- High-Voltage Startup
- Few External Component Counts
- Constant-Voltage (CV) and Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Green-Mode: Linearly-Decreasing PWM Frequency
- Fixed PWM Frequency at 50 kHz and 33 kHz with Frequency Hopping to Solve EMI Problems
- Peak-Current-Mode Control in CV Mode
- Cycle-by-Cycle Current Limiting
- V_{DD} Over-Voltage Protection (OVP)
- V_{DD} Under-Voltage Lockout (UVLO)
- Adjustable Brownout Detector
- Gate Output Maximum Voltage Clamped at 15 V
- Thermal Shutdown (TSD) Protection
- Available in the 8-Lead SOIC Package
- Application Voltage Range: 80 V_{AC} ~ 308 V_{AC}

Applications

- LED Illumination
- Battery chargers for cellular phones, cordless phones, PDA, digital cameras, power tools

Description

This third-generation Primary-Side-Regulation (PSR) and highly integrated PWM controller provides features to enhance the performance of LED illumination.

The proprietary topology, TRUECURRENT®, enables precise CC regulation and simplified circuit for LED illumination applications. The result is lower-cost and smaller LED lighting compared to a conventional design or a linear transformer.

To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease PWM frequency under light-load conditions. Green mode assists the power supply in meeting the power conservation requirements.

By using the FL103, LED illumination can be implemented with few external components and minimized cost.

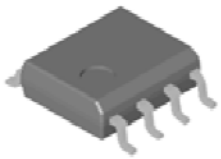


Figure 1. 8-Lead SOIC

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FL103M	-40°C to +125°C	FL103	8-Lead, Small-Outline Package (SOIC-8)	Tape & Reel

Application Diagram

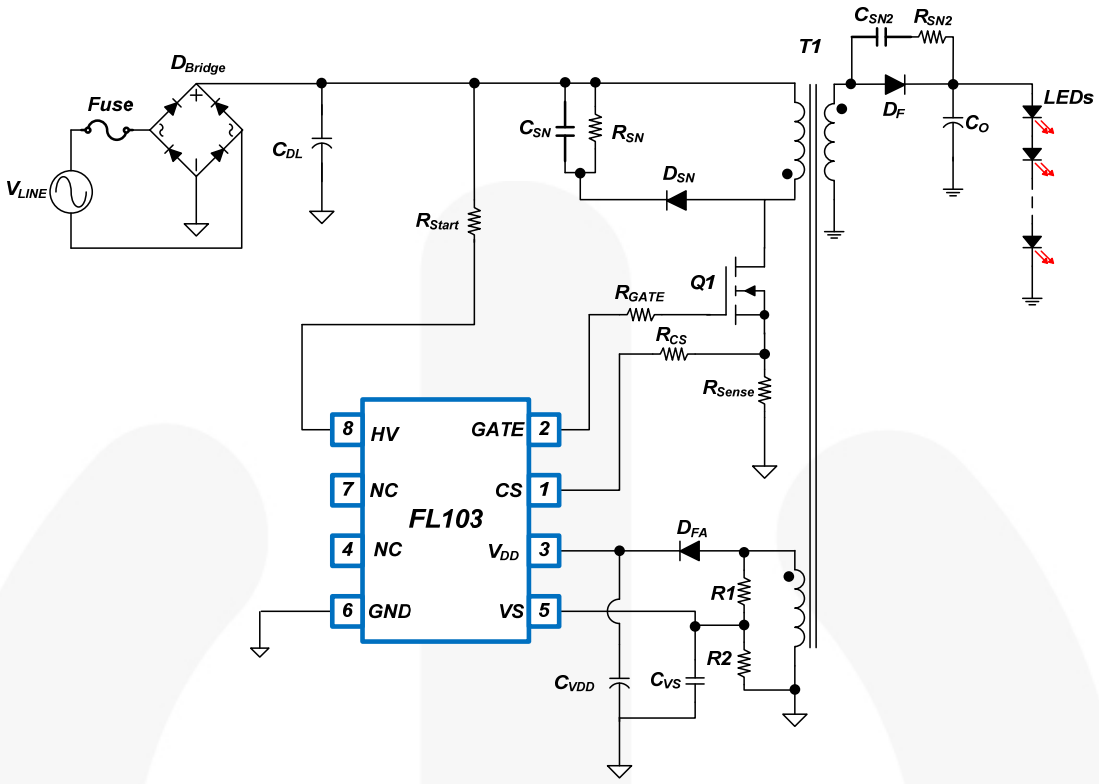


Figure 2. Typical Application

Block Diagram

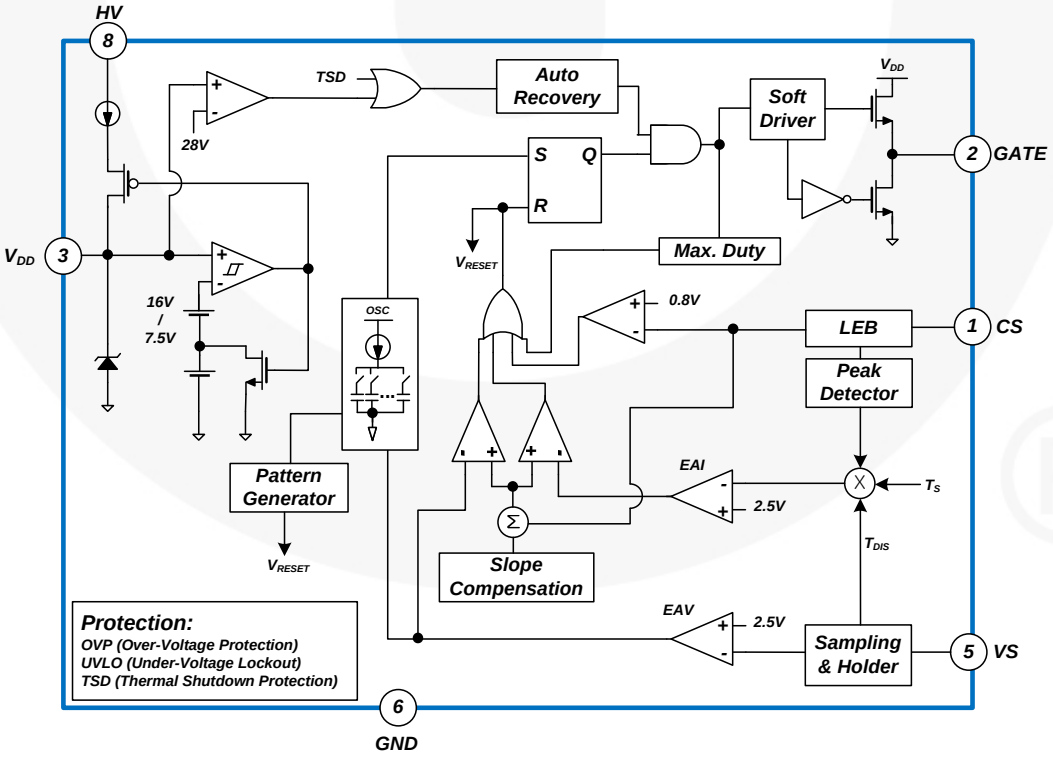
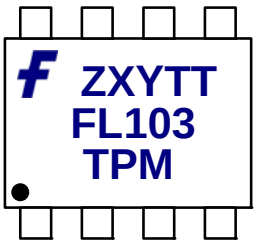


Figure 3. Internal Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: 1-Digit Year Code
Y: 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (M=SOP)
P: Y=Green Package
M: Manufacture Flow Code

Figure 4. Top Mark

Pin Configuration

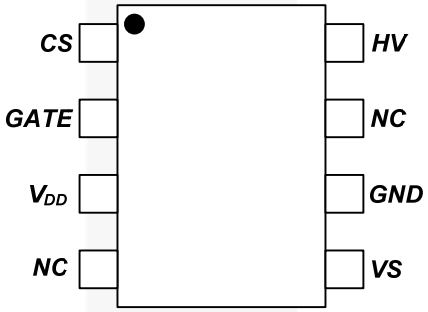


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current-sense resistor to detect the MOSFET current for peak-current-mode control in CV Mode and provides the output-current regulation in CC Mode.
2	GATE	**PWM Signal Output**. This pin uses the internal totem-pole output driver to drive the power MOSFET. It is internally clamped below 15 V.
3	V_{DD}	**Power Supply**. IC operating current and MOSFET driving current are supplied using this pin. This pin is connected to an external V_{DD} capacitor of typically 10 µF. The threshold voltages for startup and turn-off are 16 V and 7.5 V, respectively. The operating current is lower than 5 mA.
4	NC	**No Connect**. This pin is connected to GND or no connection. Does not connect any voltage source.
5	VS	**Voltage Sense**. This pin detects the output voltage information and discharge time based on voltage of auxiliary winding.
6	GND	**Ground**
7	NC	**No Connect**
8	HV	**High Voltage**. This pin connects to DC link capacitor for high-voltage startup. This pin is connected to an external startup resistor of typically 100 kΩ.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage[1]			30	V
V_{VS}	VS Pin Input Voltage		-0.3	7.0	V
V_{CS}	CS Pin Input Voltage		-0.3	7.0	V
P_D	Power Dissipation (T_A < 50°C)			660	mW
θ_{JA}	Thermal Resistance, (Junction-to-Air)			+150	°C/W
θ_{JC}	Thermal Resistance, (Junction-to-Case)			39	°C/W
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD[2]	Electrostatic Discharge Capability	Human Body Model (Except HV Pin), JEDEC-JESD22_A114		4.50	kV
		Charged Device Model (Except HV Pin), JEDEC-ESD22_C101		1.25	

Note:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. All Pins: HBM =1500 V, CDM =750 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Continuous Operating Voltage			25	V
T_A	Operation Ambient Temperature	-40		+125	°C

Electrical Characteristics

Unless otherwise specified, V_{DD} = 15 V and T_A = 25°C.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Section							
V_{DD-ON}	Turn-On Threshold Voltage			15	16	17	V
V_{DD-OFF}	Turn-Off Threshold Voltage			7.0	7.5	8.0	V
I_{DD-OP}	Operating Current				3.2	5.0	mA
$I_{DD-GREEN}$	Green Mode Operating Supply Current				0.95	1.20	mA
V_{DD-OVP}	V_{DD} Over-Voltage Protection Level			27	28	29	V
$t_{D-VDDOVP}$	V_{DD} OVP Debounce Time			90	200	350	µs
High Voltage (HV) Section							
V_{HV-MIN}	Minimum Startup Voltage on HV Pin					50	V
I_{HV}	Supply Current Drawn from Pin HV		V_{DL}=100 V	1.5	2.0	5.0	mA
I_{HV-LC}	Leakage Current after Startup		HV=500 V, V_{DD}=V_{DD-OFF} +1 V		0.5	3.0	µA
Oscillator Section							
f_{OSC}	Normal Frequency	Center Frequency	> V_O * 0.5	47	50	53	kHz
		Frequency Hopping Range		±1.5	±2.0	±2.5	
	Protection Frequency(3)	Center Frequency	< V_O * 0.5		33		
		Frequency Hopping Range			±1.3		
$V_{F-JUM-53}$	Frequency Jumping Point		50 kHz → 33 kHz, VS	1.05	1.25	1.55	V
$V_{F-JUM-35}$			33 kHz → 50 kHz, VS	1.28	1.50	1.75	V
$f_{OSC-N-MIN}$	Minimum Frequency at No-Load			300	450	600	Hz
$f_{OSC-CM-MIN}$	Minimum Frequency at CCM			7	12	17	kHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation		V_{DD}=10 V to 25 V		1	2	%
f_{DT}	Frequency Variation vs. Temperature Deviation		T_A=-40°C to +105°C			15	%
Voltage Sense (V_S) Section							
V_R	Reference Voltage for Error AMPs			2.475	2.500	2.525	V
V_N	Green-Mode Starting Voltage on EAV		f_{OSC}=2 kHz		2.5		V
V_G	Green-Mode Ending Voltage on EAV(3)		f_{OSC}=1 kHz		0.5		V
$V_{BIAS-COMV}$	Adaptive Bias Voltage Dominated by V_{COMV}		R_{VS}=20 kΩ		1.4		V
I_{tc}	IC Bias Current			7.3	10.0	12.7	µA
I_{VS-BO}	Brownout Detection Current(3)				175		µA
I_{VS-MIN}	Minimum VS Current(3)		90 V_{AC}, Heavy Load		227		µA
I_{VS-MAX}	Maximum VS Current(3)		264 V_{AC}, No Load		721		µA
t_{DIS_MIN}	Minimum Discharging Time	Normal Operation(3)	f_{OSC}=50 kHz		0.65		µs
		Protection Area	f_{OSC}=33 kHz	2.0	2.6	4.0	

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise specified, V_{DD} = 15 V and T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Current Sense (CS) Section						
t_{PD}	Propagation Delay to GATE Output			90	200	ns
t_{MIN-N}	Minimum On Time at No-Load	V_{COMR}=1 V	800	975	1150	ns
V_{TH}	Threshold Voltage for Current Limit		0.75	0.80	0.85	V
V_{TL}	Threshold Voltage on VS Pin Smaller than 0.5 V			0.25		V
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		60	75	85	%
V_{OL}	Output Voltage Low	V_{DD}=20 V, Gate Sinks 10 mA			1.5	V
V_{OH}	Output Voltage High	V_{DD}=8 V, Gate Sources 1 mA	5			V
t_r	Rising Time	C_L=1 nF		200	250	ns
t_f	Falling Time	C_L=1 nF		60	100	ns
V_{CLAMP}	Output Clamp Voltage	V_{DD}=25 V		15	18	V
Thermal Shutdown (TSD) Section						
TSD	Thermal Shutdown Temperature[3]		+140			°C
TSD_{HYS}	Thermal Shutdown Hysteresis[3]			+15		°C

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

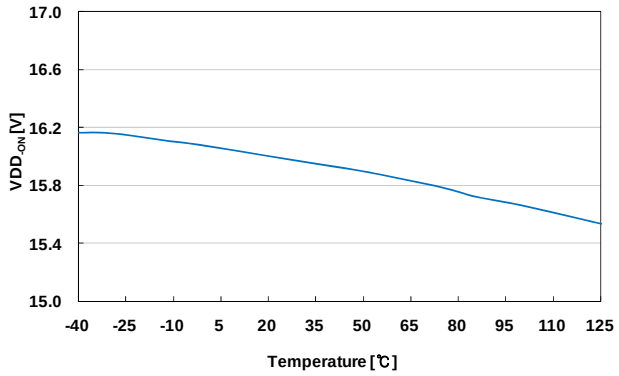


Figure 6. V_{DD-ON} vs. Temperature

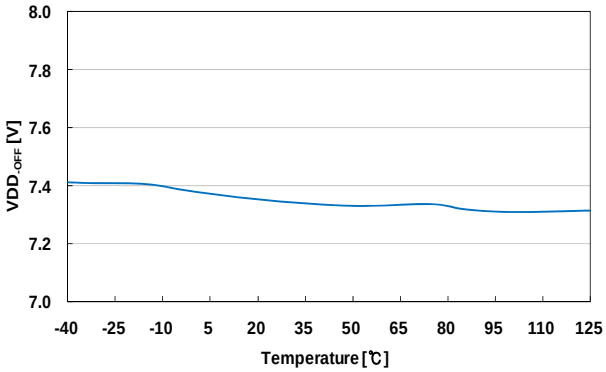


Figure 7. V_{DD-OFF} vs. Temperature

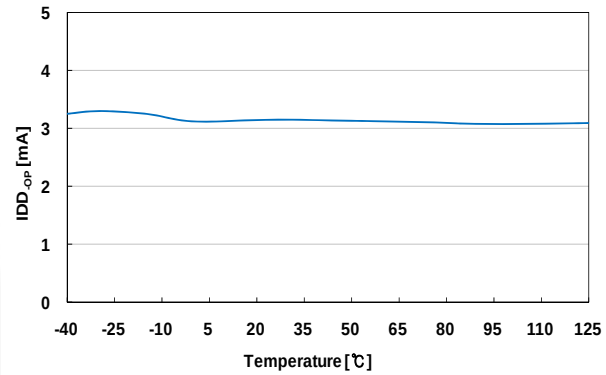


Figure 8. I_{DD-OP} vs. Temperature

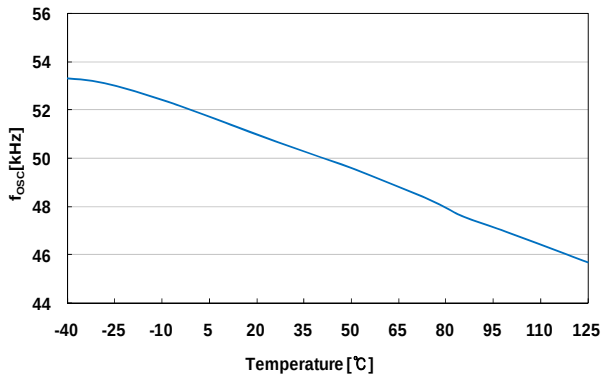


Figure 9. f_{OSC} vs. Temperature

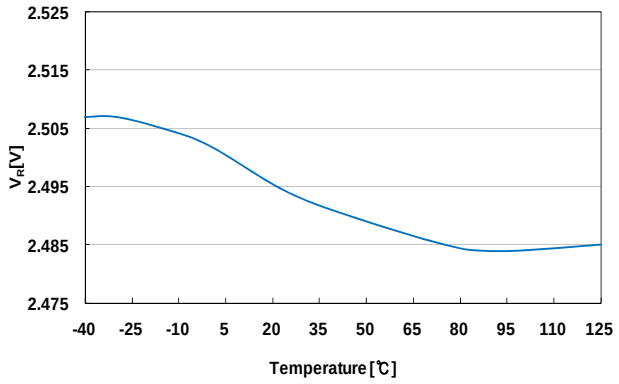


Figure 10. V_R vs. Temperature

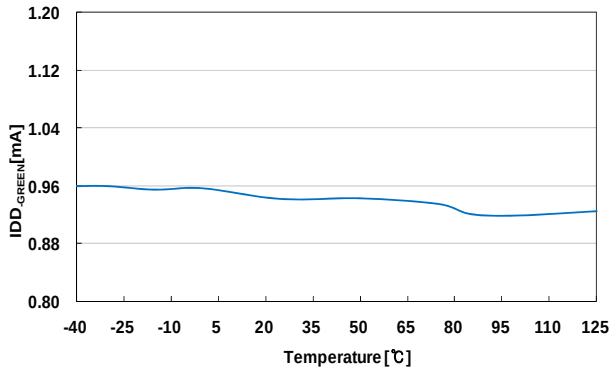


Figure 11. $I_{DD-GREEN}$ vs. Temperature

Typical Performance Characteristics (Continued)

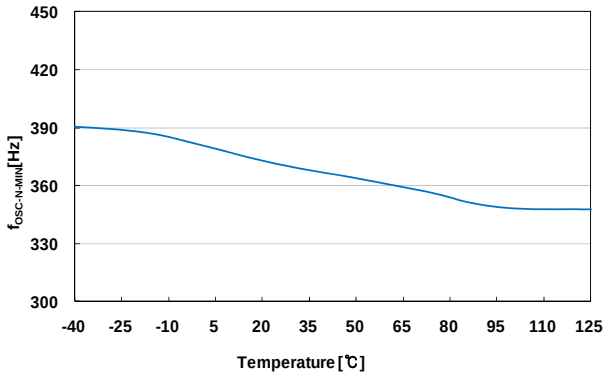


Figure 12. $f_{OSC-N-MIN}$ vs. Temperature

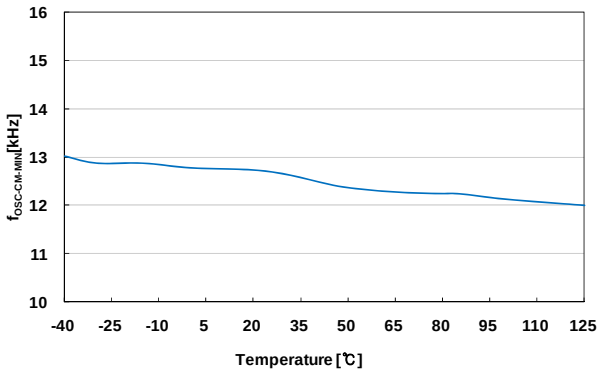


Figure 13. $f_{OSC-CM-MIN}$ vs. Temperature

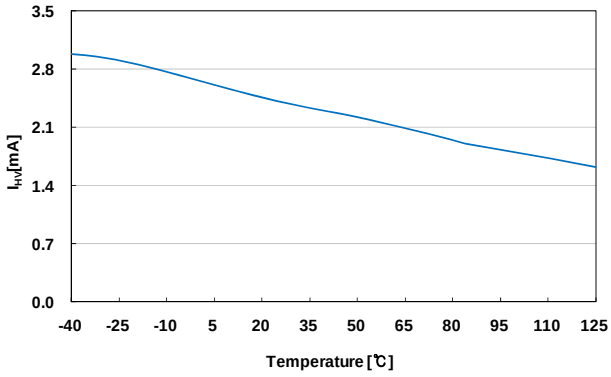


Figure 14. I_{HV} vs. Temperature

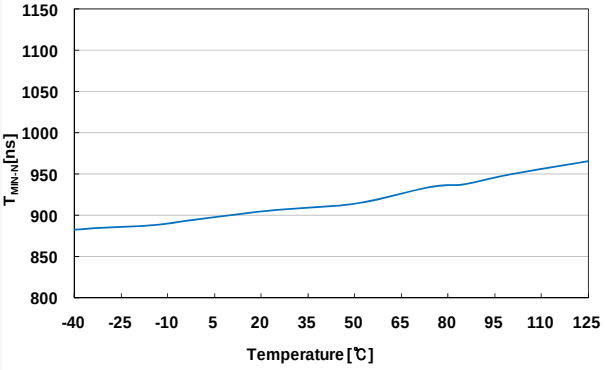


Figure 15. t_{MIN-N} vs. Temperature

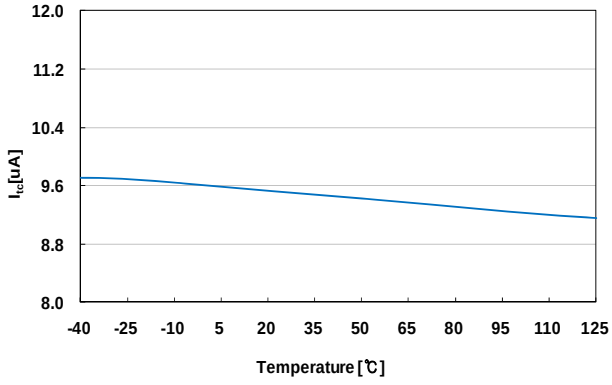


Figure 16. I_{tc} vs. Temperature

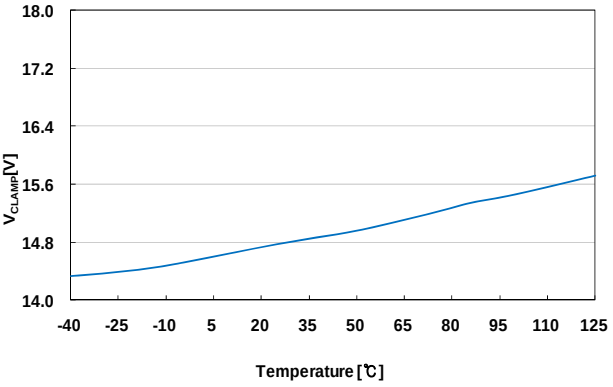


Figure 17. V_{CLAMP} vs. Temperature

Typical Performance Characteristics (Continued)

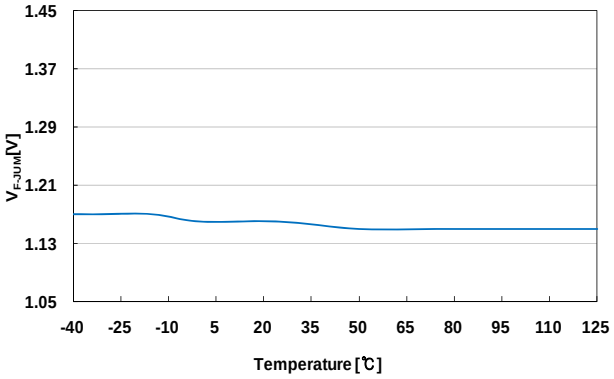


Figure 18. V_{F-JUM} vs. Temperature

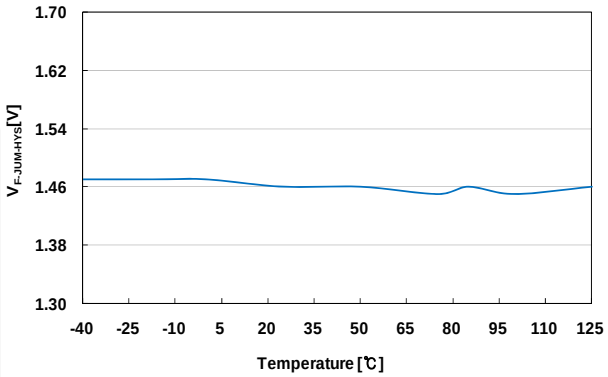


Figure 19. $V_{F-JUM-HYS}$ vs. Temperature

Functional Description

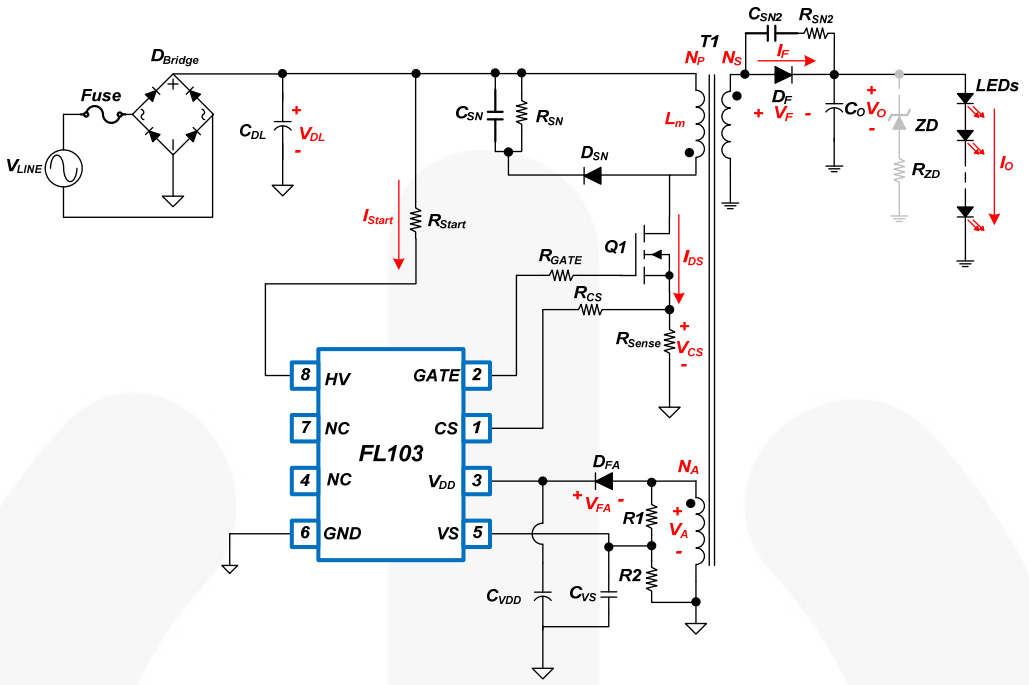


Figure 20. Basic Circuit of a PSR Flyback Converter for LED Illumination

Figure 20 shows the basic circuit diagram of a primary-side regulated flyback converter with typical waveforms shown in Figure 21. Generally, Discontinuous Conduction Mode (DCM) operation is preferred for primary-side regulation since it allows better output regulation.

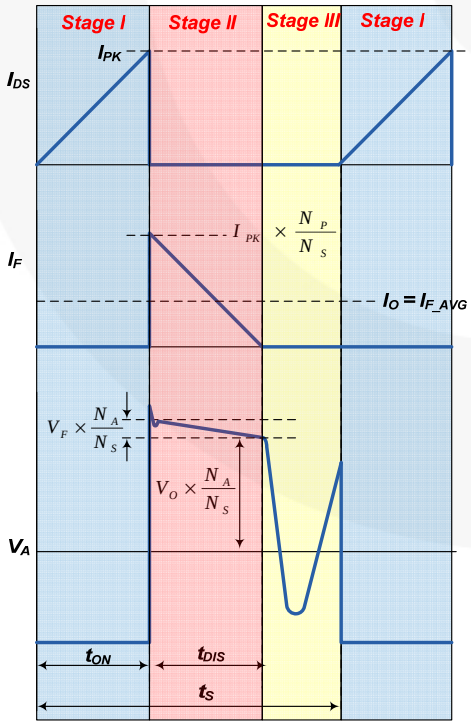


Figure 21. Waveforms of DCM Flyback Converter

The operation principles of DCM flyback converter are as follows:

Stage I

During the MOSFET on time (t_{ON}), input voltage (V_{DC}) is applied across the primary-side inductor (L_m). Then MOSFET current (I_{DS}) increases linearly from zero to the peak value (I_{PK}). During this time, the energy is drawn from the input and stored in the inductor.

Stage II

When the MOSFET (Q1) is turned off, the energy stored in the inductor forces the rectifier diode (D_F) to be turned on. While the diode is conducting, the output voltage (V_O), together with diode forward-voltage drop (V_F), is applied across the secondary-side inductor and the diode current (I_F) decreases linearly from the peak value ($I_{PK} \times N_P/N_S$) to zero. At the end of inductor current discharge time (t_{DIS}), all the energy stored in the inductor has been delivered to the output.

Stage III

When the diode current reaches zero, the transformer auxiliary winding voltage (V_A) begins to oscillate by the resonance between the primary-side inductor (L_m) and the effective capacitor loaded across MOSFET (Q1).

Constant Voltage Regulation

During the inductor current discharge time (t_{DIS}), the sum of output voltage (V_O) and diode forward-voltage drop (V_F) is reflected to the auxiliary winding side as $(V_O+V_F) \times N_A/N_S$. Since the diode forward-voltage drop (V_F) decreases as current decreases, the auxiliary winding voltage (V_A) reflects the output voltage (V_O) at the end of diode conduction time (t_{DIS}), where the diode current (I_F) diminishes to zero. By sampling the winding

voltage at the end of the diode conduction time (t_{DIS}), the output voltage (V_O) information can be obtained. The internal error amplifier for output voltage regulation (*EAV*) compares the sampled voltage with an internal precise reference to generate error voltage (V_{COMV}), which determines the duty cycle of the MOSFET (*Q1*) in Constant Voltage Mode.

Constant Current Regulation

The output current (I_O) can be estimated using the peak drain current (I_{PK}) and inductor current discharge time (t_{DIS}) since output current (I_O) is same as the average of the diode current (I_{F_AVG}) in steady state. The output current estimator (I_O *Estimator*) determines the peak value of the drain current with a peak detection circuit and calculates the output current (I_O) using the inductor discharge time (t_{DIS}) and switching period (t_S). This output information is compared with an internal precise reference to generate error voltage (V_{COMI}), which determines the duty cycle of the MOSFET (*Q1*) in Constant Current Mode. With Fairchild's innovative technique TRUECURRENT®, constant current output can be precisely controlled.

Voltage and Current Error Amplifier

Of the two error voltages, V_{COMV} and V_{COMI}, the small one determines the duty cycle. Therefore, during Constant Voltage Regulation Mode, V_{COMV} determines the duty cycle while V_{COMI} is saturated to HIGH. During Constant Current Regulation Mode, V_{COMI} determines the duty cycle while V_{COMV} is saturated to HIGH.

Operating Current

The operating current is typically 3.2 mA. The small operating current results in higher efficiency and reduces the V_{DD} capacitor (C_{VDD}) requirement. Once FL103 enters Green Mode, the operating current is reduced to 0.95 mA, assisting the power supply in meeting power conservation requirements.

Green Mode Operation

The FL103 uses voltage regulation error amplifier output (V_{COMV}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 22. The switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is fixed at 50 kHz. Once V_{COMV} decreases below 2.5 V, the PWM frequency linearly decreases from 50 kHz. When FL103 enters into green load, the PWM frequency is reduced to a minimum frequency of 370 Hz., gaining power saving power to help meet international power conservation requirements.

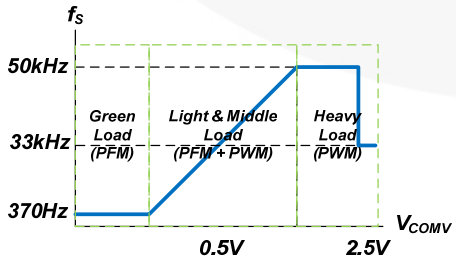


Figure 22. Switching Frequency as Output Load

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. FL103 has an internal frequency hopping circuit that changes the switching frequency between 47 kHz and 53 kHz.

High-Voltage Startup

Figure 23 shows the startup block. The HV pin is connected to the line input or DC link capacitor (C_{DC}). During startup, the internal startup circuit is enabled. Meanwhile, line input supplies the current (I_{Start}) to charge the V_{DD} capacitor (C_{VDD}). When the V_{DD} voltage reaches $V_{DD\text{-}ON}$ (16 V) and V_{DC} is enough high to avoid brownout, the internal startup circuit is disabled, blocking I_{Start} from flowing into the HV pin. Once the IC turns on, C_{VDD} is the only energy source to supply the IC consumption current before the PWM starts to switch. Thus, C_{VDD} must be large enough to prevent $V_{DD\text{-}OFF}$ (7.5 V) before the power can be delivered from the auxiliary winding. To avoid the surge from input source, the R_{Start} is connected between C_{DC} and HV, with a recommended value of 100 kΩ.

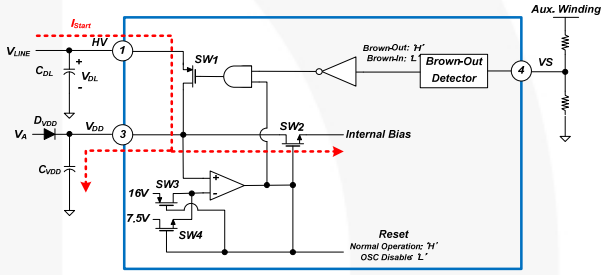


Figure 23. Startup Block

Protections

The FL103 has several self-protection functions; over-voltage protection, thermal shutdown protection, brownout protection, and pulse-by-pulse current limit.

V_{DD} Under-Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16 V and 7.5 V, respectively. During startup, the V_{DD} capacitor (C_{VDD}) must be charged to 16 V. The V_{DD} capacitor (C_{VDD}) continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} is not allowed to drop below 7.5 V during this startup process. This UVLO hysteresis window ensures that V_{DD} capacitor (C_{VDD}) properly supplies V_{DD} during startup.

V_{DD} Over-Voltage Protection (OVP)

The OVP prevents damage from over-voltage conditions. If the V_{DD} voltage exceeds 28 V at open-loop feedback condition, the OVP is triggered and the PWM switching is disabled. The OVP has a debounce time (typically 200 µs) to prevent false triggering due to switching noises.

Thermal Shutdown Protection (TSD)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C. There is a hysteresis of 15°C.

Pulse-by-Pulse Current Limit

When the current sensing voltage (V_{CS}) across the current-sense resistor (R_{Sense}) of MOSFET (Q1) exceeds the internal threshold of 0.8 V, the MOSFET (Q1) is turned off for the remainder of switching cycle. In normal operation, the pulse-by-pulse current limit is not triggered because the peak current is limited by the control loop.

Leading-Edge Blanking (LEB)

Each time the power MOSFET (Q1) switches on, a turn-on spike occurs at the sense resistor (R_{Sense}). To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. Conventional RC filtering can be omitted. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Gate Output

The FL103 output stage is a fast totem-pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 15 V Zener diode to protect power MOSFET transistors against undesired over-voltage gate signals.

Built-in Slope Compensation

The sensed voltage across the current-sense resistor is used for Current Mode control and pulse-by-pulse current limiting. Built-in slope compensation improves stability and prevents sub-harmonic oscillations due to peak-current mode control. The FL103 has a synchronized, positive-slope ramp built-in at each switching cycle.

Noise Immunity

Noise from the current sense or the control signal can cause significant pulse-width jitter, particularly in Continuous-Conduction Mode. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoiding long PCB traces and component leads, locating compensation and filter components near the FL103, and increasing the power MOSFET gate resistance are advised.

Operation Area

Figure 24 shows operation area. FL103 has two switching frequency (f_S) in Constant Current Mode. One is 50 kHz. In this case, FL103 can be operated with best condition for LED illumination. The output voltage range is between normal output voltage (V_O^N) and 50% of normal output voltage (V_O^N). The other is 33 kHz. When the output voltage is dropped, by increased load and decreasing the number of LEDs, the output voltage (V_O) drops under 50% of normal voltage (V_O^N). At that time, V_{DD} drops to near UVLO protection and triggers protection. To avoid 33 kHz, V_O^N should be designed with enough margin.

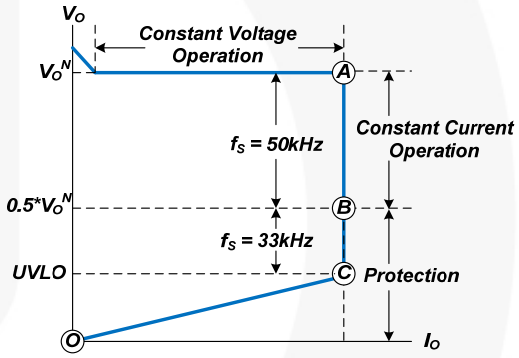
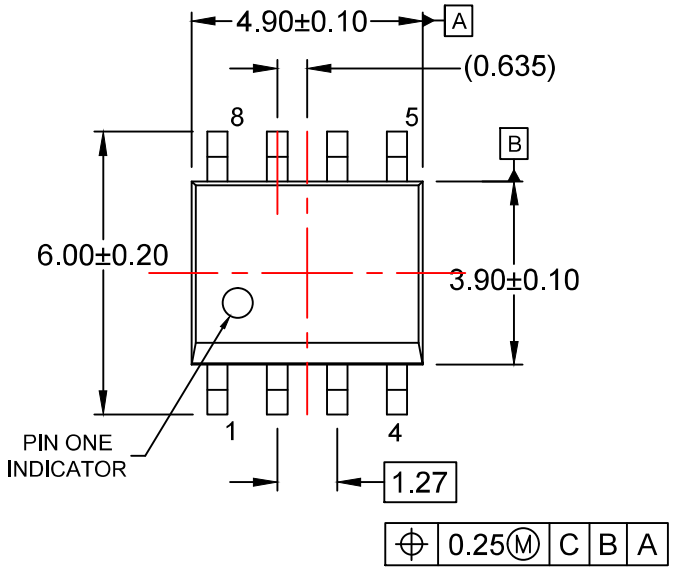
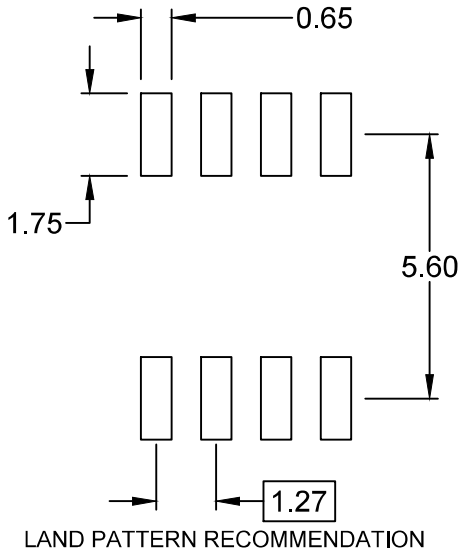
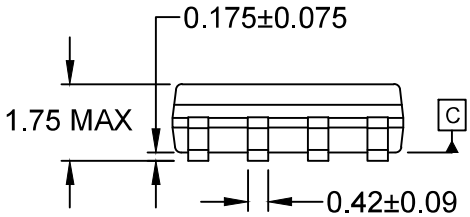


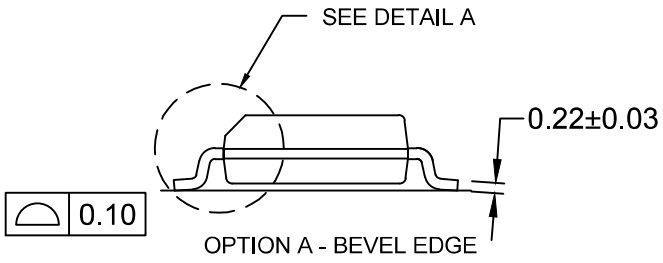
Figure 24. Operation Area



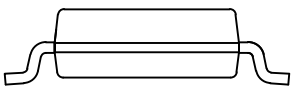


LAND PATTERN RECOMMENDATION

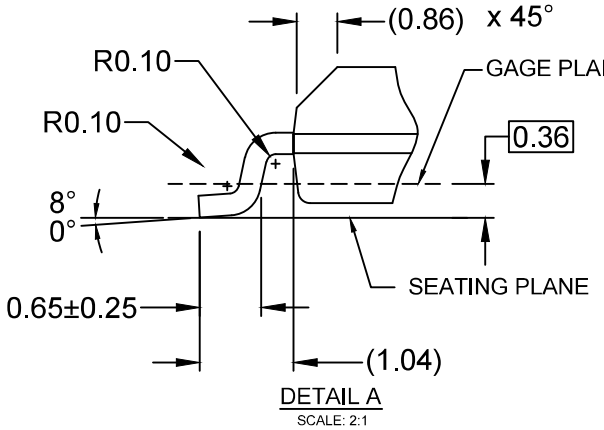




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
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E) DRAWING FILENAME: M08Arev16

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