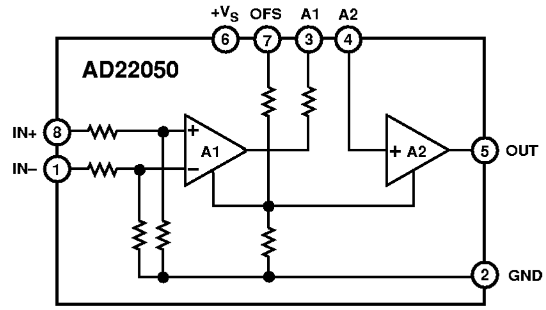
# Single-Supply Sensor Interface Amplifier

# AD22050

**FEATURES**
- Gain of ×20. Alterable from ×1 to ×160
- Input CMR from Below Ground to 6× ($V_S$ – 1 V)
- Output Span 20 mV to ($V_S$ – 0.2) V
- 1-, 2-, 3-Pole Low-Pass Filtering Available
- Accurate Midscale Offset Capability
- Differential Input Resistance 400 kΩ
- Drives 1 kΩ Load to +4 V Using $V_S$ = +5 V
- Supply Voltage: +3.0 V to +36 V
- Transient Spike Protection & RFI Filters Included
- Peak Input Voltage (40 ms): 60 V
- Reversed Supply Protection: –34 V
- Operating Temperature Range: –40°C to +125°C

**APPLICATIONS**
- Current Sensing
- Motor Control
- Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

**FUNCTIONAL BLOCK DIAGRAM**




## GENERAL DESCRIPTION

The AD22050 is a single-supply difference amplifier for amplifying and low-pass filtering small differential voltages (typically 100 mV FS at a gain of 40) from sources having a large common-mode voltage.

Supply voltages from +3.0 V to +36 V can be used. The input common-mode range extends from below ground to +24 V using a +5 V supply with excellent rejection of this common-mode voltage. This is achieved by the use of a special resistive attenuator at the input, laser trimmed to a very high differential balance.

Provisions are included for optional low-pass filtering and gain adjustment. An accurate midscale offset feature allows bipolar signals to be amplified.

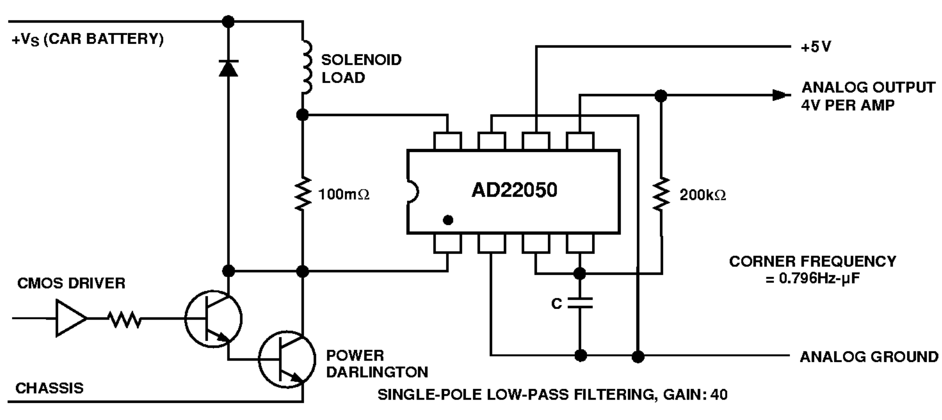



*Figure 1. Typical Application Circuit for a Current Sensor Interface*

REV. B



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## AD22050–SPECIFICATIONS ($T_A$ = +25°C, $V_S$ = +5 V, and $V_{CM}$ = 0, $R_L$ = 10 kΩ unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| INPUTS (Pins 1 and 8) | | | | | | |
| +CMR | Positive Common-Mode Range | $T_A = T_{MIN}$ to $T_{MAX}$ | | | +24 | V |
| –CMR | Negative Common-Mode Range | $T_A = T_{MIN}$ to +85°C | –1.0 | | | V |
| $CMRR_{LF}$ | Common-Mode Rejection Ratio | f ≤ 10 Hz | **80** | 90 | | dB |
| $CMRR_{HF}$ | Common-Mode Rejection Ratio | f = 10 kHz | **60** | 75 | | dB |
| $R_{INCM}$ | Common-Mode Input Resistances | Pin 1 or Pin 8 to Pin 2 | 180 | 240 | 300 | kΩ |
| $R_{MATCH}$ | Matching of Resistances | | | ±0.5 | | % |
| $R_{INDIFF}$ | Differential Input Resistance | Pin 1 to Pin 8 | 280 | 400 | | kΩ |
| PREAMPLIFIER | | | | | | |
| $G_{CL}$ | Closed-Loop Gain[1] | | 9.7 | 10.0 | 10.3 | |
| $V_O$ | Output Voltage Range (Pin 3) | | +0.01 | | +4.8 | V |
| $R_O$ | Output Resistance[2] | | **97** | 100 | **103** | kΩ |
| OUTPUT BUFFER | | | | | | |
| $G_{CL}$ | Closed-Loop Gain[1] | $R_{LOAD}$ ≥ 10 kΩ | **1.94** | 2.0 | **2.06** | |
| $V_O$ | Output Voltage Range[3] | $T_A = T_{MIN}$ to $T_{MAX}$ | **+0.02** | | **+4.8** | V |
| $R_O$ | Output Resistance (Pin 5) | $V_O$ ≥ 0.1 V dc, $I_O$ < 1 mA | | 2.0 | | Ω |
| OVERALL SYSTEM | | | | | | |
| G | Gain[1] | $V_O$ ≥ 0.1 V dc | **19.9** | 20.0 | **20.1** | |
| | Over Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | 19.8 | | 20.2 | |
| $V_{OS}$ | Input Offset Voltage[4] | | **–1** | 0.03 | **1** | mV |
| | Over Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | –3 | | 3 | mV |
| OFS | Midscale Offset (Pin 7) Scaling | | **0.49** | 0.50 | **0.51** | V/V |
| | Input Resistance | Pin 7 to Pin 2 | 14 | 20 | 26.5 | kΩ |
| $I_{OSC}$ | Short-Circuit Output Current | $T_A = T_{MIN}$ to $T_{MAX}$ | 7 | 11 | 25 | mA |
| $BW_{-3\,dB}$ | –3 dB Bandwidth | $V_O$ = +1 V dc | | 30 | | kHz |
| SR | Slew Rate | | | 0.2 | | V/µs |
| $N_{SD}$ | Noise Spectral Density[3] | f = 100 Hz to 10 kHz | | 0.2 | | µV/√Hz |
| POWER SUPPLY | | | | | | |
| $V_S$ | Operating Range | $T_A = T_{MIN}$ to $T_{MAX}$ | 3.0 | 5 | 36 | V |
| $I_S$ | Quiescent Supply Current[5] | $T_A$ = +25°C, $V_S$ = +5 V | | 200 | **500** | µA |
| TEMPERATURE RANGE | | | | | | |
| $T_{OP}$ | Operating Temperature Range | | –40 | | +125 | °C |

NOTES
[1]Specified for default mode, i.e., with no external components. The overall gain is trimmed to 0.5%, while the individual gains of A1 and A2 may be subject to a maximum ±3% tolerance. Note that the actual gain in a particular application can be modified by the use of external resistor networks.
[2]The actual output resistance of A1 is only a few ohms, but access to this output, via Pin 3, is always through the resistor R12 (see Figure 16) which is 100 kΩ, trimmed to ±3%.
[3]For $V_{CM}$ ≤ 20 V. For $V_{CM}$ > 20 V, $V_{OL}$ ≅ 1 mV/V × $V_{CM}$.
[4]Referred to the input (Pins 1 and 8).
[5]With $V_{DM}$ = 0 V. Differential mode signals are referred to as $V_{DM}$, while $V_{CM}$ refers to common-mode voltages– see the section Product Description and Figure 3.

All min and max specifications are guaranteed, although only those marked in **boldface** are tested on all production units at final test.
Specifications subject to change without notice.

### ORDERING GUIDE

| Model | Temperature Range | Package Option[1] |
|---|---|---|
| AD22050N | –40°C to +125°C | N-8 |
| AD22050R | –40°C to +125°C | SO-8 |
| AD22050R-Reel | –40°C to +125°C | SO-8[2] |

NOTES
[1]N = Plastic DIP Package, R = Plastic SOIC Package, R-Reel = Tape and Reel.
[2]Quantities must be in increments of 2,500 pieces each.

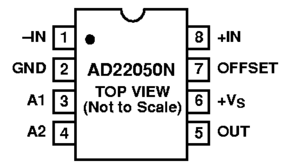
## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Supply Voltage | +3.0 V to +36 V |
| Peak Input Voltage (40 ms) | 60 V |
| $V_{OFS}$ (Pin 7 to Pin 2) | +20 V |
| Reversed Supply Voltage Protection | −34 V |
| Operating Temperature | −40°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Output Short Circuit Duration | Indefinite |
| Lead Temperature Range (Soldering 60 sec) | +300°C |

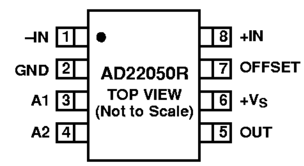
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PIN CONFIGURATIONS

**Plastic Mini-DIP Package (N-8)**




**Plastic SOIC Package (SO-8)**




## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD22050 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


## PRODUCT DESCRIPTION

The AD22050 is a single-supply difference amplifier consisting of a precision balanced attenuator, a very low drift preamplifier and an output buffer amplifier (A1 and A2, respectively, in Figure 2). It has been designed so that small differential signals ($V_{DM}$ in Figure 3) can be accurately amplified and filtered in the presence of large common-mode voltages ($V_{CM}$) without the use of any other active components.

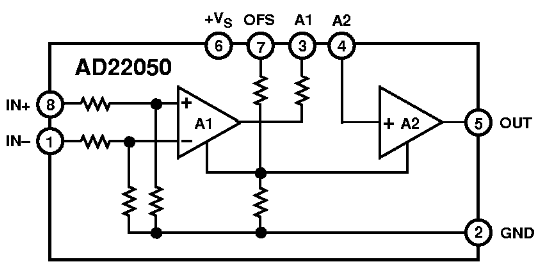



*Figure 2. Simplified Schematic*

The resistive attenuator network is situated at the input to the AD22050 (Pins 1 and 8), allowing the common-mode voltage at Pins 1 and 8 to be six times greater than that which can be tolerated by the actual input to A1. As a result, the input common-mode range extends to 6× ($V_S$ – 1V).

Two small filter capacitors (not shown in Figure 2) have been included at the inputs of A1 to minimize the effects of any spurious RF signals present in the signal.

Internal feedback around A1 sets the closed-loop gain of the preamplifier to ×10 from the input pins; the output of A1 is connected to Pin 3 via a 100 kΩ resistor, which is trimmed to ±3% (R12 in Figure 2) to facilitate the low-pass filtering of the signal of interest (see Low-Pass Filtering section). The inclusion of an additional resistive network allows the output of A1 to be offset to an optional voltage of one half of that supplied to Pin 7; in many cases this offset would be $+V_S/2$ by tying Pin 7 to $+V_S$ (Pin 6), permitting the conditioning and processing of bipolar signals (see Strain Gage Interface section).

The output buffer A2 has a gain of ×2, setting the precalibrated, overall gain of the AD22050, with no external components, to ×20. (This gain is easily user-configurable– see Altering the Gain section for details.)

The dynamic properties of the AD22050 are optimized for interfacing to transducers; in particular, current sensing shunt resistors. Its rejection of large, high frequency, common-mode signals makes it superior to that of many alternative approaches. This is due to the very careful design of the input attenuator and the close integration of this highly balanced, high impedance system with the preamplifier.

## APPLICATIONS

The AD22050 can be used wherever a high gain, single-supply differencing amplifier is required, and where a finite input resistance (240 kΩ to ground, 400 kΩ between differential inputs) can be tolerated. In particular, the ability to handle a common-mode input considerably larger than the supply voltage is frequently of value.

Also, the output can run down to within 20 mV of ground, provided it is not called on to sink any load current. Finally, the output can be offset to half of a full-scale reference voltage (with a tolerance of ±2%) to allow a bipolar input signal.

## ALTERING THE GAIN

The gain of the preamplifier, from the attenuator input (Pins 1 and 8) to its output at Pin 3, is ×10 and that of the output buffer, from Pin 4 to Pin 5, is ×2, thus making the overall default gain ×20. The overall gain is accurately trimmed (to within ±0.5%). In some cases, it may be desirable to provide for some variation in the gain; for example, in absorbing the scaling error of a transducer.

Figure 3 shows a general method for trimming the gain, either upward or downward, by an amount dependent on the resistor, R. The gain range, expressed as a percentage of the overall gain, is given by (10 MΩ/R)%. Thus, the adjustment range would be ±2% for R = 5 MΩ; ±10% for R = 1 MΩ, etc.

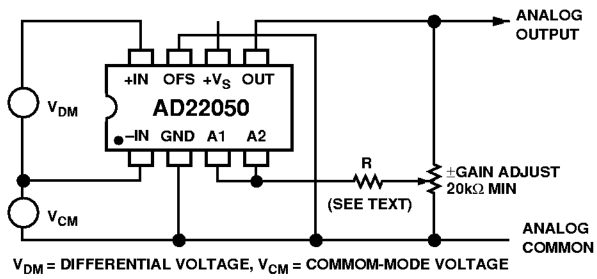



*Figure 3. Altering Gain to Accommodate Transducer Scaling Error*

In addition to the method above, another method may be used to vary the gain. Many applications will call for a gain higher than ×20, and some require a lower gain. Both of these situations are readily accommodated by the addition of one external resistor, plus an optional potentiometer if gain adjustment is required (for example, to absorb a calibration error in a transducer).

**Decreasing the Gain.** See Figure 4. Since the output of the preamplifier has an output resistance of 100 kΩ, an external resistor connected from Pin 4 to ground will precisely lower the gain by a factor R/(100k+R). When configuring the AD22050 for any gain, the maximum input and the power supply being used should be considered, since either the preamplifier or the output buffer will reach its full-scale output (approximately $V_S$ – 0.2 V) with large differential input voltages. The input of the AD22050 is limited to no greater than (V – 0.2)/10, for overall gains less than 10, since the preamplifier, with its fixed gain of ×10, reaches its full scale output before the output buffer. For $V_S$ = 5 V this is 0.48 V. For gains greater than 10, however, the swing at the buffer output reaches its full-scale first and limits the AD22050 input to ($V_S$ – 0.2)/G, where G is the overall gain. Increasing the power supply voltage increases the allowable maximum input. For $V_S$ = 5 V and a nominal gain of 20, the maximum input is 240 mV.

The overall bandwidth is unaffected by changes in gain using this method, although there may be a small offset voltage due to the imbalance in source resistances at the input to A2. In many cases this can be ignored but, if desired, can be nulled by inserting a resistor in series with Pin 4 (at "Point X" in Figure 4) of value 100 kΩ minus the parallel sum of R and 100 kΩ. For example, with R = 100 kΩ (giving a total gain of ×10), the optional offset nulling resistor is 50 kΩ.

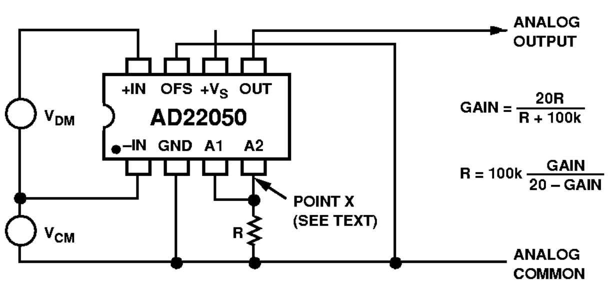



*Figure 4. Achieving Gains Less Than ×20*

**Increasing the Gain.** The gain can be raised by connecting a resistor from the output of the buffer amplifier (Pin 5) to its noninverting input (Pin 4) as shown in Figure 5. The gain is now multiplied by the factor R/(R–100k); for example, it is doubled for R = 200 kΩ. Overall gains of up to ×160 (R = 114 kΩ) are readily achievable in this way. Note, however, that the accuracy of the gain becomes critically dependent on resistor value at high gains. Also, the effective input offset voltage at Pins 1 and 8 (about six times the actual offset of A1) limits the part's use in very high gain, dc-coupled applications. The gain may be trimmed by using a fixed and variable resistor in series (see, for example, Figure 10).

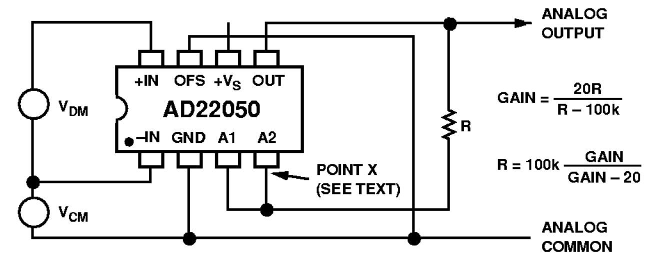



*Figure 5. Achieving Gains Greater Than ×20*

Once again, a small offset voltage will arise from an imbalance in source resistances and the finite bias currents inherently present at the input of A2. In most applications this additional offset error (about 130 µV at ×40) will be comparable with the specified offset range and will therefore introduce negligible skew. It may, however, be essentially eliminated by the addition of a resistor in series with the parallel sum of R and 100 kΩ (i.e., at "Point X" in Figure 5) so the total series resistance is maintained at 100 kΩ. For example, at a gain of ×30, when R = 300 kΩ and the parallel sum of R and 100 kΩ is 75 kΩ, the padding resistor should be 25 kΩ. A 50 kΩ pot would provide an offset range of about ±2.25 mV referred to the output, or ±75 µV referred to the attenuator input. A specific example is shown in Figure 12.

## LOW-PASS FILTERING

In many transducer applications it is necessary to filter the signal to remove spurious high frequency components, including noise, or to extract the mean value of a fluctuating signal with a peak-to-average ratio (PAR) greater than unity. For example, a full wave rectified sinusoid has a PAR of 1.57, a raised cosine has a PAR of 2 and a half wave sinusoid has a PAR of 3.14. Signals having large spikes may have PARs of 10 or more.

When implementing a filter, the PAR should be considered so the output of the AD22050 preamplifier (A1) does not clip before A2 does, since this nonlinearity would be averaged and appear as an error at the output. To avoid this error both amplifiers should be made to clip at the same time. This condition is achieved when the PAR is no greater than the gain of the second amplifier (2 for the default configuration). For example, if a PAR of 5 is expected, the gain of A2 should be increased to 5.

Low-pass filters can be implemented in several ways using the features provided by the AD22050. In the simplest case, a single-pole filter (20 dB/decade) is formed when the output of A1 is connected to the input of A2 via the internal 100 kΩ resistor by strapping Pins 3 and 4, and a capacitor added from this node to ground, as shown in Figure 6. The dc gain remains ×20, and the gain trim shown in Figure 3 may still be used. If a resistor is added across the capacitor to lower the gain, the corner frequency will increase; it should be calculated using the parallel sum of the resistor and 100 kΩ.

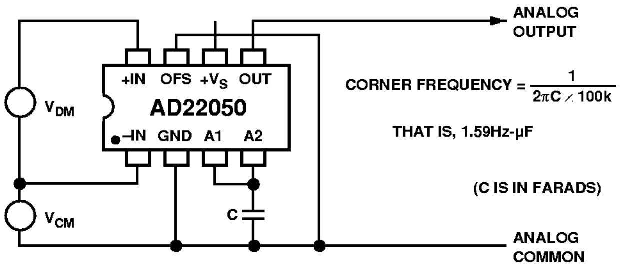



*Figure 6. Connections for Single-Pole, Low-Pass Filter*

If the gain is raised using a resistor, as shown in Figure 5, the corner frequency is lowered by the same factor as the gain is raised. Thus, using a resistor of 200 kΩ (for which the gain would be doubled) the corner frequency is now 0.796 Hz-µF, (0.039 µF for a 20 Hz corner).

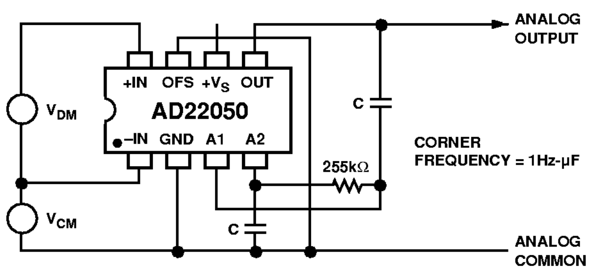



*Figure 7. Connections for Conveniently Scaled, Two-Pole, Low-Pass Filter*

A two-pole filter (with a roll-off of 40 dB/decade) can be implemented using the connections shown in Figure 7. This is a Sallen & Key form based on a ×2 amplifier. It is useful to remember that a two-pole filter with a corner frequency $f_2$ and a one-pole filter with a corner at $f_1$ have the same attenuation at the frequency $(f_2^2/f_1)$. The attenuation at that frequency is 40 Log$(f_2/f_1)$. This is illustrated in Figure 8. Using the standard resistor value shown, and equal capacitors (in Figure 7), the corner frequency is conveniently scaled at 1 Hz-µF (0.05 µF for a 20 Hz corner). A maximally flat response occurs when the resistor is lowered to 196 kΩ and the scaling is then 1.145 Hz-µF. The output offset is raised by about 4 mV (equivalent to 200 µV at the input pins).

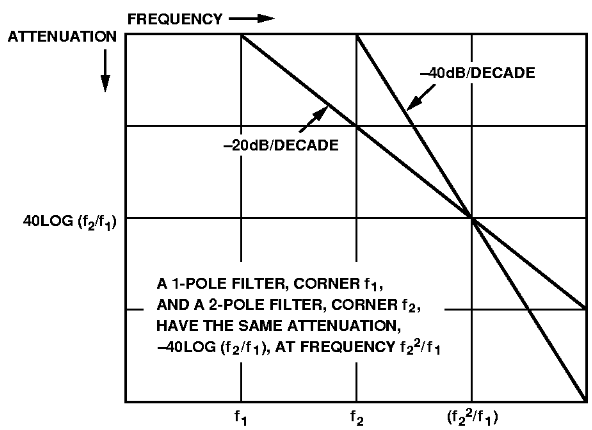



*Figure 8. Comparative Responses of One- and Two-Pole Low-Pass Filters*

A three-pole filter (with roll-off 60 dB/decade) can be formed by adding a passive RC network at the output forming a real pole. A three-pole filter with a corner frequency $f_3$ has the same attenuation a one-pole filter of corner $f_1$ has at a frequency $\sqrt{f_3^3/f_1}$, where the attenuation is 30 Log $(f_3/f_1)$ (see the graph in Figure 9). Using equal capacitor values, and a resistor of 160 kΩ, the corner-frequency calibration remains 1 Hz-µF.

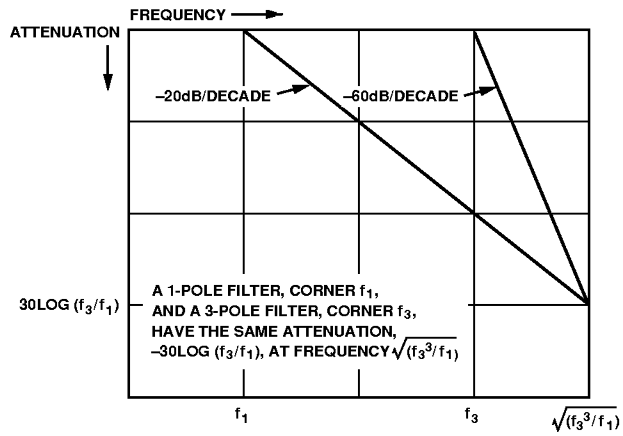



*Figure 9. Comparative Responses of One- and Three-Pole Low-Pass Filters*

## CURRENT SENSOR INTERFACE

A typical automotive application making use of the large common-mode range is shown in Figure 10.

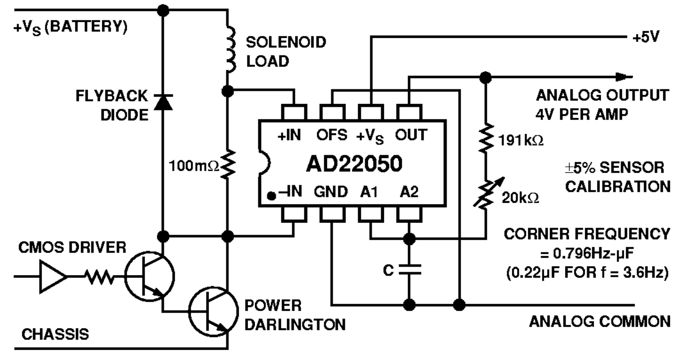



*Figure 10. Current Sensor Interface. Gain Is ×40, Single-Pole Low-Pass Filtering*

The current in a load, here shown as a solenoid, is controlled by a power transistor that is either cut off or saturated by a pulse at its base; the duty-cycle of the pulse determines the average current. This current is sensed in a small resistor. The average differential voltage across this resistor is typically 100 mV, although its peak value will be higher by an amount that depends on the inductance of the load and the control frequency. The common-mode voltage, on the other hand, extends from roughly 1V above ground, when the transistor is saturated, to about 1.5 V above the battery voltage, when the transistor is cut off and the diode conducts.

If the maximum battery voltage spikes up to +20 V, the common-mode voltage at the input can be as high as 21.5 V. This can be measured using even a +5 V supply for the AD22050.

To produce a full-scale output of +4 V, a gain ×40 is used, adjustable by ±5% to absorb the tolerance in the sense resistor. There is sufficient headroom to allow at least a 10% overrange (to +4.4 V). The roughly triangular voltage across the sense resistor is averaged by a single-pole low-pass filter, here set with a corner frequency of $f_C$ = 3.6 Hz, which provides about 30 dB of attenuation at 100 Hz. A higher rate of attenuation can be obtained by a two-pole filter having $f_C$ = 20 Hz, as shown in Figure 11. Although this circuit uses two separate capacitors, the total capacitance is less than half that needed for the single-pole filter.

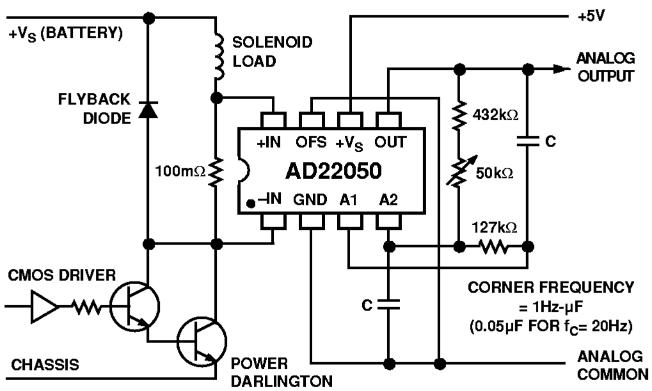



*Figure 11. Illustration of Two-Pole Low-Pass Filtering*

## STRAIN GAGE INTERFACE: MIDSCALE OFFSET FEATURE

The AD22050 can be used to interface a strain gage to a subsequent process where only a single supply voltage is available. In this application, the midscale offset feature is valuable, since the output of the bridge may have either polarity. Figure 12 shows typical connections.

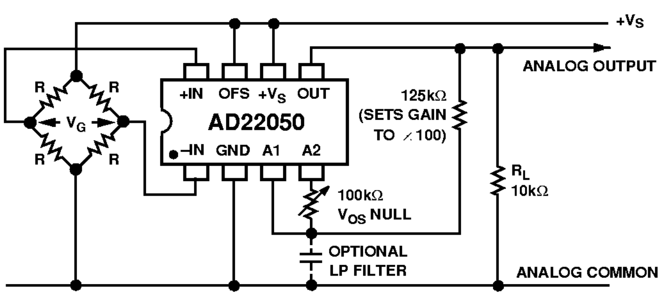



*Figure 12. Typical Connections for a Strain Gage Interface Using the Offset Feature*

The offset is obtained by connecting Pin 7 (OFS) to the supply voltage. In this way, the output of the AD22050 is centered to midway between the supply and ground. In many systems the supply will also serve as the reference voltage for a subsequent A/D converter. Alternatively, Pin 7 may be tied to the reference voltage from an independent source. The AD22050 is trimmed to guarantee an accuracy of ±2% on the 0.5 ratio between the voltage on Pin 7 and the output.

An ac excitation of up to ±2 V can also be used because the common-mode range of the AD22050 extends to –1 V. Assuming a full-scale bridge output ($V_G$) of ±10 mV, a gain of ×100 might be used to provide an output of ±1 V (a full-scale range of +1.5 V to +3.5 V). This gain is achieved using the method discussed in connection with Figure 5. Note that the gain-setting resistor does not affect the accuracy of the midscale offset. (However, if the gain were lowered, using a resistor to ground, this offset would no longer be accurate.) A $V_{OS}$ nulling pot is included for illustrative purposes. One-, two- and three-pole filtering can also be implemented, as discussed in the Low-Pass Filtering section.

### Using the Midscale Offset Feature

Figure 13 shows a more detailed schematic of the output amplifier A2. Because this is a single supply device, the output stage has no pull-down transistor. Such a transistor would limit the minimum output to several hundred millivolts above ground. When using the AD22050 in unipolar mode (Pin 7 grounded), the resistors making up the feedback network also act as a pull-down for the output stage.

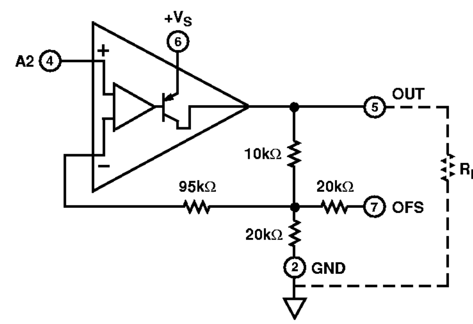



*Figure 13. Detailed Schematic of Output Amplifier A2*

If the output is called upon to source current (not sink), then it can swing almost completely to ground (within 20 mV). However, if the offset pin is connected to some positive voltage source, this source will "pull up" the output voltage, thereby limiting the minimum output swing. With no external load the minimum output voltage possible is $V_{OFS}/2$. For example, if Pin 7 is connected to +5 V, the minimum output voltage is equal to the offset voltage of 2.5 V. By adding an additional load, as shown, the output swing toward ground can be extended.

The relationship is described by:

$$V_{OUT} > \frac{1}{2} V_{OFS} \frac{R_L}{R_L + 20\,k\Omega^{*}}$$

*This 20 kΩ resistor is internal to the AD22050 and can vary by ±30%.

where $R_L$ is an externally applied load resistor. However, $R_L$ cannot be made arbitrarily small since this would require excessive current from the output. The output current should be limited to 5 mA total.

## APPLICATION HINTS

### Frequency Compensation

As are all closed-loop op amp circuits, the AD22050 is sensitive to capacitive loading at its output. However, the AD22050 is sensitive at higher output voltages due to nonlinear effects in the rail-to-rail design of the buffer amplifier (A2). In this amplifier the output stage gain increases with increasing output voltage. This behavior does not affect dc parameters such as gain accuracy or linearity; however, it can compromise ac stability. When operating from a power supply of 5 V or less (and, therefore, $V_{OUT}$ < 5 V), the AD22050 can drive capacitive loads up to 25 pF with no external components. When operating at higher supply voltages (which are associated with higher output voltages) and/or driving larger capacitive loads, an external compensation network should be used. Figure 14 shows an R-C "snubber" circuit loading the output of the AD22050.

This combination, in conjunction with the internal 20 kΩ resistance, forms a lag network. This network attenuates the open-loop gain of the amplifier at higher frequencies. The ratio of $R_{LAG}$ to the load seen by the AD22050 determines the high frequency attenuation seen by the op amp. If $R_{LAG}$ is made 1/20th of the total load resistance (≈20 kΩ‖$R_L$), then 26 dB of attenuation is obtained at higher frequencies. The capacitor ($C_{LAG}$) is used to control the frequency of the compensation network. It should be set to form a 5 µs time constant with the resistor ($R_{LAG}$). Table I shows the recommended values of $R_{LAG}$ and $C_{LAG}$ for various values of external load resistor $R_L$. Ten percent tolerance on these components is acceptable.

Alternatively, the signal may be taken from the midpoint of $R_{LAG}$–$C_{LAG}$. This output is particularly useful when driving CMOS analog-to-digital converters. For more information see the section Driving Charged Redistributed A/D Converters.

Note that when implementing this network large signal response is compromised. This occurs because there is no active pull-down and the lag capacitor must discharge through the internal feedback resistor (20 kΩ) giving a fairly long-time constant. For example if $C_{LAG}$ = 0.01 µF, the large signal negative slew characteristic is a decaying exponential with a time constant of ≈200 µs.

**Table I. Compensation Components vs. External Load Resistor**

| $R_L$ | $R_{LAG}$ | $C_{LAG}$ |
|---|---|---|
| >100 kΩ | 470 Ω | 0.01 µF |
| 50 kΩ | 390 Ω | 0.01 µF |
| 20 kΩ | 270 Ω | 0.047 µF |
| 10 kΩ | 200 Ω | 0.047 µF |
| 5 kΩ | 100 Ω | 0.1 µF |
| 2 kΩ | 47 Ω | 0.22 µF |

### Driving Charge Redistribution A/D Converters

When driving CMOS ADCs, such as those embedded in popular microcontrollers, the charge injection (ΔQ) can cause a significant deflection in the AD22050 output voltage. Though generally of short duration, this deflection may persist until after the sample period of the ADC has expired. It is due to the relatively high open-loop output impedance of the AD22050. The effect can be significantly reduced by including the same R-C network recommended for improving stability (see Frequency Compensation section). The large capacitor in the lag network helps to absorb the additional charge, effectively lowering the high frequency output impedance of the AD22050. For these applications the output signal should be taken from the midpoint of the $R_{LAG}$–$C_{LAG}$ combination as shown in Figure 15.

Since the perturbations from the analog-to-digital converter are small, the output of the AD22050 will appear to be a low impedance. The transient response will, therefore, have a time constant governed by the product of the two lag components, $C_{LAG} \times R_{LAG}$. For the values shown in Figure 15, this time constant is programmed at approximately 10 µs. Therefore, if samples are taken at several tens of microseconds or more, there will be negligible "stacking up" of the charge injections.

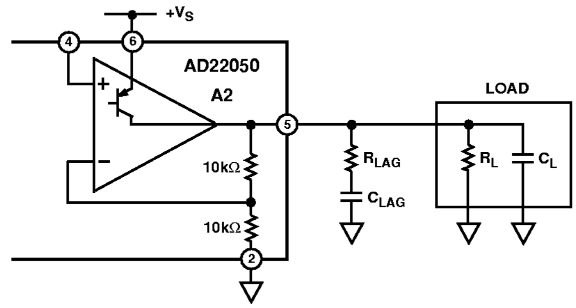



*Figure 14. Using an R-C Network for Compensation*

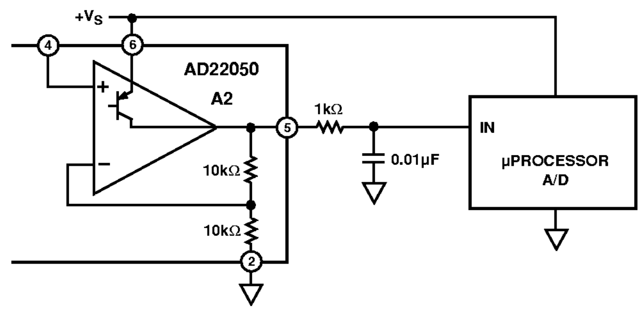



*Figure 15. Recommended Circuit for Driving CMOS A/D Converters*

## UNDERSTANDING THE AD22050

Figure 16 shows the main elements of the AD22050. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators R1 through R4, whose purpose is to reduce the common-mode voltage at the input to the preamplifier. The attenuated signal is then applied to a feedback amplifier based on the very low drift op amp, A1. The differential voltage across the inputs is accurately amplified in the presence of common-mode voltages of many times the supply voltage. The overall common-mode response is minimized by precise laser trimming of R3 and R4, giving the AD22050 a common-mode rejection ratio (CMRR) of at least 80 dB (10,000:1).

The common-mode range of A1 extends from slightly below ground to 1 V below $+V_S$ (at the minimum temperature of –40°C). Since an attenuation ratio of about 6 is used, the input common-mode range is –1 V to +24 V using a +5 V supply. Small filter capacitors C1 and C2 are included to minimize the effects of spurious RF signals at the inputs, which might cause dc errors due to the rectification effects at the input to A1. At high frequencies, even a small imbalance in these components would seriously degrade the CMRR, so a special high frequency trim is also carried out during manufacture.

A unique method of feedback around A1, provided by R9 and R7, sets the closed-loop gain of the preamplifier to ×10 (from the input pins). The feedback network is balanced by the inclusion of R6 and R8. The small value of R7 results in a more practical value for R9 (which would have to be 2 MΩ if the feedback were taken directly to the inputs of A1). R8 is not directly connected to ground, but to an optional voltage of one half that is applied to Pin 7 (OFS). It is trimmed to within close tolerances through R10 and R11. This allows the output of A1 to be offset to midscale, typically $+V_S/2$, by tying Pins 6 and 7 together. (For an example of the use of this feature, see Figure 12.) The gain is adjusted by the single resistor R5, which acts only on the differential signal. More importantly, it also results in much less feedforward of the common-mode signal to the output of A1, which, being a single-supply circuit, has no means of pulling this output down toward ground in those circumstances where the common-mode input is very positive while the net differential signal is small. (The output of A1 is the collector of a PNP transistor whose emitter is tied to $+V_S$.) R16 is specifically included to alleviate this problem.

The output of the preamplifier is connected to Pin 3 via R12, a 100 kΩ resistor that is trimmed to within ±3%. The inclusion of R12 allows a low-pass filter to be formed, with an accurate time constant, by placing a capacitor from Pin 3 to ground. By separating the connections at Pins 3 and 4, a two-pole Sallen and Key filter can be formed (see Low-Pass Filtering section) and also provides a means for setting the overall gain to values other than ×20 (see Altering the Gain section).

The output buffer has a gain of ×2, set by the feedback network around op amp A2, formed by R15 and R13‖R14. Note that this gain is not trimmed to a precise value, but may have a tolerance of ±3% (max). Only the overall gain of A1 and A2 is trimmed to within ±0.5% by R5. As a consequence, the gain of A1 may be in error by ±3% (max) as the trim to R5 absorbs the initial error in the gain of A2. In most applications Pins 3 and 4 are simply tied together, but the output buffer can be used independently if desired. The offset voltage of A2 is nulled during manufacture. R17 is included to minimize the offset due to bias currents. It is recommended, in applications where A2 is used independently and the source resistance is less than 100 kΩ, that the necessary extra resistance should be included.

The output of A2 is the collector of a PNP transistor whose emitter is tied to $+V_S$. The bias current out of the inverting input of this amplifier generates an offset voltage of about +1 mV in R13‖R14, which is passed directly to the output via R15. This sets the lowest output that can be reached when there is no load resistor. However, the output can drive a 1 kΩ load to at least +4.5 V when $+V_S$ = +5 V. If operation to much lower minimum voltages is essential, a load resistor can be added externally.

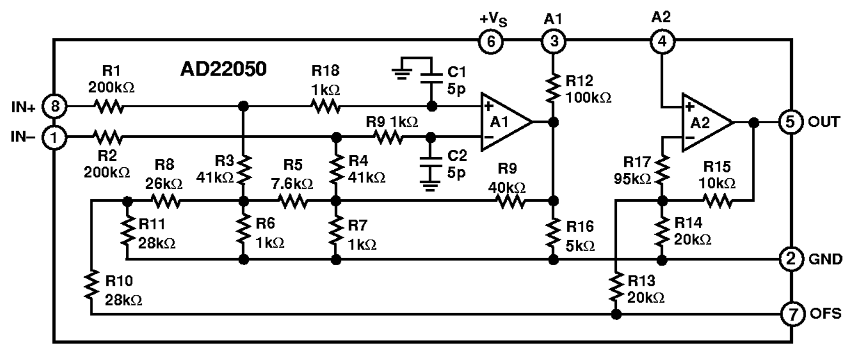
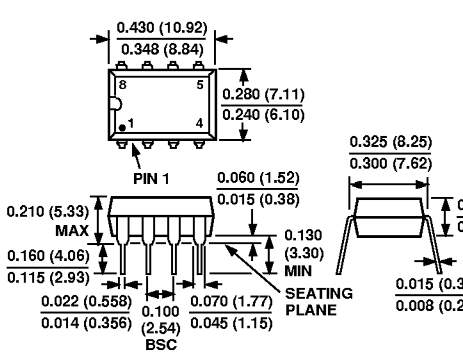



*Figure 16. Simplified Schematic of AD22050, Including Component Values*

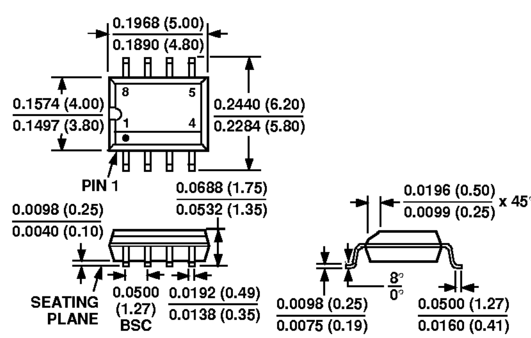
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### Plastic Mini-DIP Package (N-8)




### Plastic SOIC Package (SO-8)

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